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DS, GS, AND DEPOT MAINTENANCE MANUAL

INTERROGATOR SET AN/TPX-50

(ELECTRICAL SYNCHRONIZER SN-421/TPX-50)

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HEADQUARTERS, DEPARTMENT OF THE ARMY
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DS, GS, and Depot Maintenance Manual

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(ELECTRICAL SYNCHRONIZER SN-421/TPX-50)

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CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual contains direct support, general support, and depot maintenance information and instructions for Synchronizer, Electrical SN-421/TPX-50, hereinafter referred to as the synchronizer. Chapters 2 through 10 cover the functional operation of the synchronizer circuits; chapters 11 through 20 cover troubleshooting, alignment, and testing of those circuits; and chapters 21 and 23 cover alignment and testing of the complete synchronizer. Chapter 24 contains all fold out illustrations, and is followed by the alphabetical index.

b. The synchronizer is one assembly of Interrogator Set AN/TPX-50, which is an identification, friend, or foe equipment (IFF set) used in conjunction with a short range radar set. However, this manual treats the synchronizer as though it were a functional entity. References are made to other assemblies of the IFF set, or to the IFF set itself, or to the associated radar set only where necessary to maintain continuity of the information presented. For additional information pertaining to the synchronizer as a part of the IFF set, refer to TM 11-5895-687-12 and to TM 11-5895-687-35-1.

c. The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commander, U.S. Army Electronics Command, ATTN: AMSEL-MA-SR, Fort Monmouth, N.J. 07703.

NOTE

For applicable forms and records, refer to TM 11-5895-687-12.

1-2. Indexes of Publications

a. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions or changes to this manual or additional publications pertaining to the synchronizer.

b. Refer to the latest issue of DA Pam 310-7 to determine whether there are any modification work orders (MWO's) applicable to the synchronizer.

1-3. General Information

a. Graphic Symbols. The graphic symbols used in the illustrations of this manual are in accordance with MIL-STD-15-1A *Electrical and Electronic Symbols* and MIL-STD-806B *Graphic Symbols for Logic Diagrams.* The logic symbols, and the integrated circuit symbols derived therefrom, are explained in chapter 2.

b. Reference Designations. Reference designations have been assigned throughout the IFF set in accordance with the unit-numbering method outlined in ASA Y32.16-1968 *American Standard Electrical and Electronics Reference Designations.* That method identifies the synchronizer as assembly 1A2, designating it as the second assembly (A2) of the first free-standing inclosure (unit 1) of the IFF set. The synchronizer subassemblies and piece-parts are similarly identified, each with a class letter and location number, and these are added level by level to the synchronizer reference designation 1A2, so that each part has a complete reference designation different from every other part in the IFF set. An example of a complete reference designation for a piece-part is 1A2A1A6Q3, which identifies the third transistor (Q3) on the sixth card (A6, the low level line driver card) in the first module (A1, the interface module) of the synchronizer (1A2). The third transistor on a different card would also be identified as Q3, but its complete reference designation would differ in one or more of the portions that prefix the Q3. For a more detailed discussion of the unit-numbering method of assigning reference designations, refer to TM 11-5895-687-35-1, paragraph 5-6. For a listing of the subassembly reference designations assigned within the synchronizer, refer to paragraph 24-2 of this manual. The reference designations assigned to piece-parts are shown adjacent to or within the piece-part symbols in the corresponding assembly or subassembly schematic diagrams.

c. Panel Markings. Equipment panel markings are capitalized whenever they are mentioned in text and are blocked (inclosed within rectangular boxes) whenever they are shown in illustrations.

d. Integrated Circuits. The integrated circuits

used in the synchronizer are internally quite complicated, but they are nevertheless piece-parts from a repairman's standpoint, because none of their internal circuitry is accessible. The repairman will therefore be more directly concerned with the relationships among the input and output signals at their external terminals than with their internal electronics, because it is the observed signal relationships that provide the good/bad information needed to decide whether or not an integrated circuit must be replaced. For this reason, and to avoid unnecessarily complicating the subassembly schematic diagrams, the internal schematic diagrams of integrated circuits are not included in this manual. Instead, each integrated circuit or each part of an integrated circuit having two or more independent parts is represented by a symbol which, when properly understood, describes pictorially the satisfactory signal relationships. The integrated circuit symbols are adaptations of the nearest equivalent logic symbols, and are explained with the logic symbols in chapter 2. A thorough understanding of the information presented in chapter 2 is therefore essential to an understanding of the logic diagrams, schematic diagrams, and associated discussions in this manual.

CHAPTER 2

LOGIC SYMBOLS AND INTEGRATED CIRCUIT SYMBOLS

2-1. General

This chapter explains the logic symbols and integrated circuit symbols used in the logic diagrams and schematic diagrams of this manual. These symbols are specialized block diagram symbols for stages and circuits which are operated at the nonlinear extremes of their characteristics to provide switching functions of the kinds generally known as digital or logical functions. The input and output signals of such stages and circuits are correspondingly nonlinear: each signal is (or can be adequately represented as being) a switched voltage having only two possible voltage values, or levels, called its high and low levels. The logic symbol or integrated circuit symbol for each stage or circuit is a graphical representation of its digital or logical function, together with the particular input and output signal levels involved in that function, and is thus equivalent to a functional description of the stage or circuit in pictorial form.

2-2. Logic Symbols

Each logic symbol consists of a distinctive shape, or a distinctively labeled block, with signal level designations (high or low) at the input and output terminals. The distinctive shape or distinctively labeled block identifies the function of the stage or circuit and indicates the direction of signal flow. The level designations show the input levels which activate the function and the output level or levels thereby produced. With two exceptions, each signal level is designated by the presence or absence of a small circle at the corresponding terminal of the symbol. The presence of a small circle designates the low signal level, and the absence of a circle designates the high signal level. The low level of a signal is always the less positive of its two possible voltages, and is not necessarily the same voltage as the low level of any other signal. Similarly, the high level of a signal is always its more positive voltage, and is not necessarily the same as the high level of any other signal. An open circuit at any input is equivalent to a high level at that input, and a ground at any input is equivalent to a low level at that input. The two exceptions to the use of small circles are nonlogic signals ("analog" voltages such as sine waves) and complementary signals. Sine waves are identified by a frequency notation, and other analog voltages (usually feedback signals) are given relative magnitude or polarity designations in a manner to be described in paragraph 2-6 and in figure 2-2. Complementary signal levels are designated by lettering within the logic symbol where they originate, rather than by the use of a small circle for one of the two signals, as in the case of the complementary Q and $\overline{Q}$ outputs of a flip-flop.

2-3. Integrated Circuit Symbols

Integrated circuit symbols resemble logic symbols, and are used as logic symbols in logic diagrams, but they are also used in schematic diagrams as substitutes for their internal circuitry, and each must therefore provide enough functional information to account for all of its inputs and outputs. As a result, only the integrated circuit gate symbols are the same as the corresponding logic symbols (para 2-7). Other integrated circuits are either nonlogic circuits or they are combinations of logic circuits beyond the scope of individual logic symbols, and in such cases the integrated circuit symbols are "built up" from the nearest equivalent logic symbols by adding modifications whose meanings are explained where applicable in later paragraphs of this chapter.

2-4. Signal Names

The signal names used in the diagrams of this manual are English word names, or abbreviations of word names, in preference to the arbitrary alphabetic or alphanumeric symbols known as Boolean symbols. For two-level logic type signals (video pulses, square waves, gating or enabling voltages, etc.), the signal names are also presence-level designators, because the names of all signals which are low when present are overscored (notted). The absence of an overscore over the name of a signal therefore indicates either that the signal is high when present or that it is a nonlogic signal.

2-5. Amplifier (Logical Identity) Function Symbols
(fig. 2-1)

a. A single-input stage or circuit whose output level depends continuously on its input level is an amplifier, regardless of the overall gain, linearity, or inversion. Because changes in amplitude or polarity do not change the logical significance of a signal, amplification is sometimes called the logical identity function. The logic symbol for an amplifier consists of a triangle with input and output level designations. The triangle represents the amplifier function, the input level designation shows the significant level or direction of change of the input signal, and the output level designation shows the output produced in response to that level or direction of change of the input. By implication, the other level or direction of change of the input produces the opposite output response.

b. Symbols (1) and (2) in figure 2-1 are logic symbols for noninverting amplifiers, as indicated by their common truth table and by the fact that their output level designations are the same as their input level designations. The two symbols are therefore functionally interchangeable, and the choice in any particular case is made on the basis of the more significant input signal level: symbol (1) for signals whose high levels are more significant, such as positive-going pulses; symbol (2) for signals whose low levels are more significant, such as negative-going pulses. Readability of the overall logic diagram is the primary requirement in this choice and in all other choices between alternative logic symbols.

c. Symbols (3) and (4) are logic symbols for inverting amplifiers, as indicated by their common truth table and by the fact that they have opposite level designations at inputs and outputs. Here again the two symbols are functionally interchangeable, and the choice is made on the basis of the more significant signal level in the interests of readability.

d. Symbols (5) and (6) are integrated circuit symbols for inverting amplifiers, and are seen to resemble symbols (3) and (4) except for the number of input connections shown. These particular amplifiers are two-input integrated circuit gates (para 2-7) with their input terminals connected together, and they are shown as they would appear in a schematic diagram, where all integrated circuit terminals must be accounted for. In a logic diagram, integrated circuit amplifiers are shown as though they had only one input terminal, as in symbols (3) and (4). Integrated circuit gates with more than two input terminals are made to serve as amplifiers in the same manner. Although the one input signal to an integrated circuit gate being used as an inverter is logically necessary at only one input terminal of the gate, it is logically suitable for the extra terminals as well, and it is therefore usually paralleled to all input terminals of the gate (except expander terminals, or equivalent) in preference to leaving the extra terminals open (unconnected). Such extra input terminals are usually not left open, partly to eliminate the possibility of noise pickup, which might produce logically or functionally erroneous outputs, and partly to eliminate the slight increase in propagation (response) delay caused by the small but measurable capacitances to ground at the unused terminals.

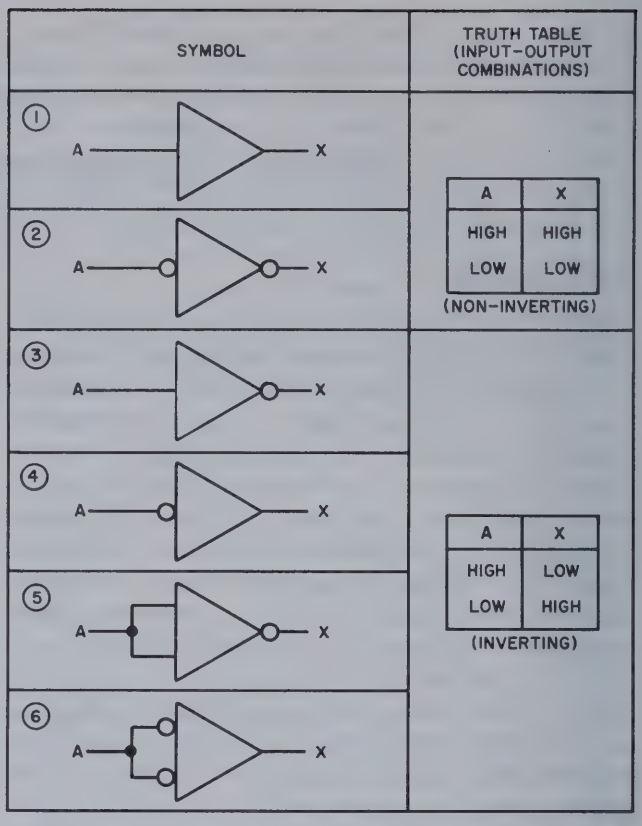


Figure 2-1. Amplifier (logical identity) function symbols.

2-6. Differential Amplifier Function Symbols
(fig. 2-2)

a. A stage or circuit which receives two variable voltage inputs and produces its output by amplifying the algebraic voltage difference between the two input voltages, called the input differential, is a differential amplifier, regardless of its gain or line-

arity. The symbols used to represent differential amplifiers are shown and explained in figure 2–2. The choice of the saturating or nonsaturating symbol for a given differential amplifier is based on the functional relationship between its two input voltages.

b. Symbol (1) is used in applications where the two input voltages are supplied by functionally independent sources, because in such cases the input differentials are usually large enough to overdrive (saturate) the differential amplifier, and the stage is then called an amplitude comparator or a threshold detector.

c. Symbol (2) or (3) is used in applications where one of the two input voltages is obtained by negative feedback from the output, or from a circuit controlled by the output, because in such cases the input differentials are normally so small that saturation rarely or never occurs, and the stage is then called an operational amplifier or a linear voltage regulator amplifier.

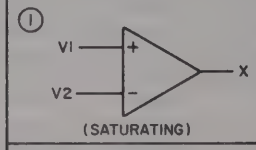
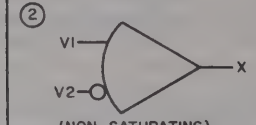
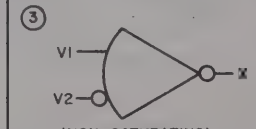
SYMBOL	FUNCTION
(1)  (SATURATING)	AMPLIFIES ALGEBRAIC VOLTAGE DIFFERENCE (INPUT DIFFERENTIAL) BETWEEN INPUT VOLTAGES VI AND V2. RESPONSE IS ESSENTIALLY LINEAR (NON-SATURATING) FOR SMALL INPUT DIFFERENTIALS, BUT IS NONLINEAR (SATURATING) FOR LARGE INPUT DIFFERENTIALS. THE INPUT LEVEL DESIGNATIONS REPRESENT POLARATIES OF VI AND V2 RELATIVE TO EACH OTHER, NOT THEIR ACTUAL LEVELS; AND THE OUTPUT LEVEL DESIGNATION REPRESENTS THE RESULTING DIRECTION OF CHANGE IN OUTPUT VOLTAGE X. SYMBOL (1) SHOWS A STAGE OR CIRCUIT IN WHICH THE INPUT DIFFERENTIALS ARE USUALLY LARGE ENOUGH TO PRODUCE SATURATING RESPONSE, AND IN WHICH X GOES HIGH WHEN VI GOES POSITIVE RELATIVE TO V2 (OR WHEN V2 GOES NEGATIVE RELATIVE TO VI). SYMBOL (2) SHOWS A STAGE OR CIRCUIT IN WHICH THE INPUT DIFFERENTIALS ARE USUALLY SMALL ENOUGH FOR NON-SATURATING RESPONSE, AND IN WHICH X INCREASES IN THE POSITIVE DIRECTION WHEN VI CHANGES IN THE POSITIVE DIRECTION RELATIVE TO V2 (OR WHEN V2 CHANGES IN THE NEGATIVE DIRECTION PELATIVE TO VI). SYMBOL (3) IS THE SAME AS SYMBOL (2) EXCEPT FOR THE DIRECTION OF CHANGE IN X.
(2)  (NON-SATURATING)	
(3)  (NON-SATURATING)	

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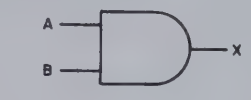
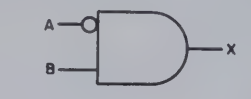
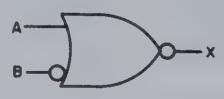
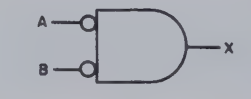
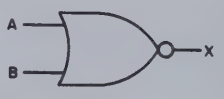
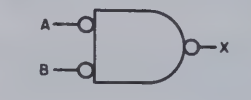
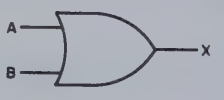
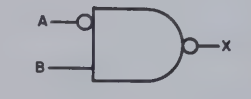
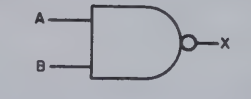
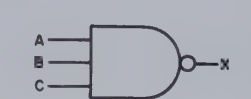
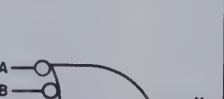
Figure 2–2. Differential amplifier function symbols.

2–7. Gate (AND, OR) Function Symbols
(fig. 2–3)

a. A multiple-input stage or circuit whose output level depends continuously on the combination of levels present at its inputs is a gate. In any given gate, one particular combination of input levels produces an output level which is opposite to the output level produced by all other possible combinations, and the gate can therefore be represented either as an AND (providing the logical AND function) for one particular combination of input levels or as an OR (providing the logical OR function) for all other possible combinations. The representation of a gate as an AND or as an OR depends on its purpose in the overall functional circuit, not on any characteristic of the gate itself. It is represented as an AND if its purpose is to detect coincidence between all of the logical events or conditions represented by its inputs. It is represented as an OR if its purpose is to detect the occurrence of any such events or conditions without the requirement of coincidence.

b. In a logic symbol for an AND, the distinctive shape which represents the AND function signifies that the designated output level (high or low) is obtained when, and only when, all of the inputs have their designated levels simultaneously. Similarly, in the logic symbol for an OR, the distinctive shape which represents the OR function signifies that the designated output level is obtained whenever any one or any combination of the designated input levels is applied. The first 12 symbols in figure 2–3 are the AND and OR symbols for six typical two-input gates, together with their truth tables. These two-input gate symbols are merely representative: gates can have any greater number of inputs and their symbols would provide a greater number of possible combinations of levels, and much larger truth tables, but would otherwise be similar, as can be seen in symbols 13 through 16, or in symbol (1) of figure 2–4.

AND	OR	TRUTH TABLE				
		INPUTS				OUTPUT
		A	B			X
① 	②	HIGH	HIGH			HIGH
		LOW	HIGH			LOW
		HIGH	LOW			LOW
		LOW	LOW			LOW
③ 	④ 	HIGH	HIGH			LOW
		LOW	HIGH			HIGH
		HIGH	LOW			LOW
		LOW	LOW			LOW
⑤ 	⑥ 	HIGH	HIGH			LOW
		LOW	HIGH			LOW
		HIGH	LOW			LOW
		LOW	LOW			HIGH
⑦ 	⑧ 	HIGH	HIGH			HIGH
		LOW	HIGH			HIGH
		HIGH	LOW			HIGH
		LOW	LOW			LOW
⑨ 	⑩	HIGH	HIGH			HIGH
		LOW	HIGH			LOW
		HIGH	LOW			HIGH
		LOW	LOW			HIGH
⑪ 	⑫	HIGH	HIGH			LOW
		LOW	HIGH			HIGH
		HIGH	LOW			HIGH
		LOW	LOW			HIGH
⑬ 	⑭	A	B	C	D	X
		HIGH	HIGH	HIGH	–	LOW
		LOW	*	*	–	HIGH
		*	LOW	*	–	HIGH
		*	*	LOW	–	HIGH
⑮	⑯ 	HIGH	HIGH	HIGH	HIGH	LOW
		LOW	*	*	*	HIGH
		*	LOW	*	*	HIGH
		*	*	LOW	*	HIGH
		*	*	*	LOW	HIGH

*IMMATERIAL. ONE LOW INPUT IS ENOUGH TO PRODUCE THE INDICATED OUTPUT LEVEL.

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Figure 2-3. Gate (AND, OR) function symbols.

c. Symbols (1) and (2) in figure 2–3 are the two possible logic symbols for a two-input gate whose output is high whenever both of its inputs are simultaneously high, and is low for any other combination of input levels. The two symbols are functionally interchangeable, as indicated by their common truth table, and the choice for any given gate is based on the significance of its output elsewhere in the overall logic diagram: symbol (1) if the output represents coincidence between two high or positive-going inputs such as a positive-going pulse and a high gating voltage; symbol (2) if the output represents the occurrence of either or both of two independent low or negative-going inputs.

d. In symbols (3) through (12), the level designations are changed one at a time to show the effect on their input-output relationships, as indicated by the associated truth tables.

2–8. Special Gate Combinations
(fig. 2–4)

a. There are three ways in which gates are combined for common functions in the present equipment. Two of these are shown in figure 2–4, and the third is shown by symbol (2) in figure 2–5.

b. Symbol (1) in figure 2–4 is a combination of integrated circuit gate symbols which performs an expanded-gate function, together with the associated truth tables. This particular combination is an AND circuit consisting of an expandable four-input gate with the outputs of two four-input expander gates connected to its E (expand) terminal. The result is a 12-input AND whose output is low when, and only when, all 12 inputs are simultaneously high, and is high for any other combination of input levels. This gate combination is shown as it would appear in a schematic diagram, where all integrated circuit terminals must be accounted for. In a logic diagram, the combination would be shown as a single 12-input AND. The small AND shape shown on the junction of the two expander gate outputs is called a dot-AND because of its appearance. A dot-AND, or the equivalent dot-OR, at any signal junction has two purposes: it calls attention to the fact that the signal at the junction has more than one source, and it indicates the direction of signal flow toward the common destination.

c. Symbol (2) in figure 2–4 is the logic symbol for an exclusive-OR, and symbol (3) is the equivalent combination of integrated circuit gate symbols. The principal use of this gate combination is to compare two bits of logical or binary data, such as bits A and B in the symbols shown. Each bit is applied as a pair of complementary levels with the cross-coupling shown in symbol (3). The output, X, then represents the equality or inequality of the two input bits: X is low whenever the two bits are the same (both "1" or both "0"), but is high whenever the two bits are different (a "1" and a "0"). The name exclusive-OR is derived from the formal logical statement: "X implies A or B exclusively." That is, X is high whenever A or B is "1" (or "0"), but not when both are "1" (or "0"). By comparison, individual gates such as those shown in figure 2–3 are nonexclusive ORs, because they do not respond to each input exclusively, and they are therefore sometimes called inclusive ORs.

d. Symbol (2) in figure 2–5 is a combination of two integrated circuit OR symbols which acts as a set-reset flip-flop. Flip-flops are discussed in the next paragraph.

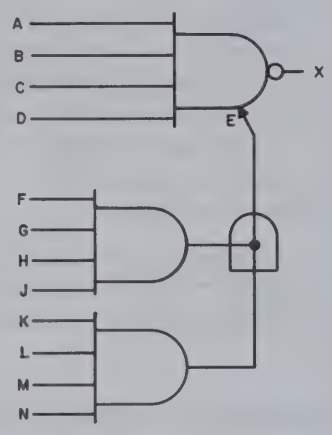
2–9. Flip-flop (Storage) Function Symbols
(fig. 2–5)

a. A flip-flop has two stable states (a set or "1" state, and a reset or "0" state) and delivers two complementary outputs (Q and $\overline{Q}$) whose levels represent the flip-flop state: in the set or "1" state, Q is high and $\overline{Q}$ is low; and in the reset or "0" state, Q is low and $\overline{Q}$ is high. Because a flip-flop is stable in either state, it must be switched from one state to the other by an external input (set input or reset input). When switched into the set state by a set input, a flip-flop remains in the set state, regardless of changes in the set input, until switched into the reset state by a reset input; and it then remains in the reset state, regardless of changes in the reset input, until switched back to the set state by another set input. Because it remains in each state until switched to the other state, a flip-flop can be said to "store" its set and reset inputs, and for this reason flip-flop functions are sometimes called storage functions. The set and reset inputs are normally never coincident in time, because if both were present simultaneously they would hold the flip-flop in an anomalous state (Q and $\overline{Q}$ levels identical, rather than complementary) for the duration of coincidence.

b. Symbol (1) in figure 2–5 is the logic symbol for a flip-flop which responds to low (negative-going) set and reset inputs, and symbol (2) shows an equivalent combination of two-input ORs, called an OR flip-flop. These are integrated circuit ORs of the type covered by symbol (12) in figure 2–3, with its associated truth table. The operation of the OR

SYMBOL

TRUTH TABLE
(INPUT-OUTPUT COMBINATIONS)



① EXPANDED AND SCHEMATIC

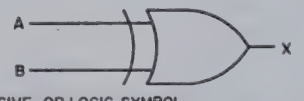
FOR EXPANDABLE GATE ALONE

INPUTS					OUTPUT
A	B	C	D	E	X
HIGH	HIGH	HIGH	HIGH	HIGH*	LOW
LOW	**	**	**	**	HIGH
**	LOW	**	**	**	HIGH
**	**	LOW	**	**	HIGH
**	**	**	LOW	**	HIGH
**	**	**	**	LOW	HIGH

FOR THE EXPANDERS & DOT-AND

INPUTS								OUTPUT
F	G	H	J	K	L	M	N	E
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH*
LOW	**	**	**	**	**	**	**	LOW
**	LOW	**	**	**	**	**	**	LOW
**	**	LOW	**	**	**	**	**	LOW
**	**	**	LOW	**	**	**	**	LOW
**	**	**	**	LOW	**	**	**	LOW
**	**	**	**	**	LOW	**	**	LOW
**	**	**	**	**	**	LOW	**	LOW
**	**	**	**	**	**	**	LOW	LOW

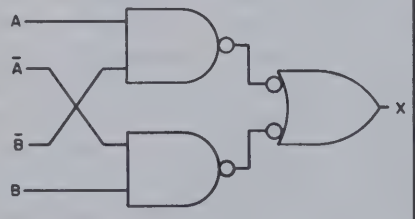
* OPEN CIRCUIT, OR EQUIVALENT (BACK-BIASED DIODE).
** IMMATERIAL. ONE LOW INPUT IS ENOUGH TO PRODUCE THE INDICATED OUTPUT LEVEL.



② EXCLUSIVE-OR LOGIC SYMBOL

INPUTS***		OUTPUT
A	B	X
HIGH	HIGH	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
LOW	LOW	LOW

*** $\bar{A}$ IS THE COMPLEMENT (LOGICAL INVERSE) OF A. THAT IS, $\bar{A}$ IS LOW WHEN A IS HIGH, AND IS HIGH WHEN A IS LOW. SIMILARLY $\bar{B}$ IS THE COMPLEMENT OF B.



③ EXCLUSIVE-OR SCHEMATIC

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Figure 2-4. Gate combination symbols.

flip-flop in symbol ② of figure 2-5 can be understood by examining its response to alternate set (S) and reset (R) inputs. To apply a set input, S is made low, resulting in a high OR1 output (Q), which combines at OR2 with the high R level (absence of a reset input) to produce a low OR2 output ($\overline{Q}$), which is subsequently enough to maintain the high OR1 output (Q), regardless of changes in the S level. The set input has thus switched the OR flip-flop into the set state, in which Q is high and $\overline{Q}$ is low, and the OR flip-flop then remains in this state until a reset input is applied by making R low. The low R input results in a high OR2 output ($\overline{Q}$), which combines at OR1 with the

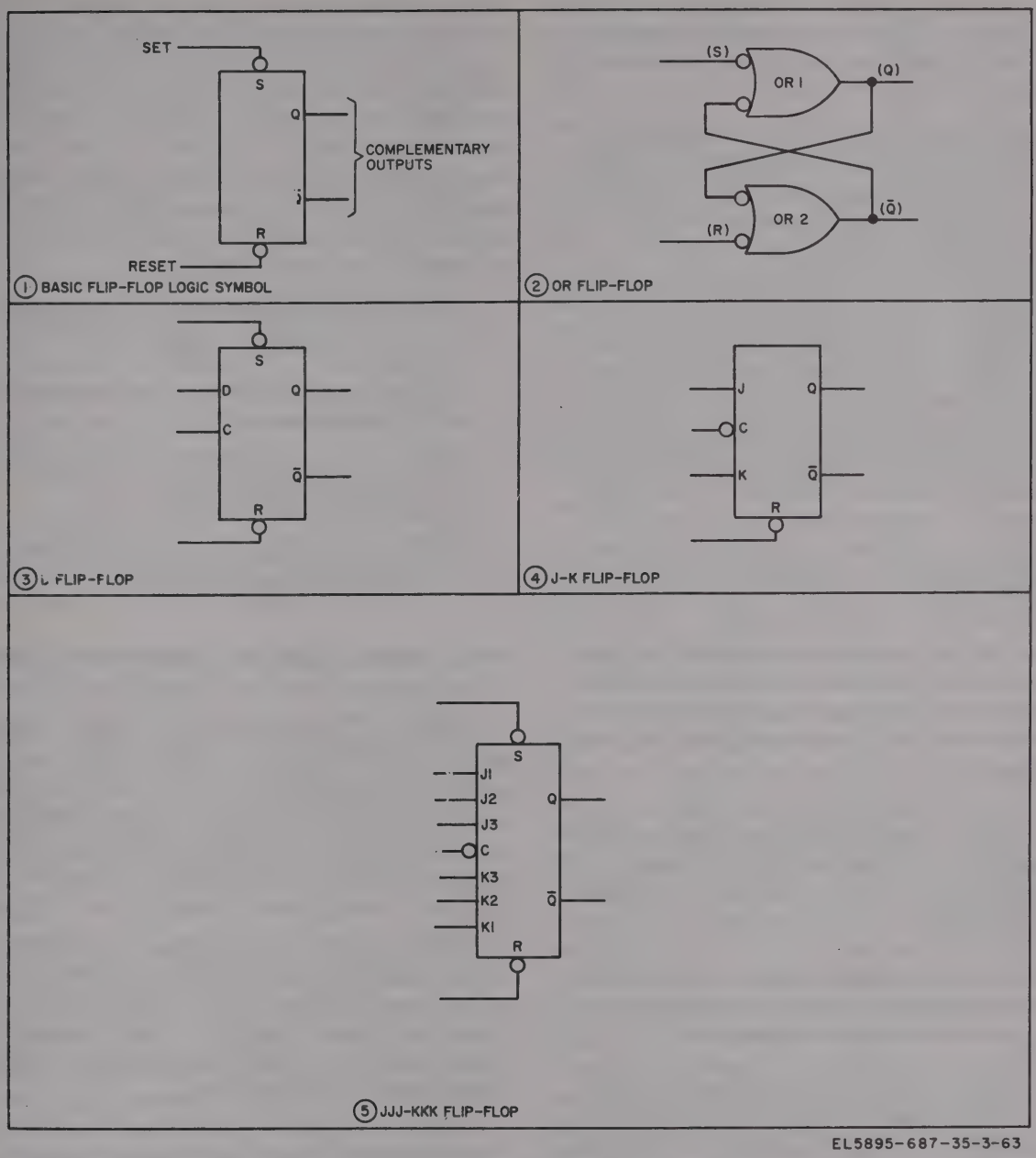

Figure 2-5. Flip-flop function symbols.

high S level (absence of a set input) to produce a low OR1 output (Q), which is subsequently enough to maintain the high OR2 output ($\overline{Q}$), regardless of changes in the R level. The reset input has thus switched the OR flip-flop into the reset state, in which Q is low and $\overline{Q}$ is high, and the OR flip-flop then remains in this state until another set input is applied.

c. Symbol (3) is the integrated circuit symbol for one of the three types of integrated circuit flip-flop used in the synchronizer. This type of flip-flop is called a D flip-flop, and its symbol is seen to be the same as symbol (1) except for the addition of two inputs: a C (clock) input and a D (data, or clock-steering) input. These inputs provide for a method of applying set and reset inputs called clocking the flip-flop. When the S and R inputs are both high, this flip-flop is clocked by positive-going edges of the waveform at C, which act either as set or reset inputs, depending on the level at D. If D is high at the time of a positive-going edge at C, that edge will act as a set input, and the flip-flop will be clocked set. Similarly, if D is low at the time of a positive-going edge at C, that edge will act as a reset input, and the flip-flop will be clocked reset.

Low inputs at S and R have the same effect as in symbols (1) and (2), and are called direct-set and direct-reset inputs because they override the C and D inputs.

d. Symbol (4) is the integrated circuit symbol for another of the three types of integrated circuit flip-flop used in the synchronizer. This type of flip-flop is called a J–K flip-flop, and its symbol is seen to resemble symbol (1) except for the lack of an S input and the addition of three other inputs: a C (clock) input, and two clock-steering inputs (J and K). This flip-flop can be clocked only if R is high, because low R forces the flip-flop into the reset state and prevents any response to the J, K, and C inputs. The R input is therefore called a direct-reset input, as in the case of the D flip-flop described in *c* above. When R is high, clocking is controlled by the J and K levels, which take effect while C is high and determine whether the flip-flop will be clocked set, clocked reset, toggled, or not clocked at all when C subsequently goes low.

(1) If J is high and K is low while C is high, then when C goes low the flip-flop will be clocked set, unless it was already set, in which case it will not be clocked (will remain set).

(2) If J is low and K is high while C is high, then when C goes low the flip-flop will be clocked reset, unless it was already reset, in which case it will not be clocked (will remain reset).

(3) If J and K are both high while C is high, then when C goes low the flip-flop will be toggled (its state will be reversed).

(4) If J and K are both low while C is high, then when C goes low the flip-flop will not be clocked (will remain in its existing state).

(5) The present equipment is designed so that in most applications of this flip-flop the required J and K levels are applied before C goes high and are then maintained at least until C has gone low.

e. Symbol (5) is the integrated circuit symbol for the remaining type of integrated circuit flip-flop used in the synchronizer. This type of flip-flop is called a JJJ–KKK flip-flop, and is the same as the J–K flip-flop described in *d* above, except that this flip-flop has a direct-set (S) input and has a greater number of J and K inputs to provide for additional sources of clock-steering control. Internally, the J inputs and the K inputs are separately ANDed to produce the equivalents of the single J and K inputs in symbol (4). The J and K inputs are all shown with high level designations (no small circles) because they are internally ANDed in the manner covered by symbol (1) in figure 2–3. Thus, the operation of this flip-flop is adequately described by *d* above, if the J and K levels mentioned in that explanation are understood to mean combined–J and combined–K levels as follows:

(1) For a high combined–J, all J inputs must be simultaneously high.

(2) For a low combined–J, one or more of the J inputs must be low.

(3) For a high combined–K, all K inputs must be simultaneously high.

(4) For a low combined–K, one or more of the K inputs must be low.

2–10. Typical Flip-Flop Application Symbols (fig. 2–6)

a. Symbol (1) in figure 2–6 is a typical method of connecting a J–K flip-flop (para 2–9*d*) for simple set-reset applications, shown as it would appear in a schematic diagram, where all integrated circuit connections must be accounted for. Here, the flip-flop is clocked set by negative-going edges of the set input at C, and is directly reset by low or negative-going reset inputs at R. The J connection to $\overline{Q}$ makes J high when the flip-flop is in the reset state, and thus provides a suitable J level for clocking the flip-flop set (para 2–9*d*(1)). The K connection to ground holds K low, and thus prevents clocking the flip-flop reset (para 2–9*d*(4)).

(1) Because direct-reset inputs (low R) override and cancel clock-set inputs, the set and reset inputs can overlap in time without placing the flip-flop in an anomalous state, unlike the flip-flops shown by symbols (1) (2) in figure 2–5 (para 2–9*a*).

(2) Because a set input cannot clock the flip-flop set unless J is high, the J level in some applications is supplied as a control voltage (enable) from a separate source, rather than by connection to $\overline{Q}$.

b. Symbol (2) in figure 2–6 shows how a flip-flop with the connections of symbol (1) would appear in a logic diagram. Because those connections make J

high whenever need be, the J connection is not shown. However, the K connection to ground is always shown to avoid confusion between the set-reset function of this arrangement and the toggling (2:1 countdown) function shown by symbol (4).

c. Symbol (3) is a typical method of connecting a J–K flip-flop for toggling (2:1 countdown) applications, shown as it would appear in a schematic diagram. Here the connections are the same as in symbol (1) except that K is connected to Q, rather than to ground. When the reset and disable input at R is high, the flip-flop reverses state on each negative-going edge of the toggle input at C, because the J and K levels are each high whenever need be. When the flip-flop is in the reset state, $\overline{Q}$ makes J high so that the next negative-going edge of the toggle input can clock the flip-flop set (para 2–9*d*(1)), and in the set state Q makes K high so that the next negative-going edge of the toggle input can clock the flip-flop reset (para 2–9*d*(2)), and so on.

d. Symbol (4) shows how a flip-flop with the connections of symbol (3) would appear in a logic diagram if the flip-flop were not part of a binary counter. (If it were part of a binary counter, it would be included within a combination symbol with the other flip-flops of the counter, and would not be shown separately.) Because the J and K connections make J and K high whenever need be, they are not shown.

e. Symbol (5) is part of the logic symbol for a binary counter, and is intended only to show how the symbol is constructed. (Incomplete symbols are never used in actual logic diagrams.) This combination symbol represents the counter flip-flops as a group arranged in ascending order of numerical significance, from least-significant bit (2^0) to most-significant bit (2^n), with their reset (R) or set (S) inputs indicated, if used, along one of the long sides and their Q and $\overline{Q}$ outputs indicated, if used, along the opposite long side. The input to be counted is shown applied to the least-significant (2^0) end of the symbol. The partial symbol shown represents part of a binary counter which is reset and disabled when the counter control line is low, and which counts negative-going pulses or negative-going edges of the input when the counter control line is high. Symbols (6), (7), and (8) are the equivalent stages of the three different binary counters, as explained below.

f. Symbol (6) shows the first four stages of an asynchronous counter as they would appear in a schematic diagram. Each stage in this counter is seen to be connected as in symbol (3). When the counter control line is high, the input is counted down 2:1 by the first stage, the 2^0 output of the first stage is counted down 2:1 by the second stage, the 2^1 output of the second stage is counted down 2:1 by the third stage, and so on until the counter control line is made low to reset and disable the counter. This counter is asynchronous because on counts where two or more flip-flops must change state together they do not change states in synchronism: the propagation delay of the first stage delays the input to the second stage, the propagation delay of the second stage delays the input to the third stage, and so on. As a result, such counts pass from flip-flop to flip-flop like a wave, or ripple, and asynchronous counters are therefore commonly called ripple counters.

g. Symbol (7) shows the first four stages of a paired-synchronous ripple counter as they would appear in a schematic diagram. In this type of counter the flip-flops are arranged in synchronously clocked pairs, each pair consisting of two successive flip-flops which are clocked by the same C waveform. The input is applied as the common C waveform for the first and second stages, the 2^1 output of the second stage is applied as the common C waveform for the third and fourth stages, the 2^3 output of the fourth stage is applied as the common C waveform for the fifth and sixth stages, and so on. When the counter control line is high, the input is counted down 4:1 by the first two stages, the 2^1 output (with only the propagation delay of the second stage) is counted down 4:1 by the third and fourth stages, the 2^3 output (with only the propagation delay of the second and fourth stages) is counted down 4:1 by the fifth and sixth stages, and so on until the counter control line is made low to reset and disable the counter. Thus, for a given number of stages, a counter of this type has half as many C waveforms, and therefore only half as much ripple delay, as the simple ripple counter of symbol (6). The synchronous clocking connections of the paired flip-flops in symbol (7) may be explained as follows:

(1) The first flip-flop supplies the 2^0 output of the counter. Because this output must change on every negative-going edge of the input, the first flip-flop is connected to toggle as in symbol (3).

(2) The second flip-flop supplies the 2^1 output. This output must change on every count

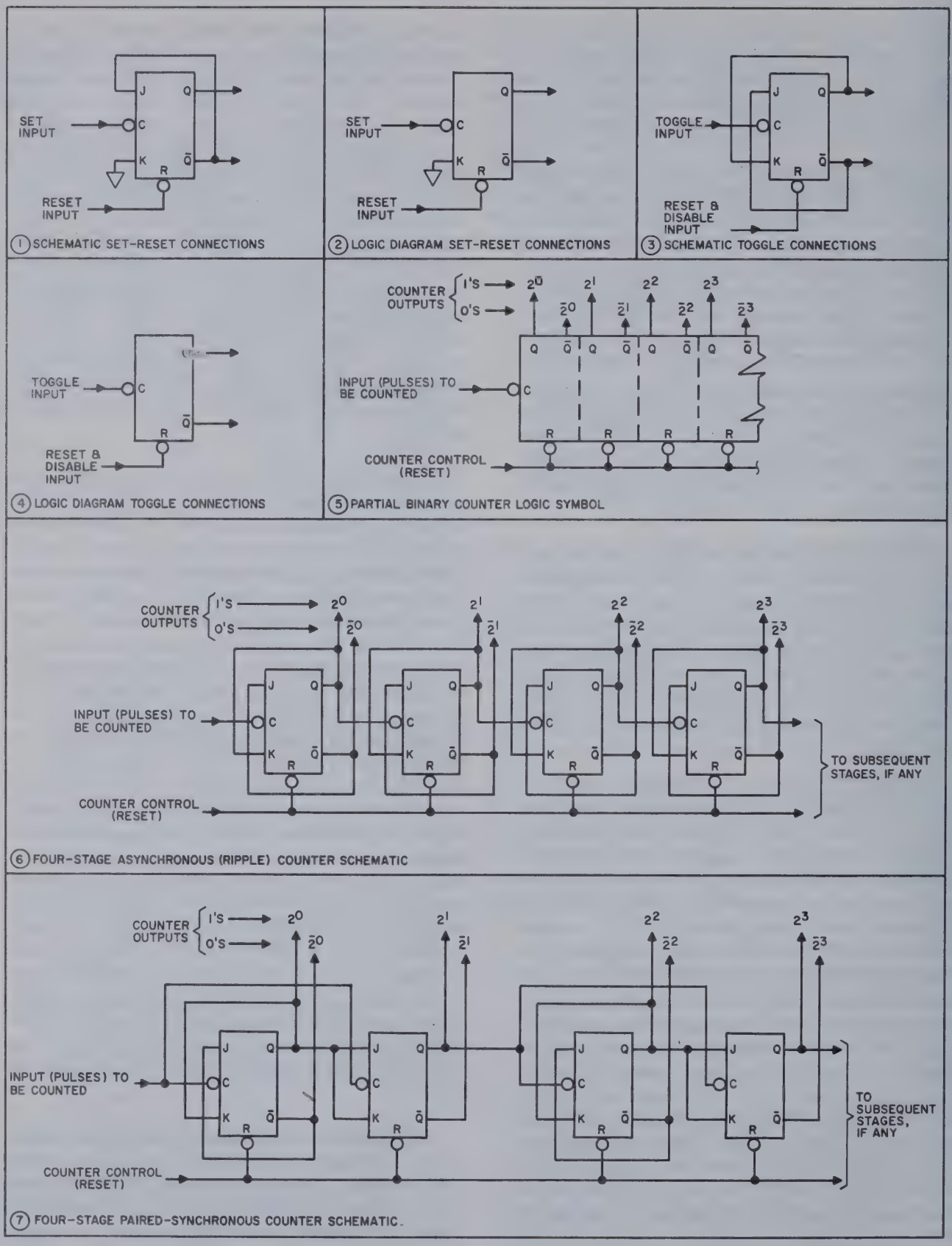

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Figure 2-6①. Typical flip-flop application symbols (sheet 1 of 2).

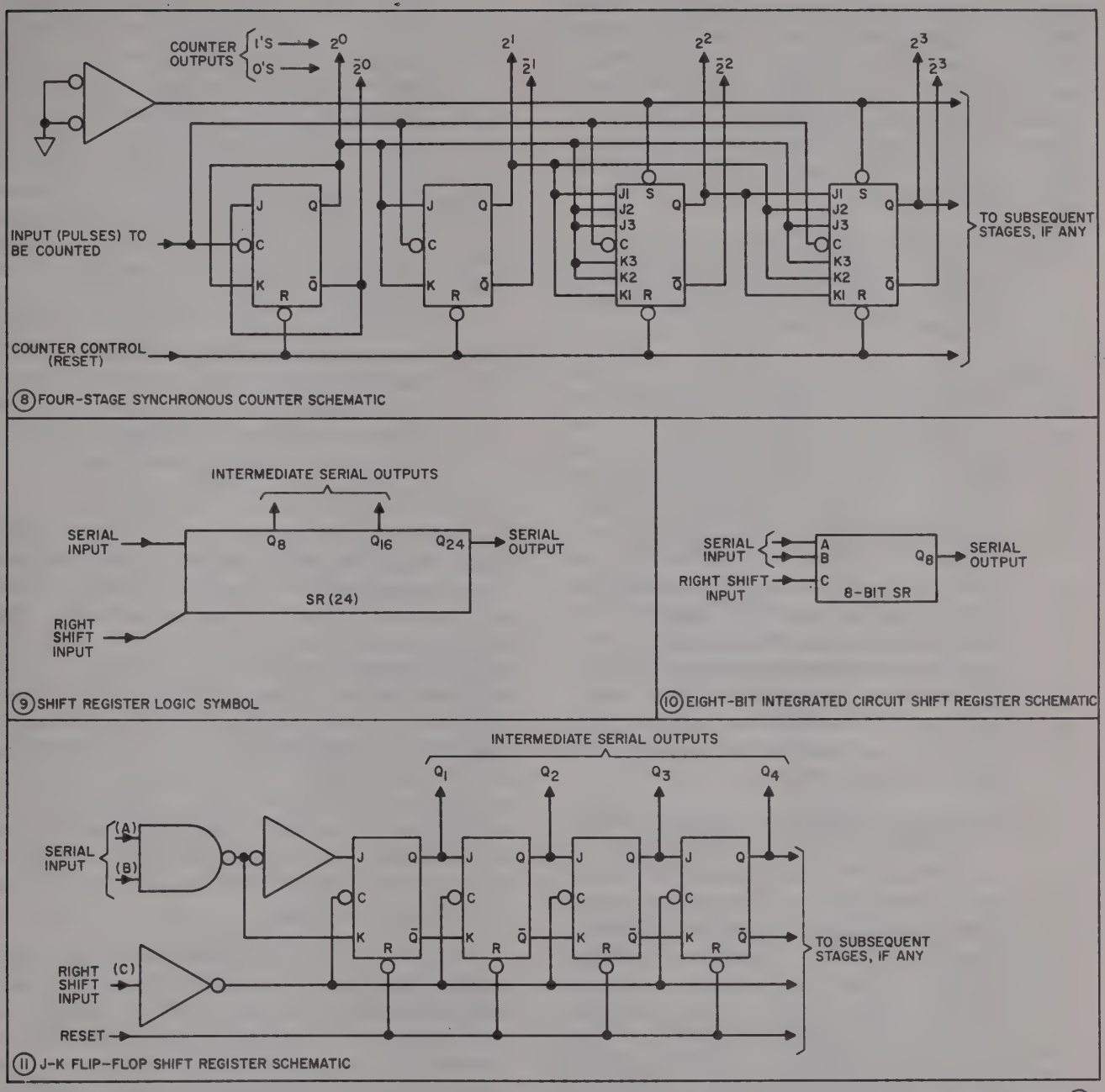


Figure 2-6②. Typical flip-flop application symbols (sheet 2 of 2).

which is a multiple of 2, and the multiples of 2 are the counts that occur when the 2^0 bit has been a "1" (2^0 output high). Accordingly, the 2^0 output is applied to the J and K inputs of the second flip-flop so that negative-going edges of the input can toggle the second flip-flop when, and only when, the 2^0 bit has been a "1."

(3) The connections and operation of the next pair of flip-flops, and of each succeeding pair, are the same as in (1) and (2) above, except for the counter outputs involved.

h. Symbol (8) shows a four-stage synchronous counter, or the first four-stage portion of a four-synchronous ripple counter, as it would appear in

a schematic diagram. Here all four stages receive the input as their common C waveform and are thereby clocked in synchronism. Thus, for a given number of stages, a counter of this type has one-fourth as many C waveforms, and therefore only one-fourth as much ripple delay, as the simple ripple counter of symbol (6). The synchronous counting connections of the four flip-flops in symbol (8) may be explained as follows:

(1) The first two flip-flops are connected in exactly the same way as the first two flip-flops in symbol (7), and are adequately described by *g*(1) and *g*(2) above.

(2) The third flip-flop supplies the 2^2 output of the counter. This output must change on every count which is a multiple of 4, and the multiples of 4 are the counts that occur when the 2^0 and 2^1 bits have simultaneously been "1's" (2^0 and 2^1 outputs both high). Accordingly, the 2^0 and 2^1 outputs are each applied to a J input and a K input of the third flip-flop so that negative-going edges of the input can toggle the third flip-flop when, and only when, the 2^0 and 2^1 outputs have been simultaneously high. The third flip-flop must therefore be a type which provides for clock-steering control from more than one source, such as the JJJ–KKK flip-flop shown.

(3) The fourth flip-flop supplies the 2^3 output of the counter. This output must change on every count which is a multiple of 8, and the multiples of 8 are the counts that occur when the 2^0, 2^1, and 2^2 bits have all simultaneously been "1's" (2^0, 2^1, and 2^2 outputs all high). Accordingly, the 2^0, 2^1, and 2^2 outputs are each applied to a J input and a K input of the fourth flip-flop so that negative-going edges of the input can toggle the fourth flip-flop when, and only when, the 2^0, 2^1, and 2^2 outputs have been simultaneously high. The fourth flip-flop must therefore be a type which provides for clock-steering control from more than one source, such as the JJJ–KKK flip-flop shown.

(4) Synchronous counters of more than four stages would require flip-flops with more than three–J, three–K clock steering, and also would place excessive loads on the common lines, and so are not used in the present equipment.

(5) As has been previously mentioned (para 2–5*d*), unused input terminals of integrated circuits (other than expander terminals, or equivalent) are usually not left unconnected because of the possibility of noise pickup and speed reduction. Instead, such unused terminals are supplied with logically suitable signals or with a fixed dc level (continuously high, but preferably not as high as $+V_{CC}$). The grounded-input inverter shown in this counter is one method used. This inverter actively supplies the continuously high level needed at the set (S) terminals of the third and fourth flip-flops. Another method is shown at the third stage, where three J and three K terminals are available, but only two of each are actually required: to avoid open circuits, the 2^0 output is used as a logically suitable level for the extra J and K terminals.

i. Symbol (9) is the logic symbol for a shift register, showing its salient features. This particular example represents a 24-stage right-shifting register with serial input, serial output from the 24th stage, and intermediate serial outputs from the eighth and sixteenth stages. The absence of a small circle at the right shift input indicates that this register shifts right on positive-going shift right pulses or on positive-going edges of the shift right waveform; and the absence of a shift left input indicates that the register does not shift left. The absence of a small circle at the serial input designates the level of that input as high for set. Finally, the absence of parallel input lines indicates that the register does not accept parallel inputs.

j. Symbol (10) is the symbol for an integrated circuit 8-bit shift register. This is an eight-stage right-shifting register which shifts right on positive-going edges of the shift right input waveform at its clock (C) terminal. It accepts a serial input through an internal AND which reads the input as a set input when the serial input levels at A and B are simultaneously high, but as a reset input when A or B, or both, are low. The serial output (Q_8) is the Q output of the eighth stage, and there are no intermediate serial outputs. For reference in the following brief description, symbol (11) was purposely constructed to show how the first four stages of a functionally similar shift register would appear in a schematic diagram if it were an electrical assembly of simpler integrated circuits that have already been described.

(1) On any one shift, if A and B are simultane-

ously high when C goes high, a set input will be shifted into the first internal flip-flop. If, instead, A or B, or both, are low when C goes high, a reset input will be shifted into the first internal flip-flop. At the same time, the existing state of the first flip-flop will be shifted into the second flip-flop, the existing state of the second flip-flop will be shifted into the third flip-flop, and so on, until the existing state of the seventh flip-flop is shifted into the eighth flip-flop and appears at Q_8, either as a high (set) output or as a low (reset) output.

(2) The same action takes place on each subsequent shift, so any given input emerges at Q_8 after eight shifts, and thus after a delay of eight times the period between successive positive-going edges at C.

k. Symbol (11) is the first four stages of a right-shifting serial input-output register composed of J–K flip-flops (para 2–9*d*), a two-input gate, and two inverters, shown as they would appear in a schematic diagram.

(1) The serial input levels at A and B are ANDed, and an inverter is used at the AND output to supply the first flip-flop with a pair of complementary J and K levels which identify the input: high J and low K for a set input, obtained when A and B are simultaneously high; or low J and high K for a reset input, obtained when A or B, or both, are low.

(2) The positive-going right shift input waveform is delivered to the common shift line through an inverter which serves two purposes: it provides the negative-going right shift edges needed at the flip-flop C inputs; and it minimizes the loading on the external source of the right shift input waveform.

(3) The direct-reset line to all stages must be high to permit shifting. A low level on this line would clear and disable the entire register.

(4) The intermediate serial output available at the Q of each flip-flop may or may not be used.

(5) On any one shift, if the serial input is a set input (A and B both high) throughout the entire time when the external shift right input is low, then regardless of its existing state the first flip-flop will be in the set state after the external shift right input goes high: it will be clocked set, if it was in the reset state, because J has been high; or it will remain set, if it was already in that state, because K has been low. Similarly, if the serial input is a reset input (A or B, or both, low) throughout the entire time when the external shift right input is low, then regardless of its existing state the first flip-flop will be in the reset state after the external shift right input goes high.

(6) Thus, when the external shift right input goes high, it shifts the existing serial input into the first flip-flop; and at the same time, in the same way, it shifts the existing state of the first flip-flop into the second flip-flop, and shifts the existing state of the second flip-flop into the third flip-flop, and so on.

(7) Successive shifts thereby pass any given input from stage to stage through the register until it reaches the last stage and becomes available at the final serial output after a total delay equal to the period between successive positive-going edges of the external shift right waveform multiplied by the total number of stages.

2–11. Single-Shot Function Symbols
(fig. 2–7)

a. A single-shot has a stable (quiescent) state and an unstable (active) state, and delivers two complementary outputs (Y and $\overline{Y}$) whose levels represent the two states: in the active state, Y is high and $\overline{Y}$ is low; and in the quiescent state, Y is low and $\overline{Y}$ is high. A single-shot remains in its quiescent state until triggered into its active state by the appropriate edge of an external input (trigger input). When triggered into the active state, a single-shot is held in the active state for a period of time (active state duration) determined by a resistance-capacitance timing network, and then automatically returns to the quiescent state, where it remains until another trigger input is applied.

b. Symbol (1) in figure 2–7 is the logic symbol for a single-shot (SS) which is triggered into its active state by negative-going edges of the waveform at its trigger (T) input, and which has an adjustable active state duration normally set for 1.0 microsecond (μsec). The purpose of the waveshape

within the symbol is to signify that the active state duration is determined within the circuit, rather than externally, and the time-labeling indicates the active state duration when properly adjusted (or the design value, if not adjustable). The waveshape can also be considered as an idealized Y output waveform, even though that is not its purpose. This symbol, like all logic symbols, is intended to show only the function and input-output responses of the circuit it represents, and is a good example of how logic symbols eliminate extraneous electronic detail in the interests of showing similar functions similarly. This one symbol, with no changes other than in trigger polarity, active state duration, and adjustment indication, can represent any single-shot circuit, regardless of the type or complexity of its circuitry.

c. Symbol (2) shows how a single-shot represented by symbol (1) might appear in a schematic diagram. This is a typical circuit for one of the two types of integrated circuit single-shot used in the synchronizer.

(1) This type of integrated circuit single-shot is triggered by negative-going edges of the waveform at its trigger (T) input when the trigger-gating (G) input is low. The uses of this type of single-shot in the synchronizer do not require the gating effect of the G terminal, and the G terminal is grounded in each case to hold it permanently low.

(2) The integrated circuit single-shot itself contains an internal timing network which provides an active state duration of approximately 80 nanoseconds. For other active state durations, external timing capacitance or resistance, or both, must be connected as shown. The external timing capacitance, if used, is placed in parallel with the internal timing capacitance by connecting it between the timing capacitance (C_T) terminal and the timing resistance (R_T) terminal. The external timing resistance, if used, is connected from R_T to $+V_{CC}$.

(3) The internal timing resistance is connected to the RX and RT terminals, but is not used in any synchronizer application. Instead R_X is connected to R_T as shown. This effectively removes the internal timing resistance from the timing network, leaving the external timing resistance as the total timing network resistance.

(4) The resistor shown connected from C_T to ground is only indirectly part of the external timing network. Its purpose is to stabilize the active state duration against changes in trigger spacing, or repetition rate. This type of integrated circuit single-shot requires a period of time, called recovery time, to recharge the total timing capacitance after each return to the quiescent state, and if retriggered before the end of that recovery time the active state duration will be shorter than normal. The resistor from C_T to ground terminates the recharge of the timing capacitance at a slightly lower voltage than would otherwise be reached, and thereby makes the active state duration slightly shorter than it would otherwise be, but in so doing it eliminates the long final portion of the recovery time which is responsible for changes in active state duration with changes in triggering rate.

(5) Two internal pullup resistors (internally connected to $+V_{CC}$) are brought out to separate terminals (R_Y and $R_{\overline{Y}}$) which can be connected to the Y and $\overline{Y}$ terminals for additional pullup capability when required by the external Y and $\overline{Y}$ loads.

d. Symbol (3) is a single-shot circuit containing the other type of integrated circuit single-shot used in the synchronizer, shown as it would appear in a schematic diagram. This type of integrated circuit single-shot is called an infinitely retriggerable single-shot.

(1) As symbolized by the internal AND-OR combination in which trigger (T) inputs are developed, this single-shot is triggered by the leading edge of coincidence between two high AND inputs and one or both of two low OR inputs.

(2) The unique characteristic of this single-shot is that when triggered into its active state it need not return to its quiescent state for recovery before being triggered again: the full active state duration begins each time a new T input is developed. As a result, the active state duration is so com-

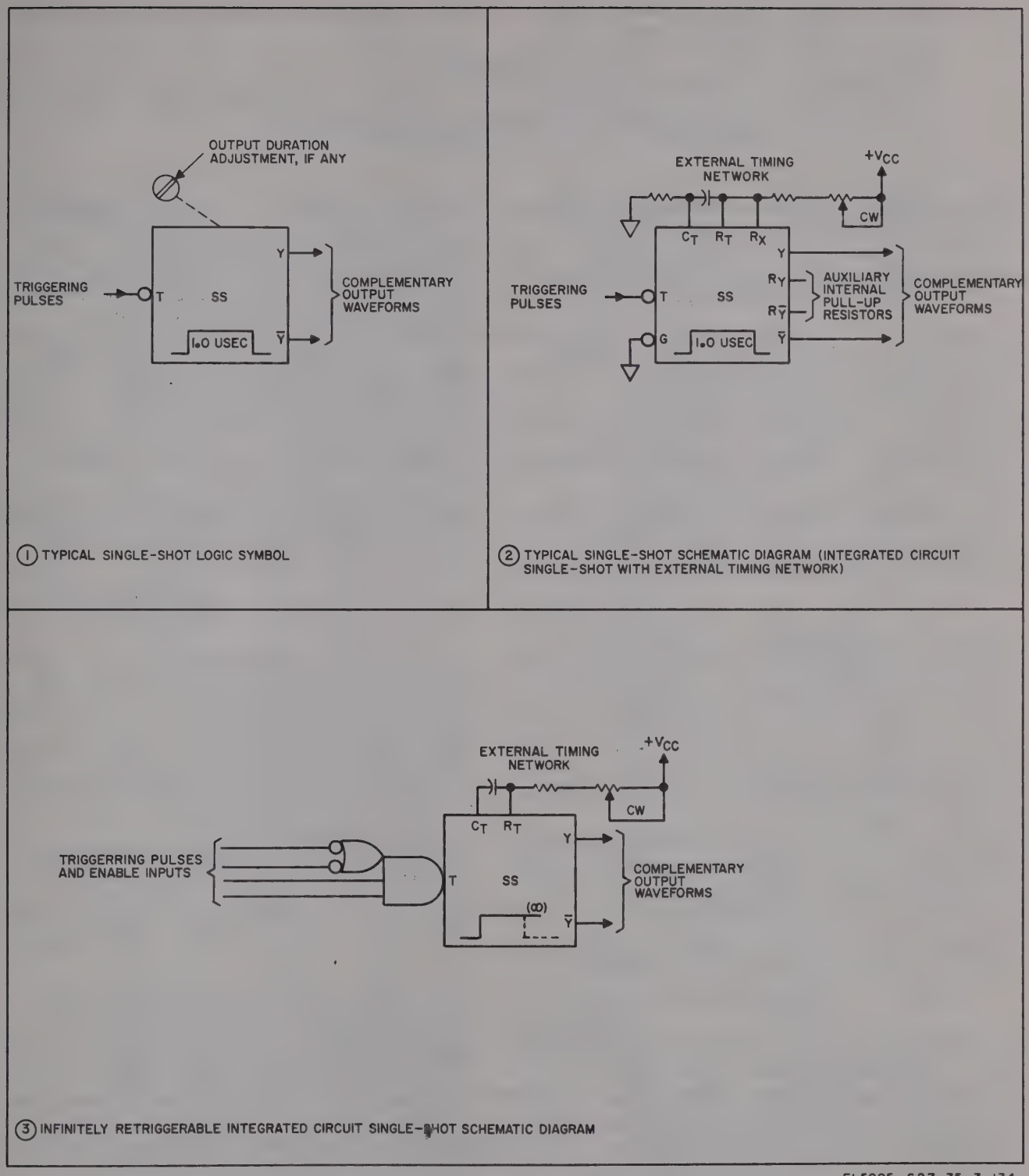


Figure 2-7. Single-shot function symbols.

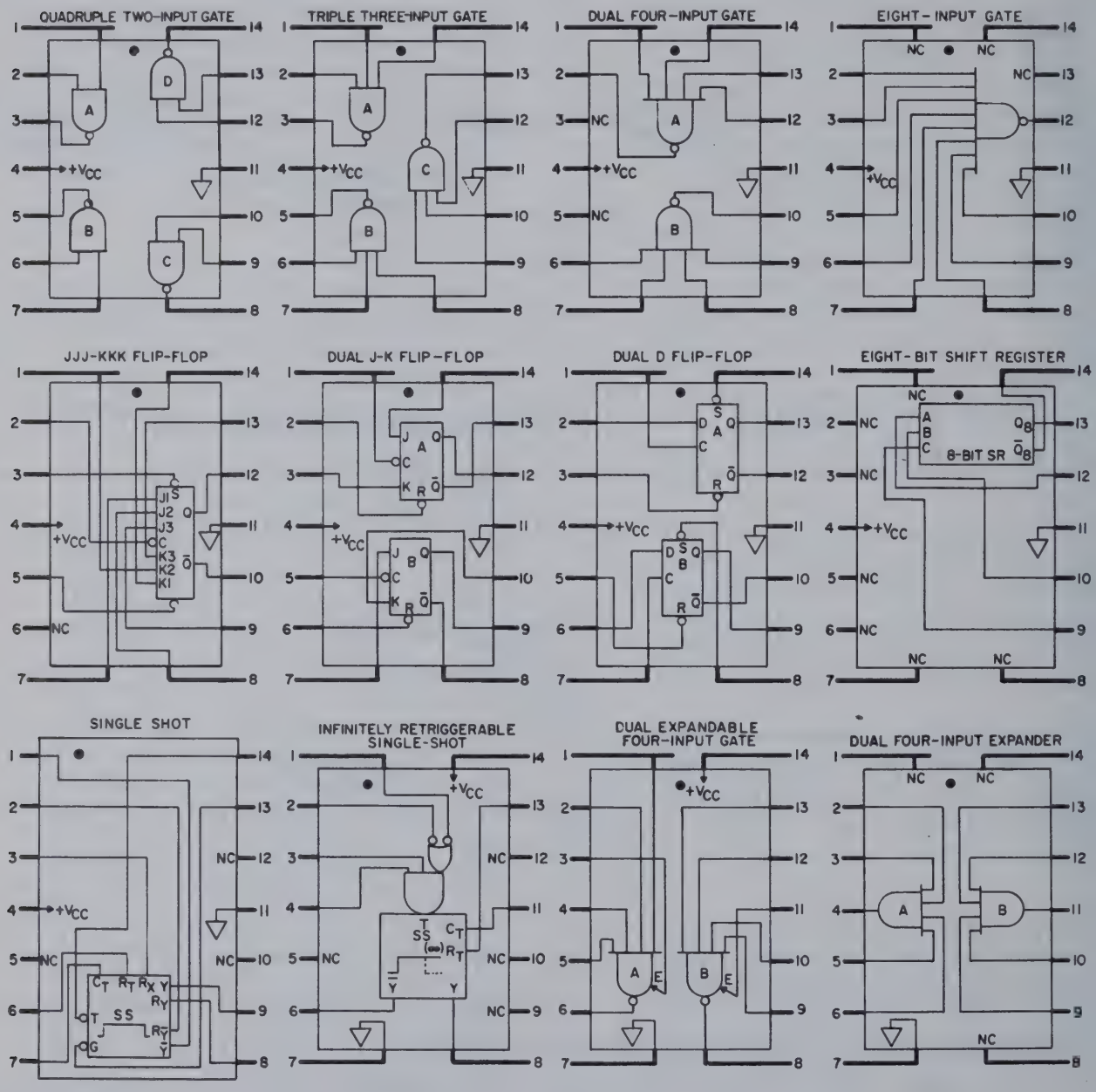
pletely independent of T pulse spacing that T pulse spacings shorter than the active state duration can hold this single-shot in the active state indefinitely. This characteristic is called infinite retriggerability.

(3) The integrated circuit single-shot itself has an internal timing capacitance of about 70 picofarads, but has no internal timing resistance. All of the timing resistance must therefore be provided externally, connected

from the timing resistance (R_T) terminal to $+V_{CC}$, as shown. External timing capacitance, if used, is placed in parallel with the internal timing capacitance by connecting it between the timing capacitance (C_T) terminal and R_T, as shown.

2-12. Integrated Circuit Terminal Identification (fig. 2-8)

Figure 2-8 provides terminal diagrams for all of the 15 types of integrated circuits used in the synchronizer.



NOTES:
1. ALL IC'S ARE SHOWN AS VIEWED FROM TOP (MARKED FACE)
2. THE DOT IN EACH IC SHOWS APPROXIMATE LOCATION OF ORIENTATION SYMBOL (DOT OR TRADE MARK, OR BOTH) STAMPED ON MARKED FACE
3. NC = NO INTERNAL CONNECTION

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Figure 2-8. Integrated circuit terminal identification.

CHAPTER 3

SYNCHRONIZER OVERALL DESCRIPTION

3-1. General

This chapter presents an overall functional description of the synchronizer, based on the synchronizer block diagram shown in figure 24-2. The purpose of the synchronizer is to time the challenging, reply decoding, and processing functions of the IFF set so that the target information (IFF display video) supplied to the associated radar set will appear at the proper radar ranges when incorporated into the radar indicator display. The synchronizer is divided into six major functional circuits: timing circuits, challenge encoding circuits, reply decoding circuits, display video interface circuits, fault indication circuits, and power supply and distribution circuits.

3-2. Timing Circuits
(fig. 24-2)

a. Radar Trigger Input. The associated radar set supplies the master timing reference for the IFF set in the form of radar triggers: one radar trigger for every sixteenth radar pulse repetition period (prp), with each radar trigger timed to occur 460 microseconds (μsec) before zero time in the corresponding radar prp. Each radar trigger is used to initiate one IFF set prp (IFF challenge-reply cycle), with the result that the radar triggers establish an IFF set pulse repetition frequency (prf) of 375 challenge-reply cycles per second (one-sixteenth of the radar prf).

b. Synchronizing Outputs. The timing circuits provide five timing signals for synchronization of the IFF set functions. Four of these are pretriggers produced in sequence after each radar trigger: a mode 4 pretrigger, a self-test pretrigger, an sif pretrigger, and a processor start pretrigger. The fifth output is a continuous 10-megacycle clock pulse train (10-mc clock), which is generated within the timing circuits for digital timing of the four pretriggers. The 10-mc clock output is delivered to the challenge encoding and reply decoding circuits for the digitally timed functions that require a 10-mc clock rate within those circuits. The 10-mc clock output is counted down 2:1 within the challenge encoding circuits, and the resulting 5-mc clock signal is delivered as an output from the challenge encoding circuits to the reply decoding and display video interface circuits for the digitally timed functions that can be carried out satisfactorily at a 5-mc clock rate. The timing and distribution of the four pretriggers are as follows:

(1) The mode 4 pretrigger is timed to occur 14.5 μsec after each radar trigger, and therefore 445.5 μsec before radar zero time. This pretrigger is reshaped and delivered to the interrogator computer for use when the IFF set is operated in mode 4. Within the synchronizer, the mode 4 pretrigger is delivered to the challenge encoding and reply decoding circuits for use in all modes as the pretrigger which marks the start of each prp.

(2) The self-test pretrigger is timed to occur 340.0 μsec after the mode 4 pretrigger (radar zero time -105.5 μsec). The self-test pretrigger is delivered to the processor for use in all modes as a reset pulse which prepares the processor to start the processing of decoded replies in each prp. Within the synchronizer, the self-test pretrigger is delivered directly to the challenge encoding circuits and display video interface circuits and indirectly (through the challenge encoding circuits) to the reply decoding circuits for use in all modes as the pretrigger which marks the start of synchronizer dead time in each prp.

(3) The sif pretrigger is timed to occur 395.2 μsec after the mode 4 pretrigger (-50.3 μsec), and is used only within the synchronizer. It is delivered to the challenge encoding circuits to initiate sif challenge encoding when the IFF set is operated in one of the sif modes. It is also delivered to the reply decoding circuits to terminate each reply decoding self-test cycle.

(4) The processor start pretrigger is timed to occur 436.0 μsec after the mode 4 pretrigger (-9.5 μsec), and is delivered to the processor for use in all modes as the pretrigger

which initiates the processing of decoded replies in each prp. Within the synchronizer, the processor start pretrigger is delivered to the challenge encoding and display video interface circuits for use in all modes as the pretrigger which marks the beginning of decoded reply processing.

c. Fault Outputs. The timing circuits supply two fault outputs to the fault indication circuits: a radar trigger fault output and a timing fault output. The radar trigger fault output is a no-fault level as long as radar triggers are present at a prf within the range from 200 to 625 radar triggers per second. If radar triggers are not supplied, or if the prf lies outside the specified range, the radar trigger fault output becomes a fault level which causes the fault indication circuits to light both the RADAR TRIG FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box. The timing fault output is a no-fault level as long as the four pretriggers (and the 10-mc clock signal which times the pretriggers) are normal. If any one or any combination of two or more of the pretriggers are not delivered, or are duplicated, or are delivered in an incorrect sequence, the timing fault output becomes a fault level, indicating a timing fault. If the radar triggers are normal, the timing fault level causes the fault indication circuits to light both the TIMING FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box. However, if radar triggers are absent, or are present at an unacceptable prf, the radar trigger fault output is a fault level, and the timing fault is not indicated: it is assumed to be the result of the radar trigger fault, rather than an actual timing circuit failure.

3-3. Challenge Encoding Circuits
(fig. 24-2)

a. Challenge Enabling. The IFF set is commanded to challenge when a challenge enable line within the control box is grounded, either manually by holding the CHALLENGE switch at ON, or automatically by an external challenge enable source within the associated radar set. In either case, the ground is delivered through the MODE SELECT switch to the synchronizer on one of four mode enable lines corresponding to the four available challenging modes: as a mode 1 enable when the MODE SELECT switch is at 1; as a mode 2 enable when the switch is at 2; as a mode 3/A enable when the switch is at 3/A; and as a mode 4 enable when the switch is at 4, TEST 4, or LOCKOUT OVERRIDE. Modes 1, 2, and 3/A are selective identification features (sif) modes employing time-coded challenge pulses and pulse-coded replies. For each of these sif modes, the challenge encoding circuits establish the timing of all challenging outputs. Mode 4 is a crypto-secure mode employing pulse-coded challenge and triple-pulse time-coded replies. For this mode, the interrogator computer performs the major challenge encoding functions, and the challenge encoding circuits in the synchronizer perform only a secondary function in delivering the interrogator computer signals as challenging outputs.

b. SIF Challenging Outputs. The challenge encoding circuits use the mode 4 pretrigger, sif pretrigger, and 10-megacycle clock from the timing circuits and the mode 1, mode 2, or mode 3/A enable from the control box to produce three outputs for delivery to the receiver-transmitter during each prp. One output is sif challenge video, normally including an interrogation side-lobe suppression (isls) pulse. The challenge video pulses are used in the receiver-transmitter as transmitter modulation pulses. Another output is an isls gate wide enough and properly timed to bracket the isls pulse. The isls gate is used in the receiver-transmitter as an RF switch drive pulse. The third output is a gain-time-control (gtc) trigger which occurs shortly before the earliest possible transponder reply pulse. The gtc trigger is used in the receiver-transmitter to initiate the receiver gate and the associated gtc action. The challenge encoding circuits also produce a transponder suppression gate, but this gate is not used.

(1) The sif challenge video (fig. 24-3, part A) normally consists of three pulses, called P1, P2, and P3 in the order of their occurrence. The spacing between the leading edges of P1 and P3 is the time-coded spacing: 3.0 μsec for a mode 1 challenge, 5.0 μsec for a mode 2 challenge, and 8.0 μsec for a mode 3/A challenge. To establish these spacings, the challenge encoding circuits reshape and delay the sif pretrigger through delay line 1A2A5, which is time shared with the reply decoding circuits. The second sif challenge video pulse (P2) is the isls pulse, and may or may not be included, depending on the level of an isls pulse inhibit input to the challenge encoding circuits from the RF switch performance monitoring (self-test) circuits within the receiver-transmitter. The purpose of that input is to prevent the gen-

eration of P2 when an RF switch fault is detected. When included, P2 is digitally timed so that its leading edge occurs 2.0 μsec after the leading edge of P1. To display IFF target information (display video) at the proper ranges in the associated radar display, P3 is generated at a fixed time (approximately 416.2 μsec after the mode 4 pretrigger), and the sif challenge time-coding is accomplished by selecting the relative timing of P1. Each sif challenge video pulse is shaped to a width of 0.77 μsec so that the transmitted RF pulse width will be 0.80 μsec. (The difference of 0.03 μsec is the amount of pulse-stretching inherent in the modulating and transmitting circuits of the receiver-transmitter.)

(2) The challenge encoding circuits deliver a digitally timed and shaped isls gate for every sif challenge, whether P2 is included in the challenge video or not. The leading edge of the isls gate is spaced 1.3 μsec after the leading edge of P1, and its width is 1.4 μsec. In the receiver-transmitter, the isls gate causes the RF switch drive circuits to switch the transmitter RF output from the antenna sum channel to the antenna difference channel and back, so that P1 and P3 are radiated in the sum channel, and P2 (when produced) is radiated in the difference channel.

(3) The sif gtc trigger is produced coincident with P3 and is delivered with a pulse width of approximately 0.6 μsec.

(4) A transponder suppression gate is produced for every challenge, but is not made available externally because there are no uses for such a gate in the present applications of the IFF set. The transponder suppression gate is started by the leading edge of the first challenge video pulse (P1 in an sif challenge) and is terminated by the leading edge of the processor start pretrigger in all modes. This is the only use of the processor start pretrigger in the challenge encoding circuits.

c. Mode 4 Challenge Outputs. When the mode 4 enable is supplied from the control box, the challenging outputs to the receiver-transmitter are controlled by the interrogator computer. The challenge encoding circuits in the synchronizer provide only the noncryptographic functions of challenge video reshaping, isls timing, and delivery of the mode 4 gtc trigger.

(1) The mode 4 enable causes the interrogator computer to respond to each reshaped mode 4 pretrigger by supplying mode 4 challenge video and a mode 4 gtc trigger. The mode 4 gtc trigger is suitable for direct delivery to the receiver-transmitter, but is supplied through the challenge encoding circuits as the gtc trigger. The mode 4 challenge video is supplied without an isls pulse and must be reshaped to the video pulse width of 0.47 μsec required for a transmitted RF pulse width of 0.5 μsec. (The difference of 0.03 μsec is the amount of pulse stretching inherent in the receiver-transmitter.)

(2) Within the synchronizer, the mode 4 enable is level shifted and inverted in the display video interface circuits and delivered as a mode 4 enable to the challenge encoding and reply decoding circuits. The mode 4 enable prepares the challenge encoding circuits to accept the mode 4 challenge video and mode 4 gtc trigger from the interrogator computer, and also enables each mode 4 pretrigger to prepare the challenge encoding circuits for digital isls timing. Then, when mode 4 challenge video begins to arrive, two actions begin: reshaping of the mode 4 challenge video for delivery to the receiver-transmitter on the challenge video line; and a pulse count to the fourth sync pulse for isls timing. The digital isls timing in mode 4 is similar to the timing in the sif modes, except that the timing begins on the leading edge of the fourth challenge video pulse (fourth sync pulse), rather than the first. With respect to that leading edge, the isls gate is started after a delay of 1.3 μsec, the mode 4 isls pulse is produced after a delay of 2.0 μsec, and the isls gate is terminated after a delay of 2.7 μsec. As in the sif modes, the mode 4 isls pulse can be inhibited by the isls pulse inhibit input from the receiver-transmitter, but the isls gate is delivered whether the isls pulse is produced or not. When not inhibited, the mode 4 isls pulse is inserted into the mode 4 challenge video to be reshaped as the fifth challenge video pulse.

(3) When the mode 4 gtc trigger arrives, it is passed directly to the receiver-transmitter on the gtc trigger line.

(4) The transponder suppression gate, as in the sif modes, is started by the leading edge of the first challenge video pulse (first sync pulse of a mode 4 challenge) and is terminated by the processor start pretrigger, but is not used in the present IFF set applications.

d. Enabling Outputs. The challenge encoding circuits supply three enable outputs to the reply decoding circuits and two to the display video interface circuits. Two of the three enables supplied to the reply decoding circuits are supplied for the decoding of sif i/p and emergency replies: reply enable 1, which is high at all times except while an sif challenge is being generated; and a mode 2, 3/A enable which is high whenever either the mode 2 enable or the mode 3/A enable is supplied (low) from the control box. The third enable supplied to the reply decoding circuits is reply enable 2, which is high throughout the reply times in each mode, and which is supplied specifically to define the mode 4 reply times during which the reply decoding circuits may deliver triple pulse decoded mode 4 replies to the processer as spoof counter video and to the interrogator computer as triple pulse decoded video. One of the two enables supplied to the display video interface circuits is an sif enable which is low whenever any one of the three sif mode enables is supplied from the control box. The other enable, sif reply enable, is formed by ANDing the sif enable with reply enable 1, and is therefore low at those times when one of the three sif mode enables is supplied from the control box and a corresponding sif challenge is not being generated.

e. Pretrigger Outputs. The challenge encoding circuits supply the reply decoding circuits with two pretrigger signals for reply decoding self-test purposes: self-test pretrigger, and reshaped self-test and sif pretriggers. The self-test pretrigger output is produced simply by inverting the self-test pretrigger input from the timing circuits. The reshaped self-test and sif pretrigger output always contains the self-test pretrigger, reshaped to a width of 0.6 μsec, whether the IFF set is challenging or not, but the sif pretrigger, also reshaped to a width of 0.6 μsec, is included only when the IFF set is challenging in one of the sif modes. The challenge encoding circuits produce this signal to delay the two pretriggers through delay line 1A2A5. The reshaped self-test pretrigger is delayed both for reply decoding self-test purposes (in all modes) and for delay line time sharing purposes (in mode 4). The reshaped sif pretrigger is delayed in each sif mode to time the P1 and P3 challenge video pulses, but would occur during reply time in mode 4, and is therefore inhibited except in the sif modes. The reply decoding circuits use only the reshaped self-test pretrigger in the reshaped self-test and sif pretriggers output.

f. Coder-Decoder Fault Output. The challenge encoding circuits include a self-test circuit which monitors the challenge encoding functions and a fault accumulator which combines the challenge encoding self-test results with the reply decoding self-test results received from the reply decoding circuits in the form of a reply decoding fault input. The output of the fault accumulator represents the performance of the challenge encoding and reply decoding circuits which are physically located in coder-decoder 1A2A2 and delay line module 1A2A5. This output is delivered to the fault indication circuits as a coder-decoder fault output which is a no-fault level as long as the self-tested circuits are functioning satisfactorily, but which becomes a fault level as soon as faults are detected in two of any three consecutive challenge-reply cycles, indicating a coder-decoder or delay line fault. If the radar triggers are normal, the fault level causes the fault indication circuits to light both the CODER DECODER FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box. However, if radar triggers are absent, or are present at an unacceptable prf, the radar trigger fault outputs from the timing circuits are fault levels which cause the radar trigger fault to be indicated and simultaneously prevent the coder-decoder fault, if any, from being indicated. The high (fault) radar trigger fault level applied to the fault indication circuits produces the radar trigger fault indication, and the low (fault) radar trigger fault level applied to the challenge encoding circuits forces a low (no-fault) coder-decoder fault level to prevent a coder-decoder fault indication.

3-4. Reply Decoding Circuits
(fig. 24-2)

a. Transponder Reply Inputs. The reply decoding circuits receive transponder replies in the form of receiver video pulses from the receiver-transmitter. Simulated replies (test target video pulses) are supplied by the display video interface circuits, but not for decoding: the test target video pulses simulate mode 4 replies that have already been decoded, and are supplied to the reply decoding circuits for de-

livery to the processor as spoof counter video in the test target mode (CHALLENGE switch on control box held at TEST). The sif and mode 4 replies from a transponder have the characteristics shown in figure 24–3, part B, and are discussed in detail in paragraphs 6–2*a* and 6–3*a*. The reply decoding circuits pulse-width discriminate and reshape the receiver video pulses for insertion into delay line 1A2A5 (time shared with the challenge encoding circuits) and for delivery as buffered receiver video, which is made available externally for possible future uses.

b. SIF Reply Decoding. When the control box supplies the challenge encoding circuits with a low mode 1 enable, mode 2 enable, or mode 3/A enable, it also supplies the reply decoding circuits with 12 code digit enables which are low and high in a combination determined by the corresponding MODE 1, MODE 2, or MODE 3/A CODE SELECT switches, and thus in a combination representing the correct reply coding for the selected challenging mode. The reply decoding circuits use delay line 1A2A5 to convert the sif replies in the receiver video from serial form to parallel form for two types of decoding: bracket decoding, and code pulse decoding.

(1) Bracket decoding detects any sif reply (and therefore all sif replies) by producing a single pulse for every pair of bracket (F1 and F2) pulses, or for any pair of receiver video pulses having the equivalent pulse width and spacing. The resulting sif bracket decoded video pulses are delivered to the display video interface circuits for use as the source of sif IFF display video pulses when a low bracket decode enable input is supplied to those circuits from the control box (SIF REPLIES switch held at ALL).

(2) Code pulse decoding detects each combination of 12 receiver video pulses and spaces which matches the combination of 12 low and high code digit enables from the control box. The results are ANDed with the corresponding bracket decoded video pulses, if any, to produce a single pulse (an sif correct code pulse) for each bracket decoded sif reply whose reply code (occupied and unoccupied code pulse positions) matches the 12 code digit enables for a period of at least 0.25 μsec. Each time such a combination of pulses is detected, the 10-mc clock input from the timing circuits is used to count out a period of 0.35 μsec. The combination of pulses is verified as a correctly coded sif reply if its code pulses match the code digit enables for any 0.25 μsec portion of the 0.35 μsec period, and an sif correct code pulse is produced for the reply. The sif correct code pulses are delivered as sif correct code video pulses to the display video interface circuits, where they serve as the source of sif IFF display video when a high bracket decode enable input is supplied to those circuits from the control box (SIF REPLIES switch left at CODED).

(3) The sif correct code pulses are also used within the reply decoding circuits to initiate a third type of sif reply decoding: i/p and emergency reply decoding, in which three inputs from the challenge encoding circuits are used. The 5-mc clock input is used for digital timing, the reply enable 1 input is used to confine i/p and emergency reply decoding to sif reply times, and the mode 2, 3/A enable input is used to enable the decoding of mode 2 or mode 3/A i/p replies. The reply decoding circuit which performs i/p and emergency reply decoding, when triggered by an sif correct code pulse, examines the interval following the F2 pulse of the correctly coded reply for the additional reply pulses which characterize i/p and emergency replies (fig. 24–3, part B). If the correctly coded reply was an i/p reply, one i/p or emergency video pulse is inserted into the sif correct code video approximately 24.65 μsec after the F2 pulse. If the reply was an emergency reply, three i/p or emergency video pulses are inserted into the sif correct code video approximately 24.65, 49.30, and 75.95 μsec, respectively, after the F2 pulse. If the reply was a normal reply, no i/p or emergency reply pulses are produced.

c. Mode 4 Reply Decoding. The reply decoding circuits perform only the noncryptographic triple pulse decoding of mode 4 replies. The cryptographic time decoding takes place in the interrogator computer. As in the sif modes, the reply decoding circuits use delay line 1A2A5 to convert mode 4 replies in the receiver video from serial to parallel form for decoding; in this case for triple pulse decoding. Each mode 4 reply which arrives during the mode 4

receiving times defined by the combination of a high reply enable 2 input from the challenge encoding circuits and a high mode 4 enable input from the display video interface circuits is triple pulse decoded to a single pulse at the time of the third reply pulse. That single pulse is then reshaped to a width of 0.5 μsec for delivery to the processor as a spoof counter video pulse and to the interrogator computer as a triple pulse decoded video pulse to be time decoded.

d. Reply Decoding Fault Output. The reply decoding circuits include a self-test circuit which performs a complete test of the reply decoding circuits during each set of pretriggers from the timing circuits, whether the IFF set is challenging or not, and delivers the results of each test in the form of a reply decoding fault output to the coder-decoder fault accumulator in the challenge encoding circuits. The mode 4 pretrigger from the timing circuits prepares for each test by reading the results of the previous test into the fault accumulator and then setting the reply decoding fault output to its fault level (low), where it will remain until the next mode 4 pretrigger, unless cleared by a complete set of satisfactory results. The self-test pretrigger from the challenge encoding circuits starts each test, during which the reshaped self-test pretrigger in the reshaped self-test and sif pretrigger input from the challenge encoding circuits is selected and used to stimulate both a mode 4 reply and a correctly coded sif reply. Then, if both simulated replies are properly decoded, the responses of the reply decoding circuits to the delayed reshaped self-test pretrigger (inserted into delay line 1A2A5 by the challenge encoding circuits) are counted to check the delay line continuity to every reply decoding tap, and also to check for proper responses to incorrectly coded sif replies. If all responses are satisfactory, the last response switches the reply decoding fault output to its no-fault level (high); if not, that output remains at its fault level (low). The sif pretrigger from the timing circuits then ends the test, leaving the reply decoding fault output at its no-fault or fault level to be read into the coder-decoder fault accumulator when the next mode 4 pretrigger arrives to prepare for another test.

3-5. Display Video Interface Circuits
(fig. 24-2)

a. General. The display video interface circuits accept the decoded replies in each mode, deliver them to the processor as decoded reply video to be processed for display decisions, and then select those decoded reply pulses which are to be displayed, rejecting those which are not to be displayed. The decoded reply pulses selected for display are then reshaped and delivered to the associated radar set on the IFF display video line either as target present pulses with a width of 1.0 μsec or as friend (tail or eyelash) pulses with a width of 5.0 μsec, depending on the mode of operation, the processor decisions, and whether or not the processor decisions are bypassed.

b. SIF Display Video.

(1) In the sif modes, the sif reply enable input from the challenge encoding circuits enables the display video interface circuits to accept both the sif bracket decoded video and the sif correct code video from the reply decoding circuits for delivery to the processor as decoded reply video. One or both of those video inputs is also applied to a digital delay circuit (a shift register shifted at the rate of the 5-mc clock input from the challenge encoding circuits) to serve as the source of target video from which pulses will subsequently be selected by the processor decisions and be reshaped for delivery as IFF display video pulses. The target video to be delayed is determined by the setting of the SIF REPLIES switch on the control box. When that switch is held at ALL, the bracket decode enable input to the display video interface circuits is low, causing the sif bracket decoded video produced for all received sif replies to be included in the selection. When the SIF REPLIES switch is left at CODED, the bracket decode enable input is high, and only the sif correct code video representing correctly coded sif replies is included in the selection.

(2) When the PROCESSOR switch on the control box is at IN, the processor bypass enable input to the display video interface circuits is high, enabling the target input from the processor to control the selection until the self-test gate input from the processor goes low. The friend threshold and friend inputs from the processor are not used in the sif modes. From the time of the processor start pretrigger until the self-test

gate input goes low, each 4 μsec segment of the target input represents a display decision for the corresponding increment of range, called a range box. The target input is low during each range box in which decoded reply video pulses have occurred consistently enough for the processor to decide that they represent an actual transponder (IFF target) within that range segment. Accordingly, each digitally delayed target video pulse corresponding to a low target input level is selected, reshaped, and delivered as an IFF display video pulse, but each delayed target video pulse corresponding to a high target input level is rejected. The strobe pulse input from the processor is used to retime the target levels, which are wide enough but slightly too early for proper IFF display video selection.

(3) When the PROCESSOR switch on the control box is at BYPASS, the processor bypass enable input is low, and the target input is not used; instead, every delayed target video pulse is reshaped for delivery as an IFF display video pulse.

(4) Pulses selected for inclusion in the IFF display video on the basis of low target inputs alone, or by a low processor bypass enable input, are reshaped to the target present pulse width of 1.0 μsec. Therefore, in the sif modes the IFF display video consists only of target present pulses; it never includes friend (tail or eyelash) pulses.

c. Mode 4 Display Video.

(1) In mode 4, the low mode 4 enable input enables the display video interface circuits to accept mode 4 time decoded video from the interrogator computer for delivery to the processor as decoded reply video and for digital delay as the target video from which pulses will subsequently be selected by the processor decisions and be reshaped for delivery as IFF display video pulses.

(2) When the PROCESSOR switch on the control box is at IN, the processor bypass enable input to the display video interface circuits is high, enabling the target, friend threshold, and friend inputs from the processor to control the selection until the self-test gate input from the processor goes low. From the time of the processor start pretrigger until the self-test gate input goes low, the combination of target, friend threshold, and friend input levels during each 4 μsec increment of range (range box) represents the display decision for that range box. The target input, as in the sif modes, is low during each range box in which the processor has decided that an IFF target is present. The friend threshold and friend inputs represent a more stringent requirement: both remain high during each range box until the processor has decided not only that there is an IFF target present in the range box, but also that the IFF target is a friend; then the friend threshold input goes low, and one prp later the friend input goes low. The friend input is then low during that range box in each subsequent prp until the IFF target has ceased to reply. Accordingly, the mode 4 target video selection is carried out as follows:

(*a*) Each digitally delayed target video pulse corresponding to a low target input level is selected for reshaping and delivery as an IFF display video pulse, but each delayed target video pulse corresponding to a high target input is rejected. Whether the selected delayed target video pulse will be reshaped to the friend pulse width of 5.0 μsec or to the target present pulse width of 1.0 μsec depends on the accompanying friend threshold and friend input levels.

(*b*) If the friend threshold and friend input levels are both high, the selected delayed target video pulse is reshaped to the target present pulse width of 1.0 μsec. If the friend threshold input level is low and the friend input level is high, the selected delayed target video pulse is reshaped to the friend pulse width of 5.0 μsec.

(3) When the PROCESSOR switch on the control box is at BYPASS, the processor bypass enable input is low, and the target, friend threshold, and friend inputs are not used; instead, every delayed target video pulse is reshaped and delivered at the target present pulse width of 1.0 μsec.

d. Test Target Video. The display video interface circuits include a test target generator which can simulate a pattern of decoded mode 4 friend replies to test the mode 4 time decoded video path through the display video interface circuits and the ability of the processor to process mode 4 replies in each of its active range boxes. The test target generator, when enabled by a low test target enable input from the control box (CHALLENGE switch held at TEST), delivers the simulated decoded mode 4 friend replies as test target video pulses, which are inserted into the mode 4 time decoded video path within the display video interface circuits, and which are also delivered to the processor as spoof counter video pulses through the reply decoding circuits. One complete pattern of test target video pulses simulates a mode 4 friend in each of the processor's active range boxes, and the patterns are repeated for as long as the CHALLENGE switch is held at TEST. The resulting IFF display video pulses, when displayed at the associated radar indicator, produce a spiraling pattern of simulated mode 4 friends so spaced in range and azimuth that the processing in each individual range box can be evaluated separately.

e. Interface Fault Output. The display video interface circuits include a self-test circuit which monitors the passage of decoded replies through the display video interface circuits. The results of the monitoring performed during successive challenge-reply cycles are read into a fault accumulator by successive self-test pretriggers from the timing circuits. The output of the fault accumulator is delivered to the fault indication circuits as an interface fault output which is a no-fault level as long as the monitored circuits are functioning satisfactorily, but which becomes a fault level as soon as faults are detected in two of any three consecutive challenge-reply cycles, indicating an interface fault. If the radar triggers are normal, the fault level causes the fault indication circuits to light both the INTERFACE FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box. However, if radar triggers are absent, or are present at an unacceptable prf, the radar trigger fault output from the timing circuits is a fault level which causes the fault indication circuits to indicate the radar trigger fault, and which simultaneously prevents those circuits from indicating an interface fault, if any. Interface fault indications are also prevented when the CHALLENGE switch on the control box is at OFF, because no signals pass through the display video interface circuits to produce valid interface fault outputs unless the IFF set is challenging (CHALLENGE switch held at ON) or operating in the test target mode (CHALLENGE switch held at TEST). The display video interface circuits sense the OFF position and force the interface fault output to a low (no-fault) level by ORing three enable inputs which are simultaneously high only when the CHALLENGE switch is at OFF. Two of these represent the ON position: the sif enable input from the challenge encoding circuits, which is low whenever the CHALLENGE switch is at ON with the MODE SELECT switch at 1, 2, or 3/A; and the mode 4 enable input from the control box, which is low whenever the CHALLENGE switch is at ON with the MODE SELECT switch at any of its other three positions. The third input is the test target enable input from the control box, which is low whenever the CHALLENGE switch is at TEST.

3–6. Fault Indication Circuits

(fig. 24–2)

The fault indication circuits receive four fault inputs which represent the operational status of the other synchronizer circuits and provide corresponding visual status indications, both locally on the front panel and remotely on the control box. As long as the associated radar set is supplying radar triggers at an acceptable prf, the radar trigger fault input from the timing circuits is a no-fault level (low), and the other three fault inputs are accepted as valid indications of the operational status of the corresponding modules. In this case, if any one or combination of those three inputs are fault levels (high), the fault indication circuits light the corresponding combination of FAULT lamps on the front panel and supply a low (grounded) synchronizer fault indicator enable to the control box to light the red SYN SELF TEST lamp and prevent the green CHALLENGE lamp from lighting. If, instead, the radar trigger fault input is a fault level (high), then the other three fault inputs are not accepted as valid. In this case, the fault indication circuits light the RADAR TRIG FAULT lamp on the front panel and ground the synchronizer fault indicator enable output, but they do not light any of the other three FAULT lamps on the front panel, regardless of the corresponding fault input levels.

3–7. Power Supply and Power Distribution Circuits

(fig. 24–2)

The IFF set receives its power input (28 volts dc,

negative-ground) from the associated radar set and distributes the power as +28 volts to all parts of the IFF set through the power control panel. Within the synchronizer, the power supply and power distribution circuits filter the +28-volt input in filter 1A2A6 and deliver it through POWER circuit breaker 1A2CB1 as lamp voltage for the five lamps on the synchronizer front panel and as the power input to power supply module 1A2A3. The power supply module produces the +12-volt, +5-volt, and −12-volt operating voltages required in the other synchronizer circuits. For power supply monitoring and troubleshooting, each of the operating voltages can be checked from the front panel, where voltage selector switch 1A2S1 delivers each voltage through appropriate multipliers on component board 1A2A7 to meter 1A2M1 for a go/no-go (green band) indication.

CHAPTER 4

TIMING CIRCUIT FUNCTIONING

4–1. General

This chapter presents a logic diagram discussion of the timing circuits, based on the timing circuit logic shown in figure 24–4. The timing circuits are physically composed of all parts within timing module 1A2A4 and some of the parts within interface module 1A2A1. These circuits accept each radar trigger from the associated radar set and respond by producing a set of four digitally timed pretriggers: a mode 4 pretrigger, a self-test pretrigger, an sif pretrigger, and a processor start pretrigger. The pretriggers are produced as negative-going pulses 0.2 μsec wide by circuits within the timing module. The parts of the timing circuits located within the interface module provide only buffering functions: the amplitude limiting and reshaping of incoming radar triggers, and the buffering and inverting of outgoing pretriggers, including the reshaping of the mode 4 pretrigger for delivery to the interrogator computer. The distribution of the pretriggers has already been described (para 3–2*b*). Self-test circuits within the timing module monitor the radar triggers and the pretriggers produced after each radar trigger to supply the fault indication circuits with two status outputs which are normally no-fault levels: a radar trigger fault output, and a timing fault output. If the associated radar set fails to supply radar triggers, or if the radar trigger prf is outside the acceptable range (200 to 625 radar triggers per second), the radar trigger fault output is switched to its fault level to declare a radar trigger fault. If any of the four pretriggers are not produced, of if they are produced in an incorrect sequence, or if more than four are produced, the timing fault output is switched to its fault level to declare a timing fault, unless the radar trigger fault output is also a fault level. A radar trigger fault takes precedence over a timing fault, and if both a radar trigger fault and a timing fault are detected, only the radar trigger fault is declared.

4–2. Pretrigger Generation
(fig. 24–4)

a. The digital timing of the four pretriggers takes place partly on 10-mc clock and counter A card 1A2A4A1 and partly on counter B card 1A2A4A2. A continuous train of 10-mc clock pulses is generated on 1A2A4A1 to be counted in a 13-stage pretrigger timing counter after each radar trigger. The 13 counter stages are divided between 1A2A4A1 and 1A2A4A2, and their outputs are decoded by four gates (two on 1A2A4A1 and two on 1A2A4A2) to produce the four pretriggers at the count values which result in proper pretrigger timing. The pretrigger timing counter is controlled from 1A2A4A1, where counter control flip-flop A2B starts a count after each radar trigger, and then stops and resets the counter after a full count (8,192) has been reached.

b. Before each radar trigger arrives, the counter control flip-flop on 1A2A4A1 is in its set state, holding all 13 stages of the pretrigger timing counter reset and disabled through reset inverters A1A and A1B. When a radar trigger arrives, it is amplitude limited and reshaped on buffer circuit 2 card 1A2A1A7 for delivery to the timing module as a positive-going reshaped radar trigger with a width of approximately 0.4 μsec. This trigger is inverted on 1A2A4A2 and passed to 1A2A4A1, where it resets counter control flip-flop A2B. With A2B reset, the high reset outputs from inverters A1A and A1B enable the pretrigger timing counter to count the 10-mc clock pulses from inverter A4A.

c. The mode 4 pretrigger is produced on 1A2A4A1 by AND A7B, A8 when the count reaches 142 (14.2 μsec after the start of the count). At that count, all 12 inputs to AND A7B, A8 are high for 0.2 μsec, resulting in a negative-going mode 4 pretrigger output 0.2 μsec wide. After buffering and reshaping on buffer circuit 2 card 1A2A1A7 for delivery to the interrogator computer, the mode 4 pretrigger has a width of approximately 3.0 μsec and a delay, measured from the leading edge of the incoming radar trigger, of 14.5 μsec.

d. The self-test, sif, and processor start pretriggers are produced in a similar manner by the other three decode gates. The self-test pretrigger is produced on 1A2A4A2 by AND A7B, A3 when the count reaches 3542 (354.2 μsec after the start of the count, or 340.0 μsec after the leading edge of the reshaped mode 4 pretrigger). The sif pretrigger is produced on 1A2A4A2 by AND A7A, A2 when the

count reaches 4094 (395.2 μsec after the leading edge of the reshaped mode 4 pretrigger). The processor start pretrigger is produced on 1A2A4A1 by AND A7A, A9 when the count reaches 4502 (436.0 μsec after the leading edge of the reshaped mode 4 pretrigger).

e. After the processor start pretrigger is produced, the count continues until it reaches 8,192 and overflows. At that point, the negative-going edge of the Q output from the thirteenth stage (2^{12}) returns to 1A2A4A1 and clocks counter control flip-flop A2B into its set state to reset and disable the pretrigger timing counter until the next radar trigger arrives and starts another count as in *b*, above.

4–3. Timing Self-Test
(fig. 24–4)

a. The timing self-test circuits check for the presence, proper sequence, and proper number of pretriggers as well as for the presence and proper prf of the radar triggers. If any of the pretriggers are missing, if they occur in the wrong sequence, or if there are any extra pretriggers, a timing fault is declared. If the radar triggers are absent, or if the radar trigger prf is too high or too low, a radar trigger fault is declared.

b. The sequence of the four pretriggers is checked on timing self-test card 1A2A4A3 by a four flip-flop ripple-reset circuit. Each reshaped radar trigger starts a ripple reset by resetting flip-flop A5A, whose low Q output then resets flip-flop A5B, which resets flip-flop A1A, which resets flip-flop A1B. All four flip-flops are then in the fault states, and one of the inputs to three-input OR A4A is low (fault). Normally (under no-fault conditions), the mode 4 pretrigger arrives first and sets flip-flop A5A to its no-fault state. The high Q output A5A then enables A5B to be set to its no-fault state by the self-test pretrigger. The high Q output of A5B then enables A1A to be set to its no-fault state by the sif pretrigger. The high Q output of A1A then enables A1B to be set to its no-fault state by the processor start pretrigger. This removes the low (fault) input from OR A4A. The sequence checking circuit remains in this state until the next radar trigger arrives and starts another ripple reset in anticipation of the next set of pretriggers.

c. If any of the pretriggers fails to arrive, or arrives out of sequence, or is duplicated, a fault condition is detected. *For example*, if the self-test pretrigger fails to arrive, or if it arrives before the mode 4 pretrigger or after the sif pretrigger, or if two self-test pretriggers arrive, flip-flop A5B is not in its set (no-fault) state when the sif pretrigger arrives, and the sif pretrigger is then unable to set flip-flop A1A. As a result, the processor start pretrigger is then unable to set flip-flop A1B, and the low (fault) input to OR A4A remains.

d. The pretriggers are also counted in two pairs by flip-flops A6A and A6B. These flip-flops are reset to their no-fault states by each reshaped radar trigger, and are then alternately set to fault and reset to no-fault by the pairs of pretriggers which they count. Flip-flop A6A counts the mode 4 pretrigger and the processor start pretrigger applied through OR A7D, and flip-flop A6B counts the self-test pretrigger and the sif pretrigger applied through OR A7B. If either flip-flop receives an odd number of pretriggers, its count ends with the flip-flop in the set (fault) state, delivering a low (fault) output to OR A4A.

e. Thus, if the sequence or count checks detect a fault, one of the inputs to OR A4A is low, and the high OR output (fault) enables timing fault flip-flop A8A to be clocked into its set (fault) state by the trailing edge of the radar trigger short gate from the radar trigger test circuit (para 4–4). If all inputs to OR A4A are high (no-fault), the low OR output enables A8A either to remain reset (no-fault) or to be clocked reset by the trailing edge of the radar trigger short gate.

4–4. Radar Trigger Test
(fig. 24–4)

a. Timing self-test card 1A2A4A3 also contains a radar trigger test circuit which monitors the reshaped radar triggers and declares a radar trigger fault if the interval between those triggers lies outside the acceptable range from 1600 to 5000 μsec. The circuit makes use of the infinite retriggerability of short gate (1600 μsec) single-shot A2 and long gate (5000 μsec) single-shot A3 to control radar trigger fault flip-flop A8B. Both single-shots are triggered by the trailing edges of successive radar triggers, if present. Acceptable radar trigger intervals are longer than the active state duration of A2, but shorter than that of A3, with the result that A2 is able to return to its quiescent state between reshaped radar triggers, but A3 is not. Thus, at the time of each reshaped radar trigger, the $\overline{Y}$ output of A2 and the Y output of A3 are normally both high at AND A4C,

allowing the reshaped radar trigger to reach radar trigger fault flip-flop A8B as a set (no-fault) input. Each positive-going trailing edge of the $\overline{Y}$ output of A2 occurs after all four pretriggers have been produced, and is therefore conveniently timed for a reading of the pretrigger test results. Accordingly, the $\overline{Y}$ output of A2 is applied to the clock input of timing fault flip-flop A8A.

b. In the event of a radar trigger fault, the interval between reshaped radar triggers is either so long that A3 can return to its quiescent state, or so short that A2 is held continuously in its active state. If A3 reaches its quiescent state, its low Y output forces A8B into the reset (fault) state to declare the radar trigger fault and prevents AND A4C from passing another reshaped radar trigger to clear the declared fault. If, instead, the interval is so short that A2 cannot reach its quiescent state, its high Y and low $\overline{Y}$ outputs at the time of each reshaped radar trigger steer the reshaped radar trigger through AND A7C to clock A8B reset, rather than through AND A4C to force A8B set, thereby declaring the radar trigger fault.

CHAPTER 5

CHALLENGE ENCODING CIRCUIT FUNCTIONING

Section I. BLOCK DIAGRAM DESCRIPTION

5-1. General

The challenge encoding circuits generate sif challenge video pulses and gtc triggers when operating in any one of the sif modes and process mode 4 challenge video pulses and gtc triggers supplied by the interrogator computer when operating in mode 4. An isls gate is generated for each sif and mode 4 challenge.

5-2. Generation of SIF Challenge Video (fig. 24-5)

a. Each sif challenge consists of three pulses (fig. 24-3, part A): two interrogation pulses designated P1 and P3 whose leading-edge-to-leading-edge spacing is 3.0 μsec for a mode 1 challenge, 5.0 μsec for a mode 2 challenge and 8.0 μsec for a mode 3/A challenge; and an interrogation sidelobe suppression (isls) pulse designated P2, whose leading edge is spaced 2.0 μsec after the leading edge of P1. All three pulses have the same nominal duration of 0.77 μsec, so that with a slight stretching inherent in the receiver-transmitter the transmitted RF challenge pulses are 0.8 μsec wide. With respect to radar zero range time, which is the governing time reference, the timing of P3 is fixed: P1 and P2 are shifted to obtain the proper challenge pulse spacing for each sif mode. The sif challenges are generated far enough ahead of radar zero range time to ensure that each transponder reply, when received, decoded, processed, and finally delivered to the associated radar set for display as an IFF video pulse, will appear at the proper display range. Associated signals generated with the sif challenge video are an isls gate (RF switch drive pulse) timed to bracket the isls pulse, a gtc trigger just before the first pulse of the earliest possible reply (zero-range reply), and a suppression gate which begins at the leading edge of the first challenge video pulse and ends at the processor start pretrigger.

b. The sif enable generation circuit (fig. 24-5) generates an sif enable level whenever any one of the sif mode enables (mode 1, 2, or 3/A enable) is supplied from the control box. This level enables the pretrigger reshaping, delay line time sharing, and isls timing circuits during sif operation. The sif and self-test pretrigger inputs to the pretrigger reshaping circuit are combined, reshaped to 0.6 μsec, and applied to the delay line and delay line drive circuit. The delay line and delay line drive circuit is time shared by the challenge encoding and reply decoding circuits in response to appropriate enable gates (a challenge enable gate for challenging, and reply enable 2 for decoding) from the delay line time sharing circuit.

c. The reshaped self-test and sif pretriggers are amplified and delayed for separate purposes. Every self-test pretrigger is inserted into the delay line, whether challenging or not, and the resulting delayed outputs are used for self-test purposes (para 5-4). The sif pretrigger, approximately 55 μsec later, is inserted into the delay line only when challenging in one of the sif modes, and the resulting delayed outputs are applied to the P1 and P3 trigger generation circuit.

d. The four inputs to the P1 and P3 trigger generation circuit represent the sif pretrigger at four values of delay. The buffered 13.05 μsec, buffered 15.95 μsec, and $\overline{18.0\ \mu sec}$ inputs are used to generate the P1 trigger for the selected mode. The $\overline{18.0\ \mu sec}$ input, enabled by the mode 1 enable, is the P1 trigger for each mode 1 challenge; the buffered 15.95 μsec input, enabled by the mode 2 enable, is the P1 trigger for each mode 2 challenge; and the buffered 13.05 μsec input, enabled by the mode 3/A enable, is the P1 trigger for each mode 3/A challenge. The $\overline{21.0\ \mu sec}$ input is the P3 trigger for all sif modes.

e. The $\overline{P1}$ and $\overline{P3\ trigger}$ outputs of the P1 and P3 trigger generation circuit are applied to the challenge video shaping circuit. The P1 trigger is also applied to the isls timing circuit, where it is used to time the generation of the $\overline{sif\ isls\ (P2)\ trigger}$ and the $\overline{isls\ gate}$. The P3 trigger is also applied to the delay line time sharing circuit, where it is used to end challenge encoding time and initiate reply decoding time.

f. The P1, P2, and P3 triggers are reshaped and combined in the challenge video shaping circuit to produce the three-pulse sif challenge video for the receiver-transmitter. The P3 trigger is also delivered as the sif gtc trigger for the receiver-transmitter. In addition, the leading edge of the P1 trigger starts the suppression gate, which is later terminated by the processor start pretrigger. The suppression gate is not used in this equipment. It is intended to be used as an inhibiting gate for a nearby ground transponder during transmission of challenges.

5-3. Generation of Mode 4 Challenges
(fig. 24-5)

a. Each mode 4 challenge (fig. 24-3, part A) consists of four sync pulses, an isls pulse, and a coded challenge word containing a combination of 21 to 32 challenge and anti-interference interrogation (AII) pulses. The basic pulse spacing is 2.0 μsec from leading edge to leading edge, with the AII pulse positions interlaced between the challenge pulse positions positions. All pulses are reshaped to the same nominal duration of 0.47 μsec, so that with a slight stretching inherent in the receiver-transmitter the transmitted RF challenge pulses are 0.5 μsec wide. Like sif challenges, mode 4 challenges are generated far enough ahead of radar zero range time to ensure that each transponder reply, when received, decoded, processed, and finally delivered to the associated radar set for display as an IFF video pulse, will appear at the proper display range.

b. Operation in mode 4 is initiated (fig. 24-5) when a mode 4 enable level is applied to the interrogator computer and to the mode 4 enable and sync counting circuit from the control box. Approximately 14.5 μsec after the radar trigger, a reshaped mode 4 pretrigger is applied to the interrogator computer, which then starts a challenge encoding cycle. At the end of the encoding cycle, approximately 168 μsec after the reshaped mode 4 pretrigger, the interrogator computer begins to supply mode 4 challenge video and, approximately 205 μsec later still, a mode 4 gtc trigger. Within the synchronizer, these signals are passed through the mode 4 enable and sync counting circuit to the challenge video shaping circuit.

c. A pulse corresponding to the fourth sync pulse of the mode 4 challenge video (mode 4 fourth sync pulse) is generated by the sync counting circuit. This pulse is applied to the isls timing circuit, where it is used to time the generation of the mode 4 isls trigger and the isls gate.

d. The mode 4 challenge video and mode 4 isls trigger are combined and reshaped by the challenge video shaping circuit and applied to the receiver-transmitter. The mode 4 gtc trigger, which occurs shortly before the earliest possible mode 4 reply pulse, is also applied to the receiver-transmitter. The leading edge of the first mode 4 challenge video pulse starts the suppression gate, which is later terminated by the processor start pretrigger.

5-4. Chalienge Encoding Self-Test
(fig. 24-5)

a. The challenge encoding self-test circuit monitors various signals generated by the challenge encoding circuits and supplies an sif fault, mode 4 fault, or excess pulse fault output to the fault accumulator circuit if a fault is detected. A self-test cycle takes place after every mode 4 pretrigger when challenging. When not challenging, the challenge encoding self-test results are forced to "no-fault".

b. When the mode 4 pretrigger arrives, it places the self-test circuits in a fault state which is cleared if, and only if, all monitored signals are normal. If the fault state is not cleared, a corresponding fault output is supplied to the fault accumulator circuit. The fault accumulator circuit supplies a coder-decoder module fault output which is normally a no-fault level, but which becomes a fault level as soon as faults have been detected in two of any three consecutive self-test cycles, and then remains a fault level until the next self-test cycle in which no fault is detected. The fault level lights the CODER-DECODER FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box.

Section II. LOGIC DIAGRAM DESCRIPTION

5-5. Sif Enable Generation Circuit
(fig. 24-6, zone A-2)

To challenge in one of the sif modes, the corresponding mode enable is grounded (made low) at the control box, and in the sif enable generation circuit the low mode enable produces a high output from the inverting level shifter for that mode. The level shifted mode enable is applied to the

P1 and P3 trigger generation circuit (para 5–9) as an individual enable, but is applied to the isls timing circuit and other portions of the synchronizer as an sif enable. If the sif mode is mode 2 or mode 3/A, the enable is also applied to the i/p and emergency code circuit of the reply decoding circuits as a mode 2, 3/A enable.

5–6. Pretrigger Reshaping Circuit

(fig. 24–6, zone C–5)

During sif operation, the sif pretrigger on challenge video card 1A2A2A5 is enabled by the high sif enable level and applied as one input to OR A6C, A9D. The other input to OR A6C, A9D is the self-test pretrigger. The self-test and sif pretrigger output of the OR is reshaped to 0.6 μsec by single-shot A1 and applied to the delay line drive circuit (para 5–8). During mode 4 operation, the sif pretrigger is not enabled. However, the self-test pretrigger is reshaped as during sif operation and used for self-test purposes.

5–7. Delay Line Time Sharing Circuit

(fig. 24–6, zone B–9)

a. The delay line time sharing circuit generates two gates which establish the challenge and reply decoding times of the synchronizer. The challenge time is initiated by the mode 4 pretrigger (14.5 μsec after receipt of a radar trigger) during both sif and mode operation (fig. 24–7, part A). In the sif modes challenge time is terminated by the P3 trigger (last pulse of an sif challenge). In mode 4, challenge time is terminated 21 μsec after the self-test pretrigger to allow for decoding of early mode 4 replies. Termination of challenge time initiates reply decoding time.

b. The mode 4 pretrigger on reply video card 1A2A2A6 resets flip-flop A4B and sets flip-flop A4A. The reset state of flip-flop A4B corresponds to challenge time, and its set state corresponds to reply decoding time. In sif operation, A4B remains in the reset (challenge) state until arrival of a P3 trigger, which sets it to the reply decoding state. In mode 4 operation, the self-test pretrigger resets flip-flop A4A, which enables AND A6B to pass the buffered 21 μsec pulse (21 μsec after the self-test pretrigger). The buffered 21 μsec pulse sets flip-flop A4A (thereby disabling AND A6B) and is enabled through AND A7D to set flip-flop A4B to the reply decoding state. The reply enable 2 and challenge enable gates are applied to the delay line and delay line drive circuit.

5–8. Delay Line and Delay Line Drive Circuit

(fig. 24–6, zone B–11)

The delay line and delay line drive circuits are time-shared between the challenge encoding and reply decoding circuits. During reply decoding time, buffered receiver video pulses from the receiver video reshaping circuit (para 6–5) are amplified by the delay line driver and applied to the delay line. The outputs from various selected delay line taps are used for decoding purposes. During sif challenge time, the reshaped self-test and sif pretriggers are amplified and applied to the delay line. The outputs of the delay line resulting from the self-test pretrigger are used for the reply decoding self-test cycles. The delay line outputs, resulting from the sif pretrigger, are used to generate the P1 and P3 sif challenge video pulses (para 5–9) in the selected mode. The duration of reply decoding time and challenge encoding time is estabished by the reply enable 2 and challenge enable gates supplied by the delay line time sharing circuit (para 5–7).

a. Delay Line Driver

(1) *Challenge encoding.* During sif challenge time, the challenge enable gate on reply video card 1A2A2A6 is high, and the reshaped self-test and sif pretriggers are enabled through AND A3C, OR A2B, and driver Q2 to the 0.00 μsec tap of delay line 1A2A5. The output of driver 1A2A2A6Q2 is a negative-going 15-volt pulse (one per pretrigger) with a duration of 0.6 μsec and a risetime of 15 nanoseconds.

(2) *Reply decoding.* During reply decoding time, the reply enable 2 gate is high, and the buffered receiver video pulses are enabled through AND A3B, OR A2B, and driver Q2 to the 0.00 μsec tap of the delay line module. The buffered receiver video output of AND A3B is also made available externally through low level line driver 1A2A1A6Q1 for possible future uses.

b. Delay Line. Delay line 1A2A5 is a 21-μsec lumped-constant delay line tapped for 17 specific values of delay required in the challenge encoding and reply decoding circuits. The connections made to obtain these values of delay, together with the 0.00 μsec delay line input, provide a total of 18 delay line output signals, and thus make each delay line input pulse available at 18 different times:

first at 0.00 μsec (undelayed), then at each of the 16 tap connections in succession, and finally at the 21.0 μsec delay line output. The 18 delay line outputs are used in three specific combinations corresponding to the groups of delay values required for sif challenge encoding, sif reply decoding, and mode 4 triple pulse reply decoding. The group of delay values required for sif reply decoding is the largest group: 0.00 μsec and 13 multiples of 1.45 μsec (1.45 to 8.7 μsec and 11.6 to 20.3 μsec), corresponding to the relative positions of the bracket pulses and code pulses (fig. 24–3, part B) in sif replies. The values of delay required for sif challenge encoding are 13.05, 15.95, 18.0, and 21.0 μsec, where 13.05 and 15.95 μsec are used as though they were 13.0 and 16.0 μsec respectively. The values required for mode 4 triple-pulse decoding are 0.0, 1.8, and 3.6 μsec, corresponding to the relative positions of the three pulses in each mode 4 reply (fig. 24–3, part B). A 10.15 μsec tap is availble, but is not used in the present design.

5–9. P1 and P3 Trigger Generation Circuit

(fig. 24–6, zone C–18)

a. Timing triggers for the P1 and P3 pulses of each sif challenge are produced by the P1 and P3 trigger generation circuit. Initially, on coder card 1A2A2A4, the enabled sif pretrigger input resets flip-flop A4B, whose high $\overline{Q}$ output enables AND's A8C and A12B. The 13.05, 15.95, 18.0, and 21.0 μsec delay line signals represent the sif pretrigger at the corresponding four values of delay. When challenging in an sif mode, one of the mode enable inputs from the sif enable generation circuit is high, and the corresponding AND (A13A, A13B or A13C) is enabled.

b. When challenging in mode 1, the 18.0 μsec delay line signal is enabled through AND A13B (mode 1 P1). In a like manner, the buffered 15.95 and buffered 13.05 μsec delay line inputs are enabled through AND's A13A and A13C, respectively, when challenging in mode 2 or mode 3/A. The selected sif P1 trigger is gated through AND A12B and eventually becomes the P1 pulse of the sif challenge.

c. The 21.0 μsec delay line output is the sif P3 trigger for all sif modes and is gated through AND A8C to eventually become the P3 pulse of the sif challenge. The trailing edge of the sif P3 trigger also sets flip-flop A4B, thereby disabling AND's A8C and A12B.

5–10. Isls Timing and Generation Circuit

(fig. 24–6, zone A–31)

a. The isls trigger and isls gate (RF switch drive pulse) for each challenge are generated in the isls timing circuit and are controlled by the leading edge of the P1 trigger in each sif mode or by the leading edge of the fourth sync pulse in mode 4. The sif isls (P2) trigger becomes the P2 pulse of an sif challenge and is transmitted by the receiver-transmitter in the difference channel. Likewise, the mode 4 isls trigger is inserted in the empty isls pulse position of the mode 4 challenge video and transmitted in the difference channel.

b. During sif operation, on coder card 1A2A2A4, the sif enable level from the sif enable generation circuit is high, and sif isls trigger generator AND A10 is enabled if the isls pulse inhibit input from the receiver-transmitter is low (isls pulse not being inhibited). Similarly, during mode 4 operation, the mode 4 enable level is high, and mode 4 isls trigger generator AND A14 is enabled if the isls pulse is not being inhibited.

c. An sif P1 trigger or mode 4 fourth sync pulse resets counter control flip-flop A15A, which enables the isls timing counter to count 10-mc clock pulses. When a count of 13 is reached (1.2 to 1.3 μsec after the leading edge of the P1 trigger or mode 4 fourth sync pulse), AND A2 is enabled, and the fourteenth clock pulse then produces a low A2 output which sets flip-flop A3A to start the isls gate. When a count of 19 (1.8 to 1.9 μsec) is reached, either AND A10 or AND A14 (depending on the mode of operation) is enabled, and the twentieth clock pulse then produces a low A10 or A14 output (isls trigger). Finally, when a count of 27 (2.6 to 2.7 μsec) is reached, AND A6 is enabled, and the twenty-eighth clock pulse then produces a low A6 output which resets flip-flop A3A thereby terminating the isls gate and clearing the isls counter by setting counter control flip-flop A15A.

d. As shown in figure 24–7, part C, the isls gate brackets the corresponding isls trigger, so that when the isls gate switches the receiver-transmitter RF switch to the difference channel, the isls pulse portion of an sif or more 4 challenge is transmitted in the difference channel. If a fault should occur in the receiver-transmitter RF switch, its performance monitoring (self-test) circuit ungrounds the isls pulse inhibit line to inhibit the generation of isls triggers. However, the isls gate is not inhibited and can be used for troubleshooting the RF switch.

5–11. Mode 4 Enable and Sync Counting Circuit

(fig. 24–6, zone A–27)

The mode 4 enable and sync counting circuit counts

out the fourth sync pulse of the mode 4 challenge video. The fourth sync pulse is used in the generation of the mode 4 isls gate and isls pulse. During mode 4 operation, on challenge video card 1A2A2A5, the mode 4 enable input to AND A13D is high. When the mode 4 pretrigger arrives, it sets OR flip-flop A3A, A3D, thereby enabling synchronous counter A4A, A4B. When the mode challenge video arrives, beginning approximately 168 μsec after the mode 4 pretrigger, the counter proceeds to count. The trailing edge of the third sync pulse brings the count to 3, which allows the fourth sync pulse to pass through AND A2C. The counter is then reset and disabled when the isls gate rests OR flip-flop A3A, A3D approximately 1.4 μsec later.

5–12. Challenge Video Shaping Circuit
(fig. 24–6, zone A–21)

a. Sif Video Shaping. During sif operation, on challenge video card 1A2A2A5, the sif P1 trigger and sif P3 trigger (representing the sif pretrigger at two values of delay) are combined in OR A7B and reshaped to a nominal pulse duration of 0.77 μsec by single-shot A8. The sif isls (P2) trigger is reshaped to a nominal pulse duration of 0.77 μsec by single-shot A11 and combined with the reshaped $\overline{P1}$ and $\overline{P3}$ pulses in OR A2B to make up the three-pulse sif challenge video. The duration of the $\overline{P1}$ and $\overline{P3}$ pulses is controlled by potentiometer R3, and the duration of the $\overline{P2}$ pulse is controlled by potentiometer R2. Since the earliest possible sif reply pulse would occur shortly after the last pulse of an sif challenge ($\overline{P3}$), the sif P3 trigger is also used as the sif gtc trigger.

b. Mode 4 Video Shaping. During mode 4 operation, the mode 4 isls trigger is inserted in the unoccupied isls pulse position of the mode 4 challenge video in OR A3C. Each pulse of the composite mode 4 challenge video is then reshaped to a nominal duration of 0.47 μsec by single-shot A5. The active state duration of the single-shot, and hence the duration of the mode 4 challenge video pulses is controlled by potentiometer R1. The mode 4 gtc trigger is supplied by the interrogator computer at a time shortly before the earliest possible mode 4 transponder reply pulse (373 μsec after the mode 4 pretrigger, or 72.5 μsec before radar zero range time).

5–13. Challenge Self-Test Circuit
(fig. 24–6, zone A–38)

The challenge self-test circuit checks the challenge video, isls gate, and gtc trigger outputs of the challenge encoding circuits during every prp while the IFF set is challenging. At the end of each prp, the test results are read (shifted) into the fault accumulator (para 5–14) by the mode 4 pretrigger, which then prepares the challenge self-test circuit to perform a new challenge test (self-test cycle) during the next prp. The challenge tests are sif challenge tests when the sif enable is high, or are mode 4 challenge tests when the mode 4 enable is high. When the sif and mode 4 enables are both low (IFF set not challenging), challenge tests are not performed, and the challenge self-test circuit supplies continuous no-fault outputs to the fault accumulator.

a. Sif Challenge Test

(1) During each prp when the sif enable is high, the challenge self-test circuit tests for: one, and only one, P1 challenge video pulse after the self-test pretrigger; one, and only one, isls gate after the P1 challenge video pulse; a P2 challenge video pulse (isls pulse) within the isls gate if, and only if, the isls pulse inhibit input is low (isls pulse not being inhibited); a gtc trigger after the isls gate; and one, and only one, P3 challenge video pulse, concurrent with the gtc trigger.

(2) On coder-decoder self-test card 1A2A2A8, the trailing edge of the mode 4 pretrigger prepares for a self-test cycle by setting flip-flop A5B, which sets OR flip-flop A1A, A4A to its no-fault state, resets flip-flop A17A to its no-fault state, and resets flip-flop A5A to its fault state. The resetting of flip-flop A5A starts a ripple reset action which resets flip-flops A13A, A13B and A17B to their fault states (fig. 24–7, part D). If there is no fault present, the self-test cycle will end with all flip-flops except A17A in their no-fault states. (Flip-flop A17A is used only during mode 4 challenge tests.) If one of the sif challenge signals is missing or out of sequence, the self-test cycle will end with one or more of the flip-flops in the fault state, and a fault level will be supplied to the fault accumulator.

(3) Assuming a no-fault condition, the self-test pretrigger arrives approximately 337 μsec after the trailing edge of the mode 4 pretrigger and resets flip-flop A5B. This removes the set input from OR flip-flop

A1A, A4A and the reset input from flip-flop A5A. OR flip-flop A1A, A4A can now be reset to the fault state by an excess pulse fault (challenge signals which should not occur). Approximately 68 to 73 μsec later, depending on the sif mode of operation, the P1 trigger and the P1 challenge video pulse arrive, and the trailing edge of their coincidence at AND A16C sets flip-flop A5A to the no-fault state which, in turn, removes the reset from flip-flop A13A. In addition, A5A enables AND A1B, so that if there should be a second P1 trigger and a corresponding second P1 challenge video pulse, their coincidence will reset OR flip-flop A1A, A4A to the fault state (excess pulse fault).

(4) The isls gate arrives approximately 1.3 μsec after the P1 trigger and is ANDed with the P2 challenge video pulse and the isls pulse inhibit input separately and together. If the isls pulse is not being inhibited (isls pulse inhibit input low), the trailing edge of coincidence between P2 and the isls gate in AND A12B sets flip-flop A13 to its no-fault state which, in turn, removes the reset from flip-flop A13B. If the isls pulse is being inhibited (isls pulse inhibit input high), the trailing edge of the isls gate itself, at AND A9B, sets flip-flop A13A to the no-fault state. If the isls timing circuit fails to inhibit the isls pulse when the isls pulse inhibit input is high, the coincidence at AND A8B will act through OR A8C and AND A1B to reset OR flip-flop A1A, A4A to the fault state. In addition, A13A enables AND A9C, so that if there should be duplicate isls gates when the isls pulse is or is not being inhibited, OR flip-flop A1A, A4A will be reset to the fault state through AND A9C.

(5) The next events are the concurrent gtc trigger and P3 pulse. The leading edge of the gtc trigger sets flip-flop A13B to the no-fault state, which removes the reset from flip-flop A17B, and then, finally, the trailing edge of the P3 pulse sets flip-flop A17B to the no-fault state to end the sif challenge self-test cycle. If any of the incoming sif challenge signals did not set its associated flip-flop, flip-flop A17B would remain in the reset (fault) state, delivering a high $\overline{Q}$ output to AND A1C. The output of A1C (sif fault) is applied to the fault accumulator circuit (para 5-14). If there are any extra challenge video pulses following the P3 pulse they will reset OR flip-flop A1A, A4A to the fault state through AND A9D. The test results are read into the fault accumulator by the next mode 4 pretrigger, just before that pretrigger starts another self-test cycle.

b. Mode 4 Challenge Test

(1) During each prp when the mode 4 enable is high, the challenge self-test circuit tests for: one and only one, fourth sync pulse counted out of the mode 4 challenge video from the interrogator computer; a challenge video pulse coincident with the fourth sync pulse; one, and only one, isls gate occurring after the fourth sync pulse and before the first challenge or AII pulse: an isls pulse within the isls gate if, and only if, the isls pulse inhibit input is low; and a gtc trigger if a mode 4 gtc trigger is supplied by the interrogator computer.

(2) On coder-decoder self-test card 1A2A2A8, the trailing edge of the mode 4 pretrigger sets flip-flop A5B to prepare for a self-test cycle in the same way as described in paragraph 5-13*a*(2). If there is no-fault present, the self-test cycle will end with all flip-flops in their no-fault states. If one of the signals is missing, the self-test cycle will end with one or more of the flip-flops in the fault state, and a fault level will be supplied to the fault accumulator (para 5-14), unless one of the signals supplied by the interrogator computer is abnormal or missing, in which case a coder-decoder fault is not declared because the fault is probably in the interrogator computer. However, if the fault is an excess pulse fault, then a coder-decoder fault is declared whether or not the interrogator computer signals are normal.

(3) The self-test action is started by the mode 4 challenge video pulses from the interrogator computer and the corresponding challenge video pulses reshaped by the challenge video shaping circuit. The first pulse of the mode 4 challenge video arrives approximately 168 μsec after the leading edge of the mode 4 pretrigger (fig. 24-7,

part E), and its trailing edge resets flip-flop A5B. This removes the set input from OR flip-flop A1A, A4A and the reset input from flip-flops A5A and A17A. The OR flip-flop can now be reset to the fault state should an excess pulse fault be detected during the self-test cycle. If the interrogator computer fails to supply mode 4 challenge video, flip-flop A5B remains in the set state and a self-test cycle is not started. However, for the remainder of this discussion, it is assumed that the interrogator computer is operating normally.

(4) The fourth sync pulse, counted out of the mode 4 challenge video by the mode 4 enable and sync counting circuit, arrives approximately 6 μsec after the leading edge of the first mode 4 challenge video pulse. If the sync counting circuit is operating properly, the fourth sync pulse is coincident with the fourth challenge video pulse at AND A16C, and the output of A16C sets flip-flop A5A to the no-fault state, thereby removing the reset from flip-flop A13A. In addition, A5A enables AND A1B, so that if there should be an extra "fourth sync pulse" during the time that challenge video is present, the extra coincidence at AND A16C will reset OR flip-flop A1A, A4A to the fault state (excess pulse fault).

(5) The isls gate arrives 1.3 μsec after the leading edge of the fourth sync pulse and is ANDed with the challenge video pulses and the isls pulse inhibit input separately and together. If the isls pulse is not being inhibited (isls pulse inhibit input low), the trailing edge of coincidence between the isls gate and the isls pulse at AND A12C sets flip-flop A13A to the no-fault state which, in turn, removes the reset from flip-flop A13B. If the isls pulse is being inhibited, AND A9B is enabled and the trailing edge of the isls gate itself sets flip-flop A13A to the no-fault state. If the isls timing circuit fails to inhibit the isls pulse when the isls pulse inhibit input is high, the coincidence at AND A8B will act through OR A8C and AND A1B to reset OR flip-flop A1A, A4A to the fault state. In addition, A13A enables AND A9C, so that if there should be duplicate isls gates when the isls pulse is or is not being inhibited, the OR flip-flop will be reset to the fault state through AND A9C.

(6) The $\overline{\text{isls gate}}$ is also ANDed with the mode 4 challenge video from the interrogator computer to check that the sync counting circuit has indeed counted out the fourth sync pulse, rather than one of the first three. Normally, the output of AND A12C remains high, because the $\overline{\text{isls gate}}$ is timed to coincide with the unoccupied isls pulse position in the mode 4 challenge video. However, if a fault causes the sync counting circuit to count out a pulse other than the fourth sync pulse, the isls gate will occur at an occupied pulse position, and the coincidence at AND A12C will act through OR A8C and AND A1B to reset OR flip-flop A1A, A4A to the fault state.

(7) The next and final event is the arrival of the mode 4 gtc trigger from the interrogator computer and the $\overline{\text{gtc trigger}}$ output from the challenge video shaping circuit. The challenge self-test circuit must declare a mode 4 fault if there was a fault detected during the tests described above and/or a $\overline{\text{gtc trigger}}$ is not delivered in response to a mode 4 gtc trigger. If no faults have been detected, the leading edge of the $\overline{\text{gtc trigger}}$ sets flip-flop A13B, whose low $\overline{\text{Q}}$ output insures a high (no-fault) $\overline{\text{mode 4 fault}}$ output from AND A1D to the fault accumulator. The trailing edge of the mode 4 gtc trigger sets flip-flop A17A, but this has no effect on the $\overline{\text{mode 4 fault}}$ output with flip-flop A13B set. However, if A13B is still in its reset (fault) state, either because its R input is low as a result of an incomplete sequence of earlier actions or because a $\overline{\text{gtc trigger}}$ output has not arrived, then the high Q output of flip-flop A17A produces a low $\overline{\text{mode 4 fault}}$ output from AND A1D to the fault accumulator.

5–14. Fault Accumulator (Coder-Decoder)

(fig. 24–6, zone A–42)

The coder-decoder fault accumulator supplies the fault indication circuits (ch. 8) with a coder-decoder fault output representing the combined results of the challenge encoding self-test cycles described in the preceding paragraphs and of the reply decoding self-test cycles described in chapter 6. A challenge

encoding self-test cycle and a reply decoding self-test cycle both take place after each mode 4 pretrigger, and the combined results are read (shifted) into the fault accumulator by the next mode 4 pretrigger, so that each mode 4 pretrigger can be considered as marking the end of one combined self-test cycle and the beginning of the next. The coder-decoder fault output is normally (no fault), and remains low even if an occasional fault is detected, but goes high (fault) as soon as faults are detected in two of any three consecutive combined self-test cycles. When high, the coder-decoder fault output remains high until a self-test cycle occurs in which no faults are detected.

a. No-Fault Condition. On coder-decoder self-test card 1A2A2A8, the challenge encoding and reply decoding self-test results are combined in OR A4B and shifted through the two-stage shift register composed of flip-flops A3A and A3B. When every self-test cycle ends with no-fault results, each mode 4 pretrigger shifts a reset state (low J, high K) into A3A and simultaneously shifts a set state (high J, low K) into A3B. These are the no-fault states of the two flip-flops, which then supply two low inputs to AND A2C, A2D for a low (no-fault) coder-decoder fault output. That output remains low even if an occasional self-test cycle produces a fault result, provided that such self-test cycles are each preceded and followed by at least two cycles producing no-fault results, because both flip-flops must be in their fault states simultaneously for a high (fault) output. The occasional fault result is shifted into A3A by one mode 4 pretrigger, then out of A3A into A3B by the next mode 4 pretrigger, and finally out of A3B by the next mode 4 pretrigger, so that the flip-flops are in their fault states one at a time, rather than simultaneously. Thus, in any three consecutive self-test cycles, if any two or all three produce no-fault results, the coder-decoder fault output is low (no-fault).

b. Continuous Fault Condition. When every self-test cycle ends with a fault result, each mode 4 pretrigger shifts a set state (high J, low K) into flip-flop A3A and a reset state (low J, high K) into flip-flop A3B. These are the fault states, which result in two high inputs to AND A2C, A2D for a high (fault) coder-decoder fault output. Thus, in any three consecutive self-test cycles, if two in succession produce fault results, a high (fault) coder-decoder fault output is obtained. That output remains high until the first self-test cycle occurs which produces a no-fault result. The mode 4 pretrigger at the end of such a no-fault cycle shifts the no-fault result into A3A, which then supplies a low input to AND A2C, A2D and thereby cancels the high (fault) output.

c. Alternating Fault and No-Fault Condition. When the results produced by successive self-test cycles are alternately fault and no-fault results, flip-flop A3A alternates between its fault and no-fault states on successive mode 4 pretriggers, but AND A2B prevents a similar alternation of flip-flop A3B to insure a high (fault) coder-decoder output each time A3A is in its fault state. The AND takes effect when such a sequence has placed A3B in the fault state and A3A in the no-fault state, with OR A4B delivering a fault result at the time of a mode 4 pretrigger. The mode 4 pretrigger shifts the fault result into A3A, but is unable to shift the no-fault state of A3A into A3B because of the low R input to A3B supplied by AND A2B. In effect, A3B is "stalled" in the fault state by the incoming fault result. Thus, in any three consecutive self-test cycles, if any two or all three produce fault results, a high (fault) coder-decoder fault output is obtained.

CHAPTER 6

REPLY DECODING CIRCUIT FUNCTIONING

Section I. BLOCK DIAGRAM DESCRIPTION

6-1. General

The reply decoding circuits completely decode sif transponder replies, but perform only the noncryptographic triple-pulse decoding of mode 4 replies. During sif operation, the reply decoding circuits supply sif correct code video and bracket decoded video to the display video interface circuits (ch. 7). During mode 4 operation, the reply decoding circuits supply triple pulse decoded video to the interrogator computer for time decoding and to the processor for spoof counting. The reply decoding circuits also make buffered receiver video available externally for possible future uses.

6-2. Decoding of Sif Replies
(fig. 24-8)

a. Types of Replies. The sif normal, i/p (identification of position), and emergency replies generated by a transponder are shown in figure 24-3, part B. The basic pulse duration (the width of each pulse in any reply) is nominally 0.45 μsec.

(1) *Normal replies.* Each normal reply consists of two bracket pulses, designated F1 and F2, whose leading edges are 20.3 μsec apart, and up to 12 code pulses located between the bracket pulses with their leading edges spaced at whole multiples of 1.45 μsec from the leading edges of the bracket pulses. The code pulse designations are based on the four-digit octal code used to communicate assigned reply codes to pilots for their transponder settings, and to IFF set operators for their CODE SELECT switch settings at the control box. The four digits of the octal code (designated A, B, C, D, from left to right) each apply to three particular code pulses, which are distinguished by numerical values (1, 2, 4) as though they were the "1's" of a three-bit binary number (the octal number). The octal code thus specifies which code pulses should be present, and which should not, in a correctly coded reply. The A, B, C, and D pulses which should be present are those whose numerical values added up to the A, B, C, and D octal digits, respectively. As an example, for a reply code communicated as 3456, a correctly coded normal reply would contain A1 and A2 (because A = 3), B4 (because B = 4), C1 and C4 (because C = 5), D2 and D4 (because D = 6), the two bracket pulses and no other pulses. Mode 1 normal replies are limited to five code pulses (A1, A2, A4, B1, and B2), and although the mode 1 reply codes may be communicated in four-digit octal form, only the first two digits (A and B) are significant. Mode 2 and 3/A normal replies can contain all 12 code pulses, and all four octal digits are significant. Each normal reply, when decoded, results in single pulse to be processed and delivered to the associated radar for display.

(2) *I/p replies.* Each mode 1 i/p reply consists of two normal mode 1 replies in succession, with a spacing of 24.65 μsec between the leading edges of their corresponding pulses. Each mode 2 or mode 3/A i/p reply consists of a normal mode 2 or mode 3/A reply followed by a special position identification (spi) pulse whose leading edge is spaced 4.35 μsec from the leading edge of the F2 pulse. Each i/p reply, when decoded, results in two pulses for processing and display: one for the normal portion of the i/p reply and the second at a display range approximately 3.7 kilometers (km) greater (nominally 24.65 μsec later). Although both pulses of a decoded i/p reply are processed, the associated radar set will not necessarily display the second pulse.

(3) *Emergency replies.* Each mode 1 or mode 2 emergency reply consists of a normal mode 1 or mode 2 reply followed by three sets of bracket pulses with a spacing of 4.35 μsec between the leading edges of each F2 pulse and the subsequent F1 pulse. Mode 3/A

emergency replies are similar to mode 1 and mode 2 emergency replies, except that the code pulses between the first pair of bracket pulses represent the fixed code 7700 (A1, A2, A4, B1, B2, and B4). Each emergency reply, when decoded, results in four pulses for processing and display: one for the normal portion of the emergency reply, and the remaining three at successive display ranges approximately 3.7, 7.4 and 11.1 greater (nominally 24.65, 49.30, and 73.95 μsec later). Although all four pulses of a decoded emergency reply are processed, the associated radar set will not necessarily display the second, third, and fourth pulses.

b. Multiple-Coincidence Decoding.

(1) During sif reply time, receiver video from the receiver-transmitter is pulse width discriminated and reshaped by the receiver video reshaping circuit (para 6–5) to produce buffered receiver video, which is applied to the delay line and delay line drive circuit (para 5–8), and which is also made available externally for possible future uses. In the delay line and delay line drive circuit, the buffered receiver video is ANDed with reply enable 2, whose leading edge corresponds to the trailing edge of the last sif challenge pulse, from the delay line time sharing circuit (para 5–7). The enabled buffered receiver video is amplified, applied to the delay line 0.00 μsec input, and returned to the sif decoding circuits at 14 values of delay: 0.00 μsec and 13 multiples of 1.45 μsec, corresponding to the relative timing of the bracket pulses and the 12 code pulse positions in a normal sif reply.

(2) The 12 code pulse delay line outputs and the corresponding 12 code digit enables from the control box are applied to the code pulse decoding circuit (para 6–6) in two groups: one group for the eight code pulse positions from C1 to D1, and the second group for the four code pulse positions from B2 to D4. This division into two groups is not a functional necessity: it represents the physical division of the sif reply decoding circuits between two printed wiring cards. The two bracket pulses, 0.00 μsec (F2) and 20.3 μsec (F1), are applied to the bracket decoding circuit (para 6–7). During the decoding self-test cycle, the code digit enable inputs to the code pulse decoding circuit are overridden by simulated code 7777 (reshaped self-test pretrigger) and simulated code 0000 (code override), supplied by the reply decoding self test circuit. The matching values of delay make it possible for the bracket and code pulses of each reply, which are received serially (one pulse at a time), to act in parallel (all pulses simultaneously) at the moment when the entire reply is properly positioned in the delay line, with the last pulse (F2) just entering the delay line at the 0.00 μsec input tap while the first pulse (F1) is passing the 20.3 μsec output tap and each code pulse contained in the reply is passing its respective intermediate output tap. The parallel action at that instant results in a decoded reply output from the correct code pulse generation circuit (para 6–9), called an sif correct code pulse, if the combination of code pulses corresponds to the control box CODE SELECT switch settings (all expected code pulses present, and none present that are not expected). For example, when challenging in mode 2 with the MODE 2 CODE SELECT switches on the control box set for code 1030 (A = 1, B = 0, C = 3, and D = 0) the normal replies received from transponders whose corresponding mode 2 code select switches are also set for code 1030 would be correctly coded normal replies, and each would consist of five pulses: F1, C1, A1, C2, and F2, in that order. With the code digit enables for code 1030 applied by the control box MODE 2 CODE SELECT switches, the decoding circuits expect simultaneous code pulses at the 18.85 μsec (C1), 17.4 μsec (A1), and 15.95 μsec (C2) delay line outputs, and produce a correct code pulse whenever those code pulses, and no others, are present while the F2 pulse is at the 0.00 μsec delay line input and the F1 pulse is at the 20.3 μsec output. Each correctly coded (1030) normal reply, when received, would then reach the sif reply decoding circuits at all 14 values of delay: first with the F1 at 0.00 μsec, before any of the other pulses are received; then, 1.45 μsec later, with F1 at 1.45 μsec while C1 is at 0.00 μsec; then, another 1.45 μsec later, with F1 at 2.9 μsec and C1 at 1.45 μsec while A1 is at 0.00 μsec; and so on, until F1 is at 20.3 μsec, C1 at

18.85, A1 at 17.4, C2 at 15.95, and F2 at 0.00 μsec. At that point, all pulses are present where expected, and none are present where not expected, and the decoding circuits accordingly produce an sif correct code pulse. The condition in which all expected pulses are present is called "go," and the condition in which any pulse is present where not expected is called "kill."

(3) The F1 and F2 bracket pulses, which are always present in each normal sif reply, and which occur four times in each emergency reply, are decoded separately. The 0.00-μsec (F2) and 20.3-μsec (F1) delay line outputs are ANDed in the bracket decoding circuit (para 6–7) and whenever two pulses are simultaneously present in those delay line outputs a negative-going bracket decoded video pulse (bracket go) is produced. The bracket go pulse is applied to the correct code generation circuits (para 6–9) and to the i/p and emergency decoding circuit (para 6–10) as a bracket decoded video pulse. Bracket decoded video is also supplied to the display video interface circuits for use as the source of IFF display video when a bracket decode enable level is supplied to the display interface circuits by the control box (SIF REPLIES switch held at ALL).

(4) The sif correct code pulse output of the correct code pulse generation circuit is applied to the i/p and emergency decoding circuit, where it initiates a check of the corresponding reply. The reply is recognized as an i/p or emergency reply if an additional pulse is detected 4.35 μsec after the leading edge of the F2 bracket pulse. After recognizing an i/p or emergency reply, the i/p and emergency decoding circuits complete their decoding cycle and supply one i/p video pulse or three emergency video pulses to the correct code pulse generation circuit. The i/p or emergency video pulses are combined with the sif correct code pulse to generate sif correct code video, which is supplied to the display video interface circuits for processing.

6–3. Decoding of Mode 4 Replies
(fig. 24–8)

a. Each mode 4 reply from a transponder (fig. 24–3, part B) is a group of three pulses occurring in one of 16 possible time coding positions. The proper time coding position (time slot) for the mode 4 replies to each mode 4 challenge is determined by the interrogator computer when it encodes the challenge, and only friendly mode 4 transponders are able to decode the challenge and transmit their replies in the proper time slots. Regardless of the time slot, the three pulses of each mode 4 reply are spaced at intervals of 1.8 μsec, leading edge to leading edge, and the duration of each pulse is nominally 0.45 μsec.

b. The mode 4 reply video from the receiver-transmitter is pulse width discriminated, reshaped, and applied to the delay line 0.00 μsec input in the same way as sif reply video. The buffered 0.00 μsec input to the delay line and the 1.8 μsec and 3.6 μsec delay line outputs are applied to the triple pulse decoding circuit (para 6–8) together with the mode 4 enable from the display video interface circuits. The three delay line signals are ANDed and, if the reshaped receiver video input to the delay line was a true mode 4 reply (three 0.45-μsec pulses spaced 1.8 μsec apart), the third pulse of the undelayed 0.00 μsec input will be coincident with the second pulse of the 1.8 μsec delayed input and the first pulse of the 3.6 μsec delayed input. If this condition exists, and the equipment is operating in mode 4 (mode 4 enable high), a single 0.5 μsec triple pulse decoded video pulse is supplied to the interrogator computer for time decoding.

c. The triple pulse decoded video pulse is also ORed with test target video supplied by the test target generator circuit (para 7–14) during the test target mode of operation (CHALLENGE switch on control box held to TEST). The resultant triple pulse decoded/test target video (spoof counter video) is supplied to the processor where it is used in conjunction with the corresponding decoded reply video pulse (para 7–8), to reach a friend decision.

6–4. Reply Decoding Self-Test

The decoding self-test circuit (para 6–11) simulates sif and mode 4 reply inputs to the reply decoding circuits, monitors the responses to those inputs, and supplies a low reply decoding fault output to the fault accumulator (para 5–14) if a fault is detected. A reply decoding self-test cycle is started by each self-test pretrigger, after the mode 4 pretrigger has placed the decoding self-test circuit in the fault state, and is ended by the next sif pretrigger. The fault state is cleared if, and only if, all monitored signals are normal. If the fault state is not cleared, a corresponding fault state is shifted into the fault accumulator by the next mode 4 pretrigger.

Section II. LOGIC DIAGRAM DESCRIPTION

6-5. Receiver Video Reshaping Circuit
(fig. 24-9, zone A-3)

a. The receiver video reshaping circuit receives raw receiver video pulses from the receiver-transmitter and adjusts their amplitude so that all input pulses with an amplitude of less than three volts are discarded. Also, the receiver video pulses are pulse-width discriminated to remove all pulses having a duration of less than 0.25 μsec (noise spikes). The result is buffered receiver video pulses which have been delayed by 0.25 μsec and stripped clean of noise content.

b. On reply video card 1A2A2A6, the raw receiver video pulses are applied to video amplifier Q1 at an input amplitude determined by the setting of video level adjust potentiometer R6. The input amplitude is adjusted so that only actual reply pulses are delivered to the pulse width discriminator with sufficient amplitude (low) to pass through the integrated circuit elements in the pulse width discriminator. The output of Q1 is delivered to AND A3A, A3D through two paths: an undelayed path through OR A6A, and a delayed path through 0.25 μsec delay line DL1. If the duration of each pulse is greater than 0.25 μsec, coincidence will occur at the input of AND A3A, A3D, whose input is returned to its input through OR A6A to maintain the coincidence until the end of the delayed pulse. Pulses less than 0.25 μsec wide are discarded, because by the time such a pulse reaches the delayed input of the AND, the undelayed pulse has ended, and coincidence does not occur.

c. The output of AND A3A, A3D also triggers retriggerable single-shot A5, whose active state output (buffered receiver video) is applied to the delay line and delay line drive circuit (para 5-8). The delay line and delay line drive circuit is time shared (para 5-7) between the reply decoding and challenge encoding circuits. Buffered receiver video is also made available externally for possible future uses, and test purposes.

6-6. Code Pulse Decoding Circuit
(fig. 24-9, zone D-14)

a. The sif reply pulses are decoded by the code pulses decoding circuit, which contains 12 identical code pulse detectors, one per code pulse, and four output decoding gates. The 12 code pulse delay line outputs are compared with their respective code digit enables to detect matching combinations (correct codes) as they occur in the reshaped receiver video. Each comparison of a delay line output with a code digit enable takes place in the associated code pulse detector circuit, which delivers two outputs, "go" and "$\overline{\text{kill}}$." These outputs are both simultaneously high when, and only when, a correct code condition exists (during the width of each pulse, when a pulse is expected; or during the clear period between pulses, when a pulse is not expected). For the simultaneously high go and $\overline{\text{kill}}$ outputs when a pulse is expected, the $\overline{\text{kill}}$ output is held high by the code digit enable, and each pulse in the delay line output is delivered as a positive-going (high) go pulse. For the simultaneously high go and $\overline{\text{kill}}$ outputs when a pulse is not expected the go output is held high by the code digit enable, and the absence of pulses in the delay line output is required to keep the $\overline{\text{kill}}$ output high. If a pulse is present, it is delivered as a negative-going (from high) $\overline{\text{kill}}$ pulse, indicating an incorrect code. Since all 12 code pulse detection circuits are identical, only one, the C1 code pulse detector, will be discussed.

b. On correct code 1 card 1A2A2A2, when the $\overline{18.85\ \mu\text{sec}}$ (C1) pulse is expected, the C1 enable is high, disabling AND A5C (code override is also high at this time) and maintaining a high $\overline{\text{C1 kill}}$ output to C1-D1 kill OR 1A2A2A2A6. Until the expected $\overline{18.85\ \mu\text{sec}}$ pulse arrives, the C1 go input to C1-D1 go AND 1A2A2A2A7 is low, disabling the gate and inhibiting the decoding of the reply. When the $\overline{18.85\ \mu\text{sec}}$ (C1) pulse is not expected, the C1 enable is low, and the C1 go input to the C1-D1 go AND is held high. With the C1 enable low, one input to AND 1A2A2A2A5C is high, but the gate is disabled by the absence of an $\overline{18.85\ \mu\text{sec}}$ pulse, thereby maintaining a high $\overline{\text{C1 kill}}$ input to the C1-D1 kill OR. However, if an $\overline{18.85\ \mu\text{sec}}$ pulse should be present when not expected, the $\overline{\text{C1}}$ kill input to the C1-D1 kill OR is low, making the C1-D1 kill output high and thereby inhibiting the decoding of the reply. The $\overline{\text{C1-D1 go}}$ output, the B2-D4 go output of AND, 1A2A2A3A8A, the C1-D1 kill output, and the B2-D4 kill output of OR 1A2A2A3A8B are applied to the correct code pulse generation circuit (para 6-9) for further decoding.

c. During each reply decoding self-test cycle, two conditions are simulated. First, the reshaped self-test pretrigger is simultaneously applied to the 12 code pulse detectors to simulate reply code 7777

(all code pulses present). This checks the go circuits for proper C1–D1 go and B2–D4 go outputs to the correct code pulse generation circuit, where the kill outputs are overridden. The correct code pulse generation circuit responds by producing an sif correct code video pulse and a bracket decoded video pulse for the reply decoding self-test circuit. Second, a code override gate simulates a control box CODE SELECT switch setting of 0000 (no code pulses expected). This checks the kill circuits for proper C1–D1 kill and B2–D4 kill outputs. The reply decoding self-test circuit is described in paragraph 6–11.

6–7. Bracket Decoding Circuit

(fig. 24–9, zone D–19)

a. The F1 and F2 pulses, which must always be present in each normal reply, and which occur four times in each emergency reply, are decoded separately from the code pulses by the bracket decoding circuit on correct code 2 card 1A2A2A3. The 0.00 μsec (F2) and 20.3 μsec (F1) delay line signals are buffered (inverted) and applied to AND A9C. If pulses are simultaneously present at those delay line taps, AND A9C delivers a low output for the duration of coincidence. This output is inverted by inverter A9D and delivered both to AND A5A, A11A as bracket go and to the i/p and emergency decoding circuit (para 6–10) as undelayed bracket decoded video. At AND A5A, A11A the bracket go pulse is ANDed with the C1–D1 and B2–D4 go outputs of the code pulse decoding circuit (para 6–6). In the i/p and emergency decoding circuit the undelayed bracket decoded video is used to decode emergency replies.

b. The bracket decoded video pulse from AND A9C is also delayed by 0.25 μsec through delay line DL1 for delivery to the display video interface circuits (chapter 7) as sif bracket decoded video. The 0.25 μsec delay matches the pulse width discriminator delay in the sif correct code video (para 6–9) so that the timing of the sif bracket decoded video at the display video interface circuits is nominally the same as the timing of the sif correct code video. During each reply decoding self-test cycle, the reshaped self-test pretrigger is applied to both inputs of AND A9C to check its ability to produce a bracket decoded video pulse.

6–8. Triple Pulse Decoding Circuit

(fig. 24–9, zone B–6)

a. During mode 4 operation, mode 4 replies are decoded by the triple pulse decoding circuits on reply video card 1A2A2A6. Each mode 4 reply consists of three 0.45 μsec pulses spaced 1.8 μsec apart. The three delay line inputs to AND A6C represent a triple pulse mode 4 reply at three values of delay: 0.00 μsec, 1.8 μsec, and 3.6 μsec. If the reply is a true mode 4 reply, the third pulse of the 0.00 μsec input will be coincident with the second pulse of the 1.8-μsec input and the first pulse of the 3.6-μsec input (fig. 24–10, part A). The resultant single pulse output of AND A6C is reshaped to 0.5 μsec by single-shot A1. If the mode 4 enable input is high and if reply enable 2 from the delay line time sharing circuit (para 5–7) is high, a triple pulse decoded video pulse is applied to the interrogator computer for time decoding.

b. The triple pulse decoded video is also ORed with the test target video from the test target generator of the display video interface circuits (para 7–14) during the test target mode of operation obtained when the control box CHALLENGE switch is held at TEST. The resultant triple pulse decoded/test target video (spoof counter video) is inverted and delivered to the processor. During each reply decoding self-test cycle, the ability of the triple pulse decoding circuit to produce triple pulse decoded video is checked by applying the reshaped self-test pretrigger to all three inputs of AND A6B.

6–9. Correct Code Pulse Generation Circuit

(fig. 24–9, zone A–20)

The correct code pulse generation circuit generates an sif correct code video pulse for each sif normal reply if four conditions are met: all expected code pulses present (B2–D4 and C1–D1 go); no pulses present that are not expected (neither a B2–D4 kill nor a C1–D1 kill); bracket pulses present (bracket go); and the above conditions present for more than 0.25 μsec.

a. Correct Code Go. On correct code 2 card 1A2A2A3, the B2–D4 go and C1–D1 go inputs from the code pulse decoding circuit (para 6–6) are applied to AND A5A, A11A together with bracket go from the bracket decoding circuit (para 6–7). With all three go inputs simultaneously high, AND A5A, produces a low output (all-go) which clocks flip-flop A2B set. Flip-flops A2B, A1A and A1B, together with AND A5B, constitute a digital single-shot with an active state duration of 0.3 μsec. The Y output (A2B–Q) of the digital single-shot, reshaped all-go, is applied to correct code AND A5C.

b. Correct Code Kill. The B2–D4 kill and C1–D1 kill inputs from the code pulse decoding circuit are applied through kill override ANDs A11D and A11C, respectively, to correct code AND A5C. The kill override ANDs inhibit erroneous kill inputs during each reply decoding self-test cycle (para 6–11). With the reshaped all go B2–D4 kill, and C1–D1 kill inputs to AND A5C all simultaneously high, a low gate output, all-go, no-kill, is applied to the pulse width discriminator circuit. If the reshaped all-go input to AND A5C is low, one or more of the expected code pulses or one or both of the bracket pulses are missing and AND A5C is disabled. Likewise, if either the B2–D4 kill or the C1–D1 kill input to AND A5C is low, at least one or more unexpected pulse is present, and again the gate is disabled.

c. Pulse Width Discrimination and Output.

(1) The duration of the all-go, no-kill output of AND A5C, which must be more than 0.25 μsec, is checked by a 0.25-μsec pulse width discriminator circuit similar to the one described for the receiver video reshaping circuit (para 6–5). The all-go, no-kill pulse is applied to the inputs of AND A3C through two paths: an undelayed path through OR A3D, and a delayed path through 0.25-μsec delay line DL2. If the all-go, no-kill pulse is wider than 0.25 μsec, the undelayed input to AND A3C overlaps the delayed input. The overlap starts a negative-going sif correct code pulse at the output of A3C which is returned to its input through OR A3D, thereby maintaining the sif correct code pulse for the duration of the delayed all-go, no-kill pulse. The sif correct code pulse output of AND A3C, representing the all-go, no-kill condition and stripped clean of all pulses narrower than 0.25 μsec, is supplied to the i/p and emergency decoding circuit.

(2) In the i/p emergency decoding circuit, the sif correct code pulse initiates a check on the corresponding reply, which is recognized as an i/p or emergency reply if an additional pulse is detected 4.35 μsec after the leading edge of the F2 bracket pulse. After an i/p emergency reply is recognized, decoding is completed and the resultant i/p or emergency video is returned to the correct code pulse generation circuit.

(3) The sif correct code pulse is ORed with the i/p or emergency video pulse(s) to produce sif correct code video, which is supplied to the target video selection circuit (para 7–7) of the display video interface circuits.

6–10. I/p and Emergency Decoding Circuit
(fig. 24–9, zone A–28)

The i/p and emergency decoding circuit generates an i/p video pulse or three emergency video pulses if a transponder reply is recognized as an i/p or emergency reply. Sif i/p and emergency replies are multiple replies equivalent to normal replies followed by one or more additional pulses (fig. 24–3, part B), beginning 4.35 μsec after the leading edge of the F2 pulse of the normal portion. The corresponding decoded i/p or emergency reply pulses are also multiple: two pulses for each i/p reply, consisting of the normal sif correct code pulse for the normal portion of the i/p reply followed by an i/p correct code pulse nominally 24.65 μsec later; and four pulses for each emergency reply, consisting of the normal sif correct code pulse for the normal portion of the emergency reply followed by three emergency correct code pulses at intervals of 24.65 μsec (nominally 24.65, 49.30, and 73.95 μsec after the leading edge of the normal correct code video pulse). The normal sif correct code pulse is generated by the correct code pulse generation circuit described in paragraph 6–9.

a. The i/p and emergency decoding circuit, when triggered by a normal sif correct code pulse from the correct code pulse generation circuit, recognizes and decodes each i/p or emergency reply as follows (fig. 24–10, part B):

(1) The normal sif correct code pulse initiates a short wait (short count) which ends just less than 4.35 μsec after the F2 pulse.

(2) At the end of the short count, a check is made for an additional reply pulse spaced 4.35 μsec from the leading edge of the F2 pulse. If such a pulse is found, the reply is recognized as an i/p or emergency reply; if not, the i/p or emergency reply decoding cycle ends.

(3) When a pulse is found 4.35 μsec after the leading edge of the F2 pulse, it is either another F1 pulse (emergency reply or mode

1 i/p reply) or an spi pulse (mode 2 or mode 3/A i/p reply). In either case, the pulse initiates a long wait (long count) which ends just less than 20.3 μsec later (just less than 24.65 μsec after the F2 pulse).

(4) At the end of the long count, a check is made for an undelayed bracket decoded video pulse and also, in mode 2 or mode 3/A only, for a delayed spi pulse. If an undelayed bracket decoded video pulse is found, the reply is recognized as an emergency reply or a mode 1 i/p reply, and the undelayed bracket decoded video pulse is passed to the correct code pulse generation circuit as an i/p or emergency video pulse. In mode 2 or mode 3/A, if an undelayed bracket decoded video pulse is not found, the reply is recognized as an i/p reply, and the delayed spi pulse is passed to the correct code pulse generation circuit as the i/p or emergency video pulse. In either case, the i/p or emergency video pulse is delivered at a nominal spacing of 24.65 μsec from the leading edge of the F2 pulse.

(5) If an undelayed bracket decoded video pulse is found at the end of the long count, it initiates another short count which ends just less than 4.35 μsec later, and the i/p or emergency reply decoding cycle repeats from (2), above. If an undelayed bracket decoded video pulse is not found at the end of the long count, the i/p or emergency reply decoding cycle ends.

b. On i/p and emergency code card 1A2A2A7, the short and long counts are carried out in a seven-stage counter which counts negative-going edges of the inverted 5 mc clock input while the count enable at the counter reset is high. The count enable is provided through OR A10C by the combination of count enable flip-flop A6B and a reset stretching circuit composed of digital single-shot A14A, A14B, and A13A. The purpose of the digital single-shot is to hold the counter stages reset for 0.1 to 0.3 μsec after the count enable goes high, so that a sufficiently wide reset pulse will be obtained in cases where the end of one count is followed immediately by the start of another count.

(1) Before the start of a count flip-flop A6B is in its set state, and its low $\overline{Q}$ output holds the seven stage counter disabled and reset to zero (binary 0000000). Flip-flop A14A is reset at this time, delivering a high $\overline{Q}$ output to OR A10C and a low Q output which holds flip-flop A14B reset.

(2) When AND A13C delivers a negative-going counter start pulse, its leading edge sets flip-flop A14A and resets flip-flop A6B. When flip-flop A14A is set, its high Q output removes the reset from flip-flop A14B, thereby allowing A14B to be set by the next negative-going $\overline{5 \text{ mc clock}}$ pulse edge (0.0 to 0.2 μsec after A14A is set). The high Q output of A14B enables AND A13A to produce a negative-going output when the $\overline{5 \text{ mc clock}}$ goes high, thereby resetting flip-flop A14A. With flip-flops A6B and A14A reset, and the reply enable 1 input high, all inputs to OR A10C are high. The resultant low output from A10C enables the seven stage counter and disables AND A3C, A3D. The counter now counts negative-going edges of the $\overline{5 \text{ mc clock}}$ pulses and continues to count until flip-flop A6B is set by a counter stop pulse from OR A7A, which restores the initial conditions.

c. Each negative-going $\overline{\text{sif correct code pulse}}$ from the correct code pulse generation circuit is applied to AND A3D, A3C, where the enable from OR A10C is high whenever a count is not in progress. With AND A3D, A3C enabled, the $\overline{\text{sif correct code pulse}}$ is passed as a negative-going pulse which accomplishes the following:

(1) Its leading edge starts a count by passing through OR A10B (short count start) and through AND A13C (enabled by reply enable 1, which is high at all times except while an sif challenge is being generated) to the count enable and digital single-shot flip-flops.

(2) Its trailing edge is passed through OR A3A to set flip-flop A2B. The resulting low $\overline{Q}$ output from A2B disables AND's A10A and A3B.

(3) Its leading edge resets flip-flop A6A by passing through OR A13D, A13B. The resulting high $\overline{Q}$ output from A6A is applied as a short count decode enable to short count decode AND A8 so that the count now starting is a short count.

(4) Its trailing edge sets flip-flop A11B by passing through OR A7B. The resulting

low $\overline{Q}$ output from A11B disables AND's A15A, A15B, A15C and A7C.

d. The counter begins counting as soon as the stretched reset from the digital single-shot goes high at A12A, A12B. When the count reaches 17 (binary 10001) the binary enables at AND A8 pass the eighteenth clock pulse as a negative-going $\overline{\text{short count stop pulse}}$ through OR A7A to the clock input of counter enable flip-flop A6B and directly to the reset input of flip-flop A2B. The $\overline{\text{short count stop pulse}}$ accomplishes the following:

(1) The leading edge of the $\overline{\text{short count stop pulse}}$ resets flip-flop A2B. The resulting high $\overline{Q}$ output from A2B enables AND A10A, where the reply will be recognized as an i/p or emergency reply if the F2 pulse (in the buffered 4.35 μsec delay line output) is followed by a pulse 4.35 μsec later (in the buffered 0.0 μsec delay line input). The high $\overline{Q}$ output from A2B also enables AND A3B, whose purpose is to pass the F2 pulse through OR A3A to the clock input of flip-flop A2B, where the trailing edge will return A2B to the set state after AND A10A has had a chance to recognize the reply as an i/p or emergency reply. Finally, the high $\overline{Q}$ output from A2B at the clock input of short count decode enable flip-flop A6A prepares A6A to go set and disable short count decode AND A8 as soon as the trailing edge of the F2 pulse returns flip-flop A2B to the set state, so that if AND A10A has recognized the reply as an i/p or emergency reply the next count will be a long count.

(2) After inversion through OR A7A, the negative-going trailing edge of the $\overline{\text{short count stop pulse}}$ sets counter enable flip-flop A6B. The resulting low $\overline{Q}$ output from A6B stops and resets the counter.

e. After the $\overline{\text{short count stop pulse}}$ resets flip-flop A2B, an i/p or emergency reply, if received, is detected in AND A10A as a pair of simultaneous pulses in the buffered 4.35 μsec (F2) and 0.0 μsec (spi or emergency bracket F1) delay line outputs. The negative-going pulse output from AND A10A resets flip-flop A6B and sets flip-flop A14A to start another count as in *b* above. While this count is getting started, the F2 pulse in the buffered 4.35 μsec delay line output passes through AND A3B, and its trailing edge sets flip-flop A2B. This terminates the high $\overline{Q}$ output from A2B, thereby disabling AND's A10A and A3B, and also completes the setting of flip-flop A6A. The low $\overline{Q}$ output from A6A then disables short count decode AND A8, so that the count now starting will be a long count.

f. After the count reaches 98 (binary 1100010) the binary enables at AND A9 pass the ninety-ninth clock pulse as a negative-going $\overline{\text{long count stop pulse}}$ through OR A7A to the clock input of flip-flop A6B, through OR A13D, A13B to the reset input of flip-flop A6A, and directly to the reset input of flip-flop A11B. The $\overline{\text{long count stop pulse}}$ accomplishes the following:

(1) The leading edge of the $\overline{\text{long count stop pulse}}$ resets flip-flop A11B. The resulting high $\overline{Q}$ output from A11B enables AND A15A, whose function is to detect emergency brackets (undelayed bracket decoded video), if received. The high $\overline{Q}$ output from A11B also enables AND A15C, whose function is to deliver negative-going $\overline{\text{i/p or emergency video}}$, if received. The i/p or emergency video is the output of OR A15D: either the detected emergency brackets from AND A15A, or, in mode 2 or mode 3/A, the delayed spi pulse from AND A7C. Finally, the high $\overline{Q}$ output from A11B enables AND A15B to pass the delayed spi pulse (or the F1 pulse of a pair of emergency brackets) through OR A7B to the clock input of flip-flop A11B. This sets the flip-flop after AND A15A has had a chance to detect an emergency bracket decoded video pulse and AND A15C has had a chance to pass i/p or emergency video, if any.

(2) The leading edge of the $\overline{\text{long count stop pulse}}$ from AND A9 resets flip-flop A6A. The resulting high $\overline{Q}$ output from A6A enables short count decode AND A8, so that the next count will be a short count.

(3) The trailing edge of the $\overline{\text{long count stop pulse}}$ from AND A9 sets flip-flop A6B. The resulting low $\overline{Q}$ output from A6B stops and resets the counter.

g. After the long count stop pulse resets flip-flop A11B, a positive-going undelayed bracket decoded video pulse will reach AND A15A if the reply was

either an emergency reply or a mode 1 i/p reply, and a positive-going pulse from the 20.3 μsec delay line output will reach AND A7C (either the spi pulse of a mode 2 or mode 3/A i/p reply, or the bracket F1 pulse of an emergency reply or a mode 1 i/p reply).

(1) If an undelayed bracket decoded video pulse reaches AND A15A, it passes as a negative-going pulse to OR A15D and also through OR A10B and AND A13C to start another count as in *b* above. While this count is getting started, the positive-going delayed spi or bracket F1 pulse from the buffered 20.3 μsec delay line output passes through AND A15B, and its trailing edge sets flip-flop A11B after AND A15A has had a chance to detect an undelayed bracket decoded video pulse and after AND A15C has had a chance to pass the corresponding $\overline{\text{i/p or emergency video}}$ pulse output. The count now getting started is a short count, and the i/p and emergency reply decoding cycle repeats from *d* above.

(2) If an undelayed bracket decoded video pulse does not reach AND A15A after the end of the long count, the reply was not an emergency reply or a mode 1 i/p reply, and therefore was a mode 2 or mode 3/A i/p reply. With no output from AND A15A, a new count is not started, and when flip-flop A11B is set by the trailing edge of the delayed spi pulse from the buffered 20.3 μsec delay line output, as in (1) above, the i/p and emergency reply decoding cycle has ended.

h. A new i/p or emergency reply decoding cycle starts as in *c* above, each time an $\overline{\text{sif correct code pulse}}$ arrives while flip-flop A6B is set, including the brief periods at the ends of successive short and long counts.

6–11. Reply Decoding Self-Test Circuit

(fig. 24–9, zone A–36)

The reply decoding self-test circuit tests the sif and mode 4 reply decoding circuits after every radar trigger, whether the IFF set is challenging or not. A reply decoding self-test cycle is started by each self-test pretrigger, after the mode 4 pretrigger has placed the reply decoding self-test circuit in the fault state, and continues until the leading edge of the sif pretrigger. If there is no fault present, the fault state is cleared by proper reply decoding circuit responses to the self-test inputs. If a fault is present, the fault state is not cleared, and a reply decoding fault is shifted into the fault accumulator (para 5–14) by the next mode 4 pretrigger. Since reply decoding self-test is performed whether the IFF set is challenging or not, the reply decoding self-test circuits is also used to check five challenge encoding circuit signals which must not be continuously low. These are: $\overline{\text{challenge video}}$, $\overline{\text{gtc trigger}}$, $\overline{\text{isls gate}}$, 5-mc clock and $\overline{\text{5-mc clock}}$. If any of these signals are continuously low, the fault is declared as a reply decoding fault.

a. The reply decoding circuits normally receive reshaped receiver video at 16 values of delay, including the undelayed delay line input (0.00 μsec), as well as sif code digit enables corresponding to the CODE SELECT switch settings at the control box, when the IFF set challenging in one of the sif modes. During each reply decoding self-test cycle, three combinations of these inputs are simulated: one representing a mode 4 reply; another representing a correctly coded sif reply for code 7777 (all code pulses); and the third representing an incorrectly coded sif reply for code 0000. The reply decoding circuit responses to these combinations are then checked to verify that—

(1) The triple pulse decoding circuit is capable of producing a triple pulse decoded video pulse in response to a mode 4 reply;

(2) The sif reply decoding circuits are capable of producing both an sif correct code video pulse and a bracket decoded video pulse in response to a correctly coded sif reply;

(3) The sif reply decoding circuits are capable of producing kill pulses in response to sif replies which are incorrectly coded with an extra (unexpected) code pulse in every possible code pulse position; and

(4) The delay line and delay line drive circuit has functional continuity to the 0.00 μsec delay line input and through the delay line to every tap used for reply decoding.

b. The first two of these conditions, and part of the fourth condition, are verified at self-test pretrigger time, when the reshaped self-test pretrigger is delivered to the delay line time sharing circuit (para 5–7), and to the reply decoding self-test circuit by the pretrigger reshaping circuit (para 5–6). The delay line time sharing circuit passes the reshaped self-test pretrigger to the delay line and delay line drive circuit (para 5–8), where it enters

the delay line and simultaneously appears at one of the 16 delay line buffers (0.00 μsec) serving the reply decoding circuits. At the same time, the reply decoding self-test circuit applies the reshaped self-test pretrigger to the other 15 delay line buffers and to the two kill override gates in the correct code pulse generation circuit (para 6–9). With the reshaped self-test pretrigger present at all 16 delayed inputs to the reply decoding circuits, the effect is as though a mode 4 reply and an sif code 7777 reply had both entered the delay line and reached the proper positions for decoding. With the pretrigger present at both kill override gates, kill pulses are prevented, and the effect is as though the IFF set were challenging in mode 2 or mode 3/A with the CODE SELECT switches set to 7777 at the control box, so that the simulated sif code 7777 reply is "correctly coded".

c. The third condition of *a* above, and the remainder of the fourth condition, are verified while the reshaped self-test pretrigger is passing through the delay line. The reply decoding self-test circuit, after verifying the first two conditions and part of the fourth, overrides the existing code digit enables, if any, at all 12 code pulse detectors of the code pulse decoding circuit (para 6–6) to produce an effect equivalent to a CODE SELECT switch setting of 0000. With that setting, the reshaped self-test pretrigger should produce a kill pulse each time it passes one of the delay line taps serving a code pulse detector. It should also produce buffered 1.8, 3.6 and 20.3 μsec pulses while passing those three taps.

d. If all four conditions are verified, the reply decoding self-test cycle ends with a no-fault output to be shifted into the fault accumulator by the next mode 4 pretrigger. If, instead, any of the conditions are not verified, the cycle ends with a fault output to be shifted into the fault accumulator.

e. On coder-decoder self-test card 1A2A2A8, all flip-flops in the reply decoding self-test circuit except decoding fault flip-flop A7B are reset at the end of each reply decoding self-test cycle by a ripple reset action which begins when the $\overline{\text{sif pretrigger}}$ resets decoding control flip-flop A14B. Decoding fault flip-flop A7B is left either in the reset (no-fault) state or the set (fault) state, depending on the results of the reply decoding self-test cycle, until the results are shifted into the fault accumulator by the next mode 4 pretrigger. The trailing edge of that mode 4 pretrigger then clocks A7B into the set (fault) state for the next reply decoding self-test cycle, which will either clear the fault state or leave it at fault, depending on the test results.

f. Approximately 340 μsec after the mode 4 pretrigger, the leading edge of the $\overline{\text{self-test pretrigger}}$ sets flip-flop A14B, thereby removing the reset from flip-flops A14A and A15A and enabling AND's A11A, A11B to pass the reshaped self-test pretrigger contained in the reshaped self-test and sif pretrigger input. The $\overline{\text{reshaped self-test pretrigger}}$ output of AND's A11A, A11B is used to simulate the mode 4 reply and the correctly coded 7777 sif reply described in *b* above. If there is no fault present, the reply decoding circuits supply a triple pulse decoded video pulse simultaneously with the leading edge of the $\overline{\text{reshaped self-test pretrigger}}$ and, 0.25 μsec later, an sif correct code video pulse and a bracket decoded video pulse. The trailing edge of the triple pulse decoded video pulse occurs while the sif correct code video pulse is present (high) and clocks flip-flop A14A set, thereby enabling flip-flop A15A to be clocked set by the trailing edge of the bracket decoded video pulse. If flip-flops A14A and A15A are both set, the first two conditions of *a* above, and part of the fourth, have been verified, and $\overline{\text{code override}}$ is supplied to the code pulse decoding circuit (para 6–6) to simulate a CODE SELECT switch setting of 0000 to prepare for the remainder of the reply decoding self-test cycle.

g. The remainder of the cycle checks the kill portions of the code pulse decoding circuit, the continuity of the delay line to all taps used for reply decoding, and the five challenge encoding circuit signals which should not be continuously low. When the CODE SELECT switch setting is 0000 as simulated by low $\overline{\text{code override}}$, every pulse passing any one of the 12 sif code pulse taps should produce a kill pulse. The reshaped self-test pretrigger should therefore produce 12 kill pulses while passing through the delay line: four on the $\overline{\text{B2 through D4 kill}}$ line, and eight on the $\overline{\text{C1 through D1 kill}}$ line. The reshaped self-test pretrigger should also produce buffered 1.8, 3.6, and 20.3 μsec pulses when passing the corresponding taps. To check for all 15 pulses, the $\overline{\text{kill}}$ pulses are applied through OR A11C to a four-stage ripple counter (flip-flops A10A, A6B, A6A, and A7A) which is fully enabled only if flip-flops A15B and A10B are set by buffered 1.8- and 3.6-μsec pulses, respectively, and if the five challenge encoding circuit signals involved are not continuously low. If these requirements are met, a count of 12 (binary 1100) in the counter enables AND A8A to pass the buffered 20.3-μsec pulse as

a reset pulse for decoding fault flip-flop A7B. Under no-fault conditions, the sequence of events is as follows (fig. 24-10, part C):

(1) First, the D4 kill pulse (at 1.45 μsec) advances the binary count in the four-stage ripple counter from 0000 to 0001, unless 5-mc clock is continuously low at A10A-J.

(2) Next, the buffered 1.8 μsec pulse sets flip-flop A15B, unless sif correct code video is continuously low at A15B-J. The resulting high output from A15B-J. The resulting high output from A15B-Q releases flip-flops A6B and A10B for the subsequent events.

(3) Next, the B4 kill pulse (at 2.9 μsec) advances the binary count to 0010, unless 5 mc clock is continuously low at A10A-K, or unless the isls gate input is continuously low at A6B-J and A6B-K.

(4) Next, the buffered 3.6 μsec pulse sets flip-flop A10B, unless challenge video is continuously low at A10B-J. The resulting high output from A10B-Q releases flip-flops A6A and A7A for the remaining events.

(5) The next five kill pulses (at 4.35, 5.8, 7.25, 8.7, and 11.6 μsec) then advance the binary count to 0111, unless the gtc trigger input is continuously low at A6A-J and A6A-K.

(6) The remaining five kill pulses (at 13.05, 14.5, 15.95, 17.4, and 18.85 μsec) then advance the binary count to 1100, unless the buffered 20.3 μsec line is continuously high (low at A7A-J and A7A-K). This count provides two of the three high inputs needed at AND A8A to reset decoding fault flip-flop A7B to the no-fault state.

(7) Finally, the buffered 20.3 μsec pulse arrives as the third high input to AND A8A, whereupon A7B is reset to the no-fault state.

(8) The other nine flip-flops are reset approximately 35 μsec later by the ripple reset action initiated when the sif pretrigger resets flip-flop A14B. The resulting low output from A14B-Q resets flip-flops A14A and A15A, thereby terminating the two low code override outputs, and also disables AND's A11A, A11B to prevent the passage of the reshaped sif pretrigger (present on the reshaped self-test and sif pretrigger line whenever the IFF set is challenging in an sif mode). Then, in sequence, the low output from A15A-Q resets flip-flops A10A and A15B, the low output from A15B resets flip-flops A6B and A10B, and the low output from A10B resets flip-flops A6A and A7A, completing the ripple reset.

CHAPTER 7

DISPLAY VIDEO INTERFACE CIRCUIT FUNCTIONING

Section I. BLOCK DIAGRAM DESCRIPTION

7-1. General

The display video interface circuits select the decoded replies which are to be processed, deliver them to the processor, then use the processor decisions to accept or reject the individual decoded reply pulses as target video pulses, and finally reshape the accepted target video pulses for delivery to the associated radar set as IFF display video pulses. The display video interface circuits include a test target generator which can generate a pattern of simulated decoded friendly replies to test the ability of the processor to process friendly replies in each of its active range boxes and to test the responses of the display video interface circuits to the friendly replies and to the resulting processor decisions.

7-2. Target Video Selection and Delay (fig. 24-11)

Decoded replies to be selected as target video pulses are received by the target video selection circuit (para 7-7) in the form of sif correct code video and sif bracket decoded video from the reply decoding circuits when the IFF set is challenging in an sif mode; or in the form of mode 4 time decoded video from the interrogator computer when the IFF set is challenging in mode 4; or (simulated) in the form of test target video from the test target generator (para 7-14) when the CHALLENGE switch on the control box is held at TEST (test target mode). The sif reply enable from the challenge encoding circuits and the bracket decode enable from the control box select the sif target video: sif correct code video alone when the bracket decode enable is high (SIF REPLIES switch on control box left at CODED); or both sif correct code video and sif bracket decoded video when the bracket decode enable is low (SIF REPLIES switch held at ALL). For mode 4 and the test target mode, the mode 4 time decoded video and the test target video are combined to form mode 4 time decoded/test target video, and the mode 4 enable and test target enable from the control box are combined to form a mode 4/test target enable to select that combined video: either the mode 4 time decoded video in mode 4, or the test target video in the test target mode. The selected target video (target line input) is applied to the target video reshaping circuit (para 7-8), where it is reshaped in two steps: first to a width of 0.2 to 0.4 μsec for delivery as decoded reply video to the processor, and then to a width of 0.2 μsec with clock-synchronized edges for delivery as undelayed target video to the digital delay circuit (para 7-9). The digital delay circuit delays each target video pulse by 5.0 μsec to allow the processor to reach a decision for the corresponding decoded reply video pulse, with the result that the target video pulse emerges from the digital delay circuit as a delayed target video pulse at the time when the corresponding processor decision is available, which is also the proper time for delivery to the associated radar set. The delayed target video pulse is applied to the target generation and processor bypass circuit (para 7-10) to become a target present trigger in any mode if the processor has decided that it represents a reply from an actual transponder (IFF target) and has supplied a low target level, or if the processor bypass enable from the control box is low; and it is also applied to the IFF video reshaping circuit (para 7-13) to become a friend pulse in mode 4 or in the test target mode if the processor has decided that the target is a friend and has supplied a low friend threshold or friend input, or both provided that the processor bypass enable is high. Target present pulses and friend pulses are reshaped to different widths and amplitudes in the IFF video reshaping circuit and are then combined and delivered to the associated radar set as IFF display video.

7-3. Sif Target Processing (fig. 24-11)

During sif operation, each delayed target video pulse applied to the target generation and processor bypass circuit represents a decoded sif reply which has been delayed by 5 μsec. The target input

represents the processor decision. If the processor has decided that the decoded reply is a target reply (target input low), and the processor is not being bypassed (processor bypass enable high), the delayed target video pulse is gated to the IFF video reshaping circuit as a target present trigger to be reshaped to a nominal width of 1.0 μsec and a nominal amplitude of 3.0 volts across 75 ohms for delivery to the associated radar set on the IFF display video line.

7–4. Mode 4 Target Processing
(fig. 24–11)

a. During mode 4 or test target operation, each delayed target video pulse from the digital delay circuit represents a mode 4 time decoded or test target video pulse which has been delayed by 5 μsec. The target, friend threshold, and friend inputs represent the processor decision. If the processor has decided that the decoded reply is a target reply (target input low), and the processor is not being bypassed, the delayed target video pulse is gated to the IFF video reshaping circuit as a target present trigger to be reshaped to the same width and amplitude as described for an sif target present trigger in the preceding paragraph.

b. In mode 4 or the test target mode, the processor may also decide that the decoded reply is sufficiently consistent to be a friendly reply, and will then supply low friend threshold and/or friend inputs to the friend generation circuit (para 7–11). If the processor is not being bypassed, this causes the friend generation circuit to produce a friend stored level which enables the IFF video reshaping circuit to reshape the delayed target video pulse for delivery to the associated radar set as a friend pulse on the IFF display video line. The friend pulse has a nominal width of 5 μsec and a nominal amplitude of 5.0 volts across 75 ohms and therefore masks the simultaneous target present pulse on the IFF display video line.

7–5. Processor Bypassing

The processor decisions can be bypassed by setting the PROCESSOR switch on the control box to BYPASS. This produces a low processor bypass enable, which inhibits the target and friend generation circuits and gates all delayed target video pulses to the IFF video reshaping circuit as target present triggers to be reshaped and delivered to the associated radar set on the IFF display video line.

7–6. Display Video Interface Self-Test
(fig. 24–11)

a. The display video interface self-test circuit monitors the passage of signals through the display video interface circuits and generates low delayed video fault, decoded reply fault, target fault, or friend fault outputs if a fault condition is detected. A monitoring interval (self-test cycle) begins at the time of each self-test pretrigger, and the resulting fault outputs are combined and shifted into the fault accumulator by the next self-test pretrigger. Display video interface self-test occurs only when replies are being processed.

b. If faults are detected during two of any three consecutive self-test cycles, the fault accumulator supplies a high (fault) interface fault output to the fault indication circuit (ch. 8), which lights the INTERFACE FAULT lamp on the synchronizer front panel and supplies a low synchronizer fault indicator enable level to the control box to light the SYN SELF TEST indicator lamp.

Section II. LOGIC DIAGRAM DESCRIPTION

7–7. Target Video Selection Circuit
(fig. 24–12, zone B–4)

a. The target video selection circuit selects the decoded replies which are to be processed as target video for the operating mode established at the control box. The selected video is reshaped and supplied both to the processor, as decoded reply video for target or friend decisions, and to the digital delay circuit, as undelayed target video to be delayed long enough for the processor to reach its decisions. The target video selection circuit also accepts the mode 4 enable and test target enable inputs from the control box and delivers the separate and combined mode 4 and test target enables required elsewhere in the display video interface circuits and also in the challenge encoding and reply decoding circuits.

b. During sif reply time, on target video card 1A2A1A4, the sif reply enable is high, enabling AND A14A to pass sif correct code video and also enabling AND A9A to pass sif bracket decoded video if the bracket decode enable is low (SIF REPLIES switch on the control box held at ALL). During

mode 4 or test target operation, the mode 4/test target enable is high, enabling AND A13D to pass mode 4 time decoded/test target video. The selected video signal is passed through OR A9C to the target video reshaping circuit as the target line input.

7–8. Target Video Reshaping Circuit

(fig. 24–12, zone C–6)

a. The target video reshaping circuit digitally reshapes each pulse in the selected decoded reply video (target line input) in two steps: first to a width of 0.2 to 0.4 μsec, with its leading edge coincident with the target line input pulse, for delivery to the processor as a decoded reply video pulse; and then to a width of 0.2 μsec with clock-synchronized leading and trailing edges for delivery to the digital delay circuit as undelayed target video. During sif operation each sif bracket decoded video pulse is reshaped separately to a width of 0.2 to 0.4 μsec and included in the decoded reply video to the processor, where it is processed in the same way as an sif correct code video pulse. However, since it is not supplied to the digital delay circuit, any processor decisions based on the sif bracket decoded video pulse alone have no effect.

b. On target video card 1A2A1A4, the leading edge of each target line input pulse from the target video selection circuit sets flip-flop A2B which, together with flip-flop A2A and AND A7A, constitute a 0.2 to 0.4 μsec digital single-shot. When A2B is set, one input to OR A6B, A5C is made low, thereby starting the decoded reply video output pulse. Also, the high Q output of A2B enables flip-flop A2A to be set by the next negative-going edge of the 5-mc clock. When A2A is set, the undelayed target video pulse to the digital delay circuit is started, and AND A7A is enabled to pass the next positive-going clock pulse edge as a reset pulse for flip-flop A2B. Flip-flop A2A is then reset by the next negative-going clock pulse edge. When A2A is reset, the decoded reply video pulse at the output of OR A6B, A5C and the undelayed target video pulse (A2A–Q) to the digital delay circuit are terminated. Because a decoded reply video pulse can start at any point in a 5-mc clock cycle, and because it ends on the second negative-going clock pulse edge thereafter, the decoded reply video pulse can have any width from 0.2 to 0.4 μsec. The corresponding undelayed target video pulse is actually the final 0.2 μsec of that decoded reply video pulse width, and its leading edge is thus delayed 0.0 to 0.2 μsec with respect to the leading edge of the decoded reply video pulse (and therefore also with respect to the target line input pulse). This delay adds to the 5.0 μsec inserted by the digital delay circuit, with the result that the total delay of each delayed target video pulse, measured with respect to the leading edge of the corresponding decoded reply video pulse, is 5.0 to 5.2 μsec.

c. During sif operation (sif enable high) the leading edge of each sif bracket decoded video pulse sets flip-flop A1B which, together with flip-flop A1A and AND A5A, constitute another 0.2 to 0.4 μsec digital single-shot. The operation of this circuit is identical to that of the target video reshaping single-shot described in *b* above, except that the Q output of flip-flop A1A is not applied to the digital delay circuit.

7–9. Digital Delay Circuit

(fig. 24–12, zone C–9)

a. The digital delay circuit accepts each undelayed target video pulse from the target video reshaping circuit, delays it by 5.0 μsec in a shift register (digital delay line), stretches the delayed target video pulse to a width of 0.8 μsec, and produces a friend reset pulse before terminating the delayed target video pulse. The delayed target video pulse is delivered to the target generation and processor bypass circuit for possible selection as a target present trigger, and is also delivered to the IFF video reshaping circuit for possible selection as a friend pulse by a stored friend decision from the friend generation circuit in mode 4 or the test target mode. The friend reset pulse is delivered to the friend generation circuit to clear the stored friend decision, if any, before the delayed target video pulse ends, and therefore before any other delayed target video pulse can arrive and be selected by the same stored friend decision.

b. On target video card 1A2A1A4, each undelayed target video pulse is shifted through 25 shift register stages at a 5-mc clock rate (0.2 μsec per stage) for the delay of 5.0 μsec, and is then held in the 25th stage for four additional shifts to stretch its width to 0.8 μsec so that a friend reset pulse can be generated before the delayed target video pulse ends (fig. 24–13, part A). Most of the stages involved are in integrated circuit shift registers (A3, A4, and A8) which shift on the positive-going edges of their clock (C) inputs, and the remainder are individual flip-flops which shift on negative-going

edges of their C inputs. To insure that all stages shift in synchronism (a requirement in any shift register), the 5-mc clock signal for the C inputs of the flip-flops (including the input source stage, A2A) is inverted with respect to the 5-mc clock signal for the C inputs of the integrated circuit shift registers by inverter A12A.

c. The circuit which quadruples the width of delayed target video pulses in flip-flop A11A and generates the corresponding friend reset pulses is composed of flip-flops A11B, A15A, and A10, together with AND A7B. Each time a delayed target video pulse is shifted into A11A, the resulting high delayed target video level at A11A–Q enables flip-flop A11B to be set by the first of the next four negative-going edges of the 5-mc clock signal, and the high level at A11B–Q, in turn, enables flip-flop A15A to be set by the second negative-going edge. Flip-flop A10 then has three high J inputs and is accordingly set by the third negative-going edge. The resulting high output from A10–Q then provides the high K inputs which allow the fourth negative-going edge to reset A11A, A11B, and A10, thereby terminating the delayed target video pulse 0.8 μsec (four cycles of the 5-mc clock signal) after it was shifted into A11A from A8.

d. When flip-flop A15A is set (0.4 μsec after a delayed target video pulse is shifted into A11A), its high Q output enables AND A7B to pass the next positive-going half-cycle of the 5-mc clock signal to the friend generation circuit as a friend reset pulse. The effect of the next few negative-going edges of the 5-mc clock signal at A15A depends on the friend stored level at A15A–K, and thus depends on whether or not a friend decision has been stored in the friend generation circuit. If not, friend stored is high at A15A–K, enabling the next negative-going edge at A15A–C to reset A15A. Then, because A11B remains set until after the following negative-going edge, that edge and its successor can set and reset A15A once again. If, instead, a friend decision has been stored for the delayed target video pulse, friend stored is low at A15A until after the trailing edge of the first friend reset pulse has cleared the stored friend decision. As a result, the negative-going edge at A15A–C which coincides with the trailing edge of the friend reset pulse is unable to reset A15A, and A15A remains set until the following negative-going edge, which then resets all four flip-flops and thereby terminates all action.

7–10. Target Generation and Processor Bypass Circuit

(fig. 24–12, zone C–16)

The target generation and processor bypass circuit retimes the processor target decisions and then uses the retimed target decisions (or the processor bypass enable, if the PROCESSOR switch on the control box is at BYPASS) to gate delayed target video pulses, if any, to the IFF video reshaping circuit as target present triggers to be reshaped and delivered to the associated radar set as target present pulses in the IFF display video.

a. The processor target decisions contained in the target input to buffer circuit 1 card 1A2A1A8 are valid during range boxes 1 through 47, but are not valid during the processor self-test gate which follows range box 47. The processor self-test gate input is therefore used on the buffer circuit 1 card at AND A6B to gate off (inhibit) the nonvalid portion of the target input. The valid portion is then passed to display video card 1A2A1A5 and interface self-test card 1A2A1A1 as target gated and its complement, target gated.

b. When the processor decides that the decoded replies in a given range box are sufficiently consistent to represent an actual target, the target input goes low at processor read time in the range box and remains low for a period of 4.0 μsec (until read time in the next range box). The target gated signals thus represent target decisions from read time to read time in each range box. However, the timing required for proper gating of the corresponding delayed target video pulse, if any, is from strobe pulse to strobe pulse, rather than from read time to read time, because the interval from read time to read time does not include the latest possible time of arrival of the delayed target video pulse from the digital delay circuit.

c. The required strobe-to-strobe timing is obtained on display video card 1A2A1A5, where the target gated information is shifted into flip-flop A6B by successive processor strobe pulses (fig. 24–13, part B). When the processor decision is target present, the high target gated and low target gated inputs enable AND A1A and disable AND A2D. The strobe pulse of the range box then emerges from AND A1A as a strobed target pulse which resets flip-flop A6B, thereby storing the target present decision in A6B at the leading edge of the strobe pulse. The strobed target pulse is also supplied to the friend generation circuit, where the processor

friend decisions in mode 4 and the test target mode are similarly retimed in flip-flop A6A.

7-11. Friend Generation Circuit
(fig. 24-12, zone B-16)

The friend generation circuit retimes the processor friend decisions for delivery as friend stored pulses to the IFF video reshaping circuit. The IFF video reshaping circuit uses the friend stored pulses to select the corresponding delayed target video pulses, if any, to be reshaped and delivered to the associated radar set in mode 4 or the test target mode as friend pulses in the IFF display video.

a. Like the target decisions contained in the target input (para 7-10*b*), the processor friend decisions contained in the friend threshold and friend inputs to target video card 1A2A1A4 are timed read-to-read, rather than strobe-to-strobe. That is, each time the processor decides (in mode 4 or the test target mode) that the decoded replies in a given range box are sufficiently consistent to represent a friendly target, the low friend threshold and/or friend levels which indicate the decision begin at read time in the range box and end 4.0 μsec later (at read time in the subsequent range box). The friend threshold input goes low for that period during the prp in which the decision is the first reached, but the friend input does not go low until the corresponding period in the next prp. The friend input then goes low for that period during each subsequent prp until the processor decides that the target has ceased to reply (target end). Thus, the combination of the low friend threshold input and a high friend input represents the first friend decision for a target, and a low friend input represents each subsequent friend decision for the same target.

b. The first friend decision for each target is detected on target video card 1A2A1A4, where AND A16C receives the friend threshold input after one inversion and receives the friend input after two inversions. The output of AND A16C, tail trigger, is then low when friend threshold is low but friend is high, and is high under all other conditions.

c. The tail trigger is delivered to display video card 1A2A1A5, where it is applied to one input of OR A1C. The other (eyelash trigger) input to OR A1C is the friend input from the processor after two inversions: one on 1A2A1A4, and the other on 1A2A1A5 through AND A1D (always enabled). With either input low during a range box OR A1C enables AND A1B, A2C to pass the strobe pulse of the range box, which is applied to AND A1B, A2C in the form of a strobed target pulse from the target generation circuit (para 7-10*c*). This resets flip-flop A6A and thereby stores the friend decision at the leading edge of the strobe pulse. The use of strobed target pulses at AND A1B, A2C has the effect of canceling the nonvalid friend decisions which occur during the processor self-test gate, because the strobed target pulses are inhibited during the processor self-test gate by target gating (para 7-10*a*).

d. When flip-flop A6A is reset, its friend stored output is high at friend pulse single-shot A4 in the IFF video reshaping circuit, enabling the corresponding delayed target video pulse, from the digital delay circuit to trigger the single-shot, provided that the display gate input from the display gate generation circuit is low (para 7-12). As soon as the friend pulse single-shot has been triggered, the high friend stored output of flip-flop A6A is no longer necessary and is cleared by a friend reset pulse from the digital delay circuit. The friend reset pulse clears the high friend stored output by passing through OR A5B and setting A6A. The other output of A6A, friend stored, is supplied to the digital delay circuit and to the friend self-test circuit (para 7-17). However, if a delayed target video pulse does not arrive, the friend pulse single-shot is not triggered, and the digital delay circuit will not supply a friend reset pulse to clear the high friend stored output of A6A. In this case, the high friend stored output will be cleared by a strobe pulse as soon as the eyelash trigger is high (during a subsequent range box) at AND A5A. The high eyelash trigger will enable the strobe pulse to pass through AND A5A and OR A5B to set flip-flop A6A and thereby clear the high friend stored (and low friend stored) output .

7-12. Display Gate Generation Circuit
(fig. 24-12, zone A-13)

The display gate generation circuit generates the display gate which establishes the time during which IFF display video is supplied to the associated radar set. The display gate is started by the processor start pretrigger (approximately 9.8 μsec before radar zero range time). On test target gen-

erator card 1A2A1A3, each processor start pretrigger triggers single-shot A5 into its active state, making one input to AND A12C high. The other input to AND A12C is the processor self-test gate, which is low during processor self-test time (range box 48) and high at all other times. The resultant display gate output of AND A12C is supplied to the IFF video reshaping circuit, where it enables the generation of IFF display video. The processor self-test gate normally goes low approximately 188 μsec after the processor start pretrigger, and the active state duration of single-shot A5 is adjusted (to 188 μsec by means of potentiometer R2) so that A5-Y goes low at the same time. Thus, the display gate output of AND A12C is terminated either by the processor self-test gate or, if the processor is removed or not operational (processor self-test gate input continuously high), by the end of the active state of single-shot A5.

7-13. IFF Video Reshaping Circuit
(fig. 24-12, zone B-18)

The IFF video reshaping circuit reshapes the target present triggers and friend stored pulses from the target generation and processor bypass and friend generation circuits for delivery as IFF display video to the associated radar set.

a. On display video card 1A2A1A5, each target present trigger represents a correctly decoded reply which has been processed and identified as a target by the processor. The target present trigger is ANDed with the display gate, which is low during the time that IFF display video can be delivered to the associated radar set, and reshaped to a duration of 1.0 μsec by infinitely retriggerable single-shot A3. The active state duration of the single-shot is adjusted by potentiometer R1. If the target present trigger represents an actual or simulated (test target) mode 4 reply which has not yet been identified as friendly, the reshaped target present trigger is buffered and delivered to the associated radar set as an IFF display video pulse.

b. The friend stored input represents a mode 4 reply or a test target video pulse which has been identified as friendly. The delayed target video pulse input, from the digital delay circuit (para 7-9), represents the decoded reply pulse sent to the processor to reach the friend decision, except that it is delayed by 5.0 to 5.2 μsec. If the friend stored and delayed target video pulses are simultaneously present, indicating that the friend stored pulse is the result of this particular delayed target video pulse, and if the display gate is low, infinitely retriggerable single-shot A4 is triggered into its active state (approximately 5.0 μsec). The active state duration of the single-shot is adjusted by potentiometer R3. The friend present output of single-shot A4 passes through AND A7A if the mode 4/test target enable is high and the processor is not being bypassed (processor bypass enable high). The output of AND A7A is combined with the reshaped target present output of single-shot A3 in potentiometer R2, buffered, and then delivered to the associated radar set as an IFF display video pulse. Since the duration of the reshaped friend present pulse (5.0 μsec) is longer than the duration of the reshaped target present pulse (1.0 μsec), it is painted in the radar display as a long bar (tail or eyelash, para 7-11), thereby identifying the reply as friendly. The setting of potentiometer R2 establishes the amplitude of the friend present pulse at a level equal to or greater than the fixed amplitude of the target present pulse. This allows the associated radar set to discriminate between target and friend pulses on the basis of their pulse amplitudes in the IFF display video.

7-14. Test Target Generator
(fig. 24-12, zone A-6)

a. The test target generator generates test target video pulses while the CHALLENGE switch on the control box is held at TEST (test target enable low). The test target video is a pattern of simulated decoded mode 4 friend replies which are passed through the synchronizer display video interface circuits and the processor to become IFF display video pulses. At the associated radar set, these pulses provide a visible indication of the ability of the processor to properly process friend replies in each of its active range boxes and the ability of the display video interface circuits to generate IFF display video in accordance with the processor decisions. For adequate range and azimuth separation in the test pattern display, the test target video pulses are generated in 16 separate groups, with the pulses in each group spaced 16 range boxes (9.6 kilometers) apart, and with the pulses in each group one range box (0.6 kilometer) greater in range than the corresponding pulses in the preceding group. In this manner each complete cycle of 16 consecutive groups of test target video pulses simulates individual decoded mode 4 friend replies in all active range boxes.

b. Each individual test target video pulse simulates a decoded reply in a given range box and is repeated in the same range box 32 times in succession to simulate a decoded friend reply. To simulate each group of decoded friend replies, therefore, a set of test target video pulses 9.6 kilometers apart is generated and repeated at the same ranges 32 times in succession. For synchronization with the respective range boxes, each set of pulses is started after a processor start pretrigger and is generated by counting strobe pulses and delivering every sixteenth strobe pulse as a test target video pulse until the set of pulses is terminated after range box 47 by the next processor self-test gate. After a set of pulses has been repeated 32 times for 32 consecutive processor start pretriggers, no test target video pulses are generated for the next 32 consecutive processor start pretriggers. This provides an adequate azimuth spacing between test targets in the associated radar set display. Thus, for each group of test target video pulses and the clear period that follows it, the number of processor start pretriggers (and processor self-test gates) is 64.

c. For the next 64 processor start pretriggers, another group of test target video pulses is generated, again consisting of one pulse in every sixteenth range box, repeated 32 times after the first 32 processor start pretriggers and followed by a clear period for the remaining 32 processor start pretriggers. However, the first pulse in this group is generated at a range 0.6 kilometer (one range box) greater than the first pulse of the preceding group, so that each pulse in this group occurs one range box later than the corresponding pulse in the preceding group. The generation of test target video pulses continues in this manner, one group and a clear period for every 64 processor start pretriggers, with each group synchronized to a different set of range boxes, until a complete pattern of 16 groups has simulated a decoded friend reply in each of the active range boxes, whereupon a new pattern begins. Thus, for each complete pattern of test target video pulses, the number of processor start pretriggers (and processor self-test gates) is 1024, and the pattern repeats itself as long as the CHALLENGE switch is held at TEST.

d. Test target video pulses are generated on test target generator card 1A2A1A3 by comparing the count bits in a four-stage strobe pulse counter with the count bits in the last four stages of a 10-stage processor self-test gate counter. The bits are stored in a four-bit binary comparator consisting of four exclusive-OR's and a seven-input AND.

(1) The 10-stage processor self-test gate counter is divided into two sections. The first six stages supply a scale-of-64 gate (2^5) which is alternately high and low for each group of 32 processor self-test gates. That is, starting from zero, it goes high when the count reaches 32 and remains high until the count reaches 64, at which time it goes low until a count of 96 is reached, etc. The scale-of-64 gate alternately enables and disables AND A2 to pass or inhibit test target video pulses. The trailing edge of each scale-of-64 gate is also counted by the last four stages (starting range control) of the counter so that the last four count bits (2^6, 2^7, 2^8, and 2^9), considered as a separate four-bit group count, bits are advanced once for each group of 64 processor self-test gates. This four-bit group count is applied as one set of inputs to the four-bit exclusive-OR count comparator, where it determines the starting range for each set of test target video pulses in the complete pattern of 16 sets.

(2) The trailing edge of the processor start pretrigger sets flip-flop A13A, enabling the strobe pulse counter to count trailing edges of strobe pulses until a count of 15 is reached, after which the 16th strobe pulse overflows the count to 0000, and a new count begins. This action is repeated until the leading edge of the processor self-test gate (approximately 188 μsec after the processor start pretrigger) resets flip-flop A13A, thereby resetting the strobe pulse counter and disabling AND A9C, A9D. The four-bit count output of the strobe pulse counter (2^0 thru 2^3) is supplied as the other set of inputs to the four-bit exclusive-OR count comparator.

(3) The count comparator individually compares each bit of the four-bit strobe pulse count with the corresponding bit of the four-bit group count of the last four stages (starting range control) of the processor self-test gate counter. Each time the strobe pulse count becomes equal to the count in the starting range control stages, the outputs of the four exclusive-OR's simultaneously high and, if the test target enable input (CHALLENGE switch in the TEST position) and the scale-of-64 gate are both high, AND A2 is enabled to pass the next

strobe pulse as a test target video pulse. Because the two counts are equal once during each scale-of-16 count through the strobe pulse counter, every sixteenth strobe pulse is passed as a test target video pulse, and because each strobe pulse is produced during a particular processor range box, the test target video pulses occur in every sixteenth range box.

(4) When the starting range control count (last four bits of the processor self-test gate count) is 0000, test target video pulses are generated in range boxes 1, 17 and 33 for as long as the scale-of-64 gate is high (32 processor self-test gates). When the scale-of-64 gate goes low, the starting range control count is advanced to 0001, and AND A2 is disabled. Then, the scale-of-64 gate goes high again 32 processor self-test gates later, another group of test target video pulses is generated. Then comparison is repeated. However, with a starting range control count of 0001, the pulses of this group are produced each time the strobe pulse count passes 0001, or one strobe pulse later than for the preceding group, and thus in range boxes 2, 18, and 34. Similarly, the pulses of the next group are produced in range boxes 3, 19, and 35; and the progression continues in this manner as long as the CHALLENGE switch on the control box is held at TEST.

7–15. Decoded Reply and Delayed Video Self-Test Circuit

(fig. 24–12, zone C–25)

The decoded reply and delayed video self-test circuit monitors the operation of the target video selection, target video reshaping, and digital delay circuits, and supplies a low fault output to the fault accumulator if a fault is detected.

a. Decoded Reply Test

(1) The target video selection and reshaping circuits can be considered to be functioning satisfactorily if they select and reshape the proper decoded reply pulses from the reply decoding circuits for delivery to the processor as decoded reply video pulses and to the digital delay circuits as target line inputs pulses. The decoded reply test is a pulse-by-pulse comparison test performed by interface self-test card 1A2A1A1 in flip-flop A1A. The proper decoded reply video pulses are selected and applied as fault inputs to A1A, and the corresponding decoded reply video pulses, if produced by the target video selection and reshaping circuits, are applied as fault-clearing inputs.

(2) In each sif mode, the proper decoded reply video pulses are the sif correct code video and/or sif bracket decoded video pulses, which are selected at AND A7A by the sif reply enable and passed to the set input of flip-flop A1A as comparison decoded reply video pulses. The actual decoded reply video pulses, if produced, are applied to the reset input of A1A. Thus, as long as each comparison decoded reply video pulse is matched by an actual decoded reply video pulse, the successive pulses will leave A1A in the reset (no-fault) state, delivering a high (no-fault) decoded reply fault output to the fault accumulator. If actual decoded reply video pulses are not produced, A1A will be left in the set (fault) state, delivering a low decoded reply fault output to the fault accumulator, where the self-test pretrigger will later read the low level as "fault".

(3) In mode 4, or in the test target mode, the proper decoded reply video pulses are the mode 4 time decoded/test target video pulses, which are selected at AND A11A by the mode 4/test target enable and passed to A1A as the comparison decoded reply video pulses.

b. Delayed Target Video Test. The digital delay circuit can be considered to be functioning properly if it supplies a delayed target video pulse for every undelayed target video (target line input) pulse. The test for this condition is a pulse-by-pulse comparison test similar to the decoded reply test described in *a* above. On interface self-test card 1A2A1A1, each target line input pulse is applied as a set input to flip-flop A1B, and the corresponding delayed target video pulse which should arrive approximately 5 μsec later, is applied as a reset input, If delayed target video pulses do not arrive, the flip-flop is left in the set (fault) state, delivering a low delayed video fault output to the fault

accumulator, where the next self-test pretrigger will read the low level as "fault".

7–16. Target Present Self-Test Circuit
(fig. 24–12, zone B–25)

a. The target present self-test circuit monitors the operation of the target generation circuit and supplies a low target fault output to the fault accumulator if a fault is detected. The target generation circuit can be considered to be functioning satisfactorily if it produces a target present trigger in response to each delayed target video pulse for which the processor supplies a low target input when not bypassed, or if it produces a target present trigger for every delayed target video pulse when the processor is bypassed. The test for this condition is a pulse-by-pulse comparison test similar to the decoded reply test described in paragraph 7–15*a*.

b. On interface self-test card 1A2A1A1, the delayed target video pulses for which target present triggers should be produced are selected either at AND A5C when the processor bypass enable is high, or at AND A4C, A12B when the processor bypass enable is low, and are passed to the set input of flip-flop A3A as comparison target present triggers. The actual target present triggers, if produced, are applied to the reset input of A3A. If actual target present triggers do not arrive, the flip-flop is left in the set (fault) state, delivering a low target fault output to the fault accumulator, where the self-test pretrigger will later read the low level as "fault".

c. To include the processor target decisions in the selection at AND A5C, those decisions are strobed into OR flip-flop A6C, A6D to supply an appropriate enable for AND A5C. When the processor has decided that a decoded reply video pulse represents a target, the target gated input to the friend self-test circuit is high, enabling AND A13D to deliver a negative-going self-test strobed target pulse which sets OR flip-flop A6C, A6D. At the same time, the target gated input to AND A13C is low, preventing the strobe pulse from reaching the OR flip-flop as a reset pulse. With the OR flip-flop (A6C, A6D) set, AND A5C has the high enable needed to pass the corresponding delayed target video pulse as a comparison target present trigger. For each processor no-target decision, the corresponding delayed target video pulse, if any, is prevented from reaching flip-flop A3A as a comparison target present trigger because it would not be used as an actual target present trigger in the target generation circuit. In such cases, the target gated input to AND A13C is high, enabling the corresponding strobe pulse to reset OR flip-flop A6C, A6D and thus provide a low (disabling) input to AND A5C. At the same time, the target gated input to AND A13D is low, preventing the strobe pulse from reaching the OR flip-flop (A6C, A6D) as a set pulse.

7–17. Friend Self-Test Circuit
(fig. 24–11, zone A–25)

a. The friend self-test circuit monitors the operation of the friend generation circuit and supplies a low friend fault output to the fault accumulator if a fault is detected. The friend generation circuit is self-tested only in mode 4 and the test target mode, because those are the only modes in which its outputs are used. The circuit can be considered to be functioning satisfactorily in those modes if, during each display gate, it produces a high friend stored output (low friend stored) whenever a delayed target video pulse arrives in a range box where the friend input from the processor is low. The test for this condition is a pulse-by-pulse comparison test similar to the decoded reply test described in paragraph 7–15*a*. On interface self-test card 1A2A1A1, the delayed target video pulses for which the friend input from the processor is low are selected at AND A6B, and the selected pulses are passed through OR A12C and AND A8D to set flip-flop A3B as comparison friend stored pulses which clock A3B into the set (fault) state. The actual friend stored pulses, if produced, are applied to the reset input of A3B. If actual friend stored pulses do not arrive, A3B is left in the set (fault) state, delivering a low friend fault output to the fault accumulator, where the self-test pretrigger will later read the low level as "fault".

b. For the selection at AND A6B, each low friend input from the processor is low at AND A13B and high at AND A5B, steering the corresponding strobe pulse to OR flip-flop A4D, A12A as a set pulse, rather than as a reset pulse. The target gated input (continuously low during the processor self-test gate) is used in the strobe pulse path to the set input of OR flip-flop A4D, A12A as a means of inhibiting the low friend inputs from the processor during its self-test cycles, and thus has the effect of limiting the selection at AND A6B to the duration of the display gate. With OR flip-flop A4D, A12A set, AND A6B has the high enable

needed to pass the corresponding delayed target video pulse, if any. Conversely, each high friend input from the processor is high at AND A13B and low at AND A5A, steering the corresponding strobe pulse to the OR flip-flop as a reset pulse for a low (disabling)input to AND A6B.

c. The eyelash enable input on pin 34 to AND A14 is tied to a constant low, therefore, AND A14 will constantly be high.

7–18. Fault Accumulator (Interface)

(fig. 24–12, zone D–29)

The interface fault accumulator combines the results of the four display video interface self-tests (para 7–15, through 7–17), monitors the dc levels of two timing circuit outputs (reshaped mode 4 pretrigger to the interrogator computer, and processor start pretrigger to the processor), and supplies the fault indication circuits (ch. 8) with an interface fault output representing the status of the circuits involved. The combined self-test results and the two dc levels are read by each self-test pretrigger, which thus marks the end of one interface self-test cycle and the beginning of the next. The interface fault output is normally low (no-fault), and remains low even if an occasional fault is detected, but goes high (fault) as soon as faults have been detected in two of any three consecutive self-test cycles. When high, the interface fault output remains high until a self-test cycle occurs in which no faults are detected. On interface self-test card 1A2A1A1, the fault accumulator consists of eight-input OR A2, flip-flops A10A and A10B, and their associated gates. Two of the eight inputs to A2 are made available for possible future self-test inputs (auxiliary fault inputs), but are not used in the present design. Each of the other six inputs must be high at self-test pretrigger time for a no-fault reading: if any are low the reading will be "fault". This fault accumulator is functionally identical to the coder-decoder fault accumulator, and is therefore adequately described by paragraph 5–14, with the following minor exceptions:

a. The input OR has eight inputs, rather than four;

b. Readings are taken by self-test pretriggers rather than by mode 4 pretriggers;

c. Part reference designations differ; and

d. The input for automatic error reset is an OR combination of the sif enable and the mode 4/test target enable, rather than a radar trigger fault reading. This has the effect of limiting interface self-test to the times when the IFF set is challenging or operating in the test target mode, because it forces a low (no-fault) interface fault output at all other times.

CHAPTER 8

FAULT INDICATION CIRCUIT FUNCTIONING

8-1. General

The fault indication circuits visually indicate the results of the radar trigger test performed within the timing circuits and the accumulated results of the self-tests performed within the timing, challenge encoding, reply decoding, and display video interface circuits. To indicate a fault result, the fault indication circuits light the corresponding red FAULT lamp on the front panel of the synchronizer to identify the physical location of the fault, and also supply a low (grounded) synchronizer fault indicator enable output to the control box to light the red SYN SELF TEST lamp and to prevent the green CHALLENGE lamp from lighting when challenging is attempted.

8-2. Radar Trigger Fault Indication

(fig. 24-14)

When a radar trigger fault is detected (para 4-4), the timing circuits provide a high (fault) radar trigger fault level. On buffer circuit 1 card 1A2A1A8, that input is inverted by inverter A5B and amplified through amplifier A3A,Q1 to light RADAR TRIG FAULT lamp 1A2DS1 (red). The inverted level from A5B is also applied to the other four fault indication circuits on the buffer circuit 1 card. At the ANDs in the timing, coder-decoder, and interface lamp drive circuits, it prevents the self-test fault inputs to those circuits from lighting the corresponding FAULT lamps, thereby preventing any indication of the spurious self-test fault states that almost inevitably result from loss of radar triggers. In the synchronizer fault relay drive circuit, it causes synchronizer fault relay K1 to be deenergized for as long as the radar trigger fault input is high, or for the active state duration (0.8 second) of infinitely retriggerable single-shot A1, whichever is longer. This grounds the synchronizer fault indicator enable line to the control box, which lights the red SYN SELF TEST lamp and prevents the green CHALLENGE lamp from lighting when challenging is attempted.

8-3. Timing Fault Indication

(fig. 24-14)

When a timing fault is detected, the timing self-test circuit (para 4-3) provides a high (fault) timing fault level. On buffer circuit 1 card 1A2A1A8, that input is inverted through AND A5C (unless the radar trigger fault input is also high) and amplified through amplifier A3C, Q4 to light TIMING FAULT lamp 1A2DS2 (red) as an indication that the detected fault is in timing module 1A2A4. On the buffer circuit 1 card, the inverted timing fault input is also applied to the synchronizer fault relay drive circuit, causing that circuit to deenergize synchronizer fault relay K1. When deenergized, K1 grounds the synchronizer fault indicator enable line for as long as the timing fault input is high, or for the active state duration (0.8 second) of infinitely retriggerable single-shot A1, whichever is longer. At the control box, this lights the red SYN SELF TEST lamp and prevents the green CHALLENGE lamp from lighting when challenging is attempted.

8-4. Coder-Decoder Fault Indication

(fig. 24-14)

When a challenge encoding or reply decoding fault is detected, the coder-decoder fault accumulator (para 5-14) provides a high (fault) coder-decoder fault level. On buffer circuit 1 card 1A2A1A8, that input is applied to the coder-decoder lamp drive circuit, which is identical, except for reference designations, to the timing lamp drive circuit described in the preceding paragraph. CODER DECODER FAULT lamp 1A2DS3 (red), when lighted, indicates that the detected fault is in coder-decoder module 1A2A2 or in delay line module 1A2A5. However, if the TIMING FAULT lamp is also lighted, there is a fault in timing module 1A2A4, and it is possible that the indication of a simultaneous fault in the coder-decoder module is spurious.

8-5. Interface Fault Indication

(fig. 24-14)

When an interface fault is detected, the interface fault accumulator (para 7-18) provides a high (fault) interface fault level. On buffer circuit 1 card 1A2A1A8, that input is applied to the interface lamp drive circuit, which is identical, except for reference designations, to the timing lamp drive

circuit described in paragraph 8-3. INTERFACE FAULT lamp 1A2DS4 (red), when lighted, indicates that the detected fault is in interface module 1A2A1. However, if either the TIMING FAULT lamp or the CODER DECODER FAULT lamp, or both, is also lighted, there is a fault in one or both of those modules, or in power supply module 1A2A3, and it is possible that the indication of a simultaneous fault in the interface module is spurious.

8-6. Synchronizer Fault Relay Drive

(fig. 24-14)

Whenever a radar trigger fault or a fault in one of the synchronizer modules is indicated on the front panel of the synchronizer, the synchronizer fault indicator enable line to the control box is grounded (made low). At the control box, this provides an indication that the synchronizer circuits have detected a fault by lighting the red SYN SELF TEST lamp and preventing the green CHALLENGE lamp from lighting when challenging is attempted. On buffer circuit 1 card 1A2A1A8, the four inverted fault inputs are applied to OR A2B, which deenergizes synchronizer fault relay K1 both directly, through OR A2A, A4D, and indirectly, by triggering infinitely retriggerable single-shot A1 to provide a low $\overline{Y}$ output to OR A2A, A4D for a period of 0.8 second. The single-shot is included in this circuit to ensure that every synchronizer fault indication at the control box will last long enough to be noticed, even if the indications at the synchronizer are very brief, as they might be in the event of widely spaced intermittent faults.

CHAPTER 9

POWER SUPPLY AND POWER DISTRIBUTION CIRCUIT FUNCTIONING

9-1. General

The 28-volt dc IFF set power supplied by the associated radar set is delivered to the synchronizer through the power control panel of the interrogator group case, unit 1, under the control of POWER circuit breaker 2CB1 on the control box and POWER circuit breaker 1CB1 on the power control panel. When both of those circuit breakers are ON, the 28-volt dc power is supplied to the synchronizer power supply and power distribution circuits. These circuits accept the 28-volt dc power through an input filter and a third POWER circuit breaker, 1A2CB1, deliver it as lamp voltage to the fault indication circuits, and reduce it to the +12-volt, +5-volt regulated, and −12-volt levels required in the other synchronizer circuits. A front panel voltmeter and an associated four-position voltage select switch (OUT, +5, +12, −12) are provided to monitor these levels on a go/no-go (green band) basis.

9-2. +12-Volt Regulator
(fig. 24-15)

a. The +12-volt regulator is a switching regulator circuit which reduces the 28-volt dc input to +12 volts for the +5-volt regulator (para 9-3), for the −12-volt inverter (para 9-4), and for all circuits in the synchronizer which employ +12 volts. This circuit also contains a crowbar (a silicon-controlled rectifier which, when fired, effectively short circuits the +28-volt input) to trip the POWER circuit breaker almost instantaneously when any of three circuit-endangering conditions is detected: a +12-volt output in excess of +15 volts, a +5-volt regulator output in excess of +6.9 volts, or a −12-volt inverter output less negative than −6 volts (short circuited or overloaded).

b. On +12-volt regulator card 1A2A3A1, the +28-volt input is applied to +12-volt regulator switch Q1, where it is switched on and off to flywheel circuit L1, C3, CR1 by the Y output of the voltage controlled single-shot formed by transistors Q8 through Q12. This single-shot is triggered every 100 μsec by 10-kc triggers from the −12-volt inverter circuit, and has an active state duration which depends on a duration control voltage supplied by +12-volt error amplifier Q14. The active state duration (as a fraction of the 100-μsec triggering period) determines the actual +12-volt output (as a fraction of the +28-volt input), and would be 12/28 of 100 μsec for an output of exactly +12 volts with an input of exactly +28 volts and with no voltage losses either in Q1 or in the flywheel circuit. To correct for variations in the +28-volt input and voltage losses, +12-volt error amplifier Q14 compares a sample of the +12-volt output with the fixed reference voltage from zener diode VR5, amplifies the difference, if any, and applies it to the single-shot as a change in the duration control voltage which corrects the +12-volt output by changing the on-time of Q1. The duration control voltage decreases the active state duration of the single-shot to increase the on-time of Q1, or increases the active state duration to decrease the on-time of Q1.

c. The sample of the +12-volt output for Q14 is provided by the voltage divider composed of resistors R22 and R28 and +12-volt adjustment potentiometer R27. This voltage divider samples the current limited +12-volt output provided for the −12-volt inverter circuit by −12-volt current limiter Q13, R21. The purpose of the −12-volt current limiter is to protect both the +12-volt regulator circuit and the −12-volt inverter circuit against a short circuit or similar severe overload on the −12-volt inverter circuit by reducing the +12-volt output to the −12-volt inverter circuit, under those conditions, to a value which prevents the −12-volt inverter circuit from drawing more than a maximum of about one ampere from the +12-volt regulator circuit. Normally, the current limited +12-volt output is equal to the +12-volt output minus the small saturation voltage (approximately 0.2 volt) across Q13.

d. The action of the +12-volt regulator circuit forces the +12-volt sample from R27 into equality with the reference voltage from VR5 at the inputs to Q14. Any higher sample voltage, such as might be caused by an increase in the +28-volt input or by a counterclockwise adjustment of R27, would result in a higher (more positive) duration control voltage from Q14, which would increase the

active state duration of the voltage controlled single-shot and thereby decrease the on-time of Q1. The result would thus be a decrease in the +12-volt output and a corresponding decrease in the +12-volt sample (toward equality with the reference voltage). Conversely, any lower sample voltage, such as might be caused by a decrease in the +28-volt input, or a clockwise adjustment of R27, or an increase in the voltage drop across the −12-volt current limiter, would produce the opposite result.

e. Although the principal effect of adjusting R27 is to vary the +12-volt output, the adjustment also varies the −12-volt output of the −12-volt inverter circuit, because that output is produced as a voltage very nearly equal, but opposite in polarity, to the current limited +12-volt output, without provision for separate adjustment. However, the tolerances on the +12-volt and −12-volt outputs are broad enough so that a compromise adjustment of R27 can always be found at which both voltages are within their respective tolerances.

f. To protect the synchronizer circuits, and the power supply circuits themselves, against the effects of transient voltage surges on the +28-volt input, and to prevent the +12-volt regulator from delivering a +12-volt output in excess of +14 volts (as might otherwise occur in the event of a failure causing loss of 10-kc triggers from the −12-volt inverter circuit), overvoltage detector Q6 samples the +28-volt input and the +12-volt output through a corresponding pair of zener diodes and takes control of the conduction of Q1 through switch control Q2, Q5, Q7 if either voltage becomes excessive. If the +28-volt input exceeds +37 volts, Q6 cuts off Q1 through Q2, Q5, Q7 and thus forces the +12-volt output (and therefore the +5-volt and −12-volt outputs) to zero until the +28-volt input returns to normal. This interrupts all synchronizer functions, but protects the synchronizer against the overvoltage input. However, if the +12-volt output becomes excessive while the +28-volt input is normal, as it might in the event of a +12-volt regulator failure or loss of 10-kc triggers, the overvoltage detector cannot completely cut off Q1; instead, it can only reduce the conduction of Q1 far enough to limit the +12-volt output to the maximum safe value of +14 volts, provided that the failure is not in switch control Q2, Q5, Q7 nor in regulator switch Q1 itself. If the failure is in one of those stages, the overvoltage detector cannot take control, and when the +12-volt output reaches +15 volts crowbar driver Q3 immediately turns off the synchronizer to protect its circuits by firing crowbar Q4 to trip 1A2CB1.

9–3. +5-Volt Regulator
(fig. 24–15)

The +5-volt regulator is a switching regulator circuit of the same type as the +12-volt regulator described in the preceding paragraph. On +5-volt regulator card 1A2A3A2, the +12-volt input from the +12-volt regulator is switched on and off through +5-volt regulator switch Q1 to flywheel circuit L1, C2, CR1 by the Y output of the voltage controlled single-shot composed of transistors Q7 through Q11. The duration control voltage for this single-shot is supplied by +5-volt error amplifier Q12, which compares a sample of the +5-volt output from +5-volt adjustment R23 with the reference voltage from the same Zener diode that serves the +12-volt regulator. To protect the circuits which use both +5 volts and −12 volts against undervoltage on the −12-volt line, switch control Q2, Q4, Q5, Q6 is enabled by the −12-volt output, and is designed to cut off Q1 and thereby reduce the +5-volt output to zero whenever the −12-volt line is less negative than −10 volts. A +5-volt output in excess of +6.9 volts, as might occur in the event of a +5-volt regulator failure, is sensed by crowbar driver Q3, which immediately turns off the synchronizer to protect its circuits by firing the crowbar on the +12-volt regulator card to trip 1A2CB1.

9–4. −12-Volt Inverter
(fig. 24–15)

a. The −12-volt inverter generates and rectifies a 10-kc square wave to produce a −12-volt output which is very nearly equal, but opposite in polarity, to the current limited +12-volt input from the +12-volt regulator. On −12-volt inverter card 1A2A3A3, 10-kc oscillator Q1, Q2, T1 generates a continuous 10-kc square wave, using the current limited +12-volt input as collector power. Full wave rectifier CR5, CR6 rectifies the 10-kc square wave to produce the −12-volt output, and trigger generator Q4 reshapes the square wave for delivery as 10-kc triggers (about 5 μsec wide) to the +12-volt and +5-volt regulators.

b. The −12-volt output is sampled through Zener diode VR1 to detect the undervoltage condition which would result if the −12-volt output were short circuited or severely overloaded. The sample voltage at the cathode of VR1 (−12-volt short circuit protection sample) is normally between zero

and +2 volts. This sample is applied both to crowbar trigger generator Q3 and to the −12-volt current limiter on the +12-volt regulator card. Only undervoltage (short circuit) protection is provided, because the −12-volt inverter cannot produce an overvoltage output unless its current limited +12-volt input is excessive, and in that case the overvoltage protection on the +12-volt regulator card takes control.

c. A short circuit or severe overload on the −12-volt output reduces that output toward zero volts and thus makes the short circuit protection sample at the cathode of VR1 more positive, which has one or both of two effects, depending on the duration of the short circuit or overload condition. First, the positive sample reduces the current limited +12-volt input to limit the −12-volt output current by increasing the voltage drop across the −12-volt current limiter on the +12-volt regulator card. If the condition is cleared within 0.5 to 5 seconds, depending on the severity of the overload, the current limited +12-volt input and the −12-volt output can return to normal as soon as the condition is cleared. However, if the condition is not cleared within that time, the second effect of the positive short circuit protection sample is a crowbar trigger pulse produced on the −12-volt inverter card by crowbar trigger generator Q3. The crowbar trigger pulse, on the +12-volt regulator card, fires crowbar 1A2A3A1Q4 to trip 1A2CB1 and thereby turn off the synchronizer to protect its circuits.

d. The synchronizer circuits which use both +5 volts and −12 volts are protected against −12-volt undervoltage (not only under fault conditions, but also during the build-up interval each time power is turned on) by cutting off +5 volts whenever the −12-volt output is less negative than −10 volts. This is accomplished on +5-volt regulator card 1A2A3A2, where +5-volt regulator switch Q1 is cut off through switch control Q2, Q4, Q5, Q6 by the −12-volt undervoltage.

9–5. Power Supply Fault Indication
(fig. 24–15)

The three power supply voltages can be checked on a go/no-go (green band) basis by means of meter 1A2M1 and voltage selector 1A2S1 (OUT, +5, +12, −12). The metering sensitivity is determined by the shunting combination of resistor 1A2A7R2 and meter calibration potentiometer 1A2A7R3, which is adjusted for readings at the center of the green band when the three voltages are exactly +5, +12, and −12 volts, respectively, and resistors 1A2A7R1 and 1A2A7R4 are within tolerance. (This represents a metering sensitivity of approximately 1330 ohms per volt, or 1.0 milliampere to the center of the green band.) With 1A2S1 at OUT, the meter is disconnected and short circuited, providing the dynamic damping needed to prevent vibration damage during transportation. With 1A2S1 at +5, the meter is connected to the +5-volt output, with 1A2A7R1 as the meter multiplier. With 1A2S1 at +12 or −12, the meter is connected to the corresponding voltage with the proper polarity for an up-scale reading, and with 1A2A7R4 as the meter multiplier.

9–6. Power Distribution
(fig. 24–17)

All synchronizer parts involved in the distribution of the +28-volt input and the distribution of the +12-, +5-, and −12-volt power supply voltages to the timing, coder-decoder, and interface modules are shown in the overall synchronizer schematic diagram (fig. 24–17). The distribution of the three power supply voltages within those modules is adequately indicated in the corresponding module schematic diagrams. For the distribution and control of the +28-volt input from the associated radar set to the synchronizer, refer to TM 11–5895–687–35–1.

CHAPTER 10

SYNCHRONIZER SUBASSEMBLY FUNCTIONS

Section I. INTERFACE MODULE 1A2A1A1

10-1. General
(fig. 24-18)

The interface module contains eight printed wiring cards whose circuits provide the display video interface functions described in chapter 7, the fault indication logic described in chapter 8, and most of the input and output buffering required in the external signal paths to and from the synchronizer and in the internal signal paths between the major functional circuit groups described in chapters 3 through 7. The wiring interconnections between the printed wiring cards and the interconnections to and from the sychronizer chassis through the module connectors are shown in figure 24-18. The printed wiring cards are described individually in the following paragraphs.

10-2. Interface Self-Test Card 1A2A1A1
(fig. 24-19)

a. The interface self-test card contains decoded reply and delayed video, target present, and a friend present self-test circuits which test the operation of the display interface circuits. It also contains a fault accumulator circuit. The functional operation of the decoded reply and delayed video self-test circuits are described in paragraph 7-15. The functional operation of the target present self-test circuit is described in paragraph 7-16. The functional operation of the friend self-test circuit is described in paragraph 7-17. The functional operation of the fault accumulator circuit is described in paragraph 7-18.

b. The circuits contained on the interface self-test board consist of inverters, gates, and flip-flops. In the logic diagram (fig. 24-12), inverters are sometimes combined with gates for clarity and simplicity. For information pertinent to inverters, gates, and flip-flops, refer to paragraphs, 2-5, 2-7, 2-9, and 2-10.

10-3. Level Shifter Card 1A2A1A2 or 1A2A2A1
(fig. 24-20)

a. The two level shifter cards are identical and interchangeable. Each contains ten inverter (level shifter) stages, Q1 through Q10, which are used to shift low control inputs to high control outputs for use by the challenge encoding, reply decoding, and display video interface circuits as required. Since the ten level shifter stages are identical, only one (Q1) will be discussed.

b. When the input to the base of Q1 is high, diode CR1 is forward-biased, thereby clamping the base of Q1 to approximately +0.7 volt. This is sufficient to cut off Q1, resulting in a low output at the collector which is clamped slightly below ground (approximately −0.7 volt) by diode CR2. When the input to the base of Q1 goes low, Q1 switches on, thereby making the output at the collector high (slightly less than +5 volts).

10-4. Test Target Generator Card 1A2A1A3
(fig. 24-21)

a. The test target generator card contains a test target generator circuit and a display gate generation circuit. The functional operation of the test target generation circuit is shown in figure 24-12 and described in paragraph 7-14. The functional operation of the display gate generation circuit is also shown on figure 24-12 and is described in paragraph 7-12. The circuits contained on the test target generator board consist of inverters, gates, flip-flops, and a single-shot. For information pertinent to inverters, gates, flip-flops and single-shots, refer to paragraphs 2-5, 2-7, 2-9, and 2-11 respectively.

b. In figure 24-12, the strobe pulse counter (flip-flops A14B, A14A, A15B and A15A) and the two sections of the processor self-test gate counter (flip-flops A8A, A8B, A4A, A4B, A1A and A1B; and flip-flops A10B, A10A, A11B, and A11A) are shown as rectangular blocks. Also, the four-bit comparator exclusive-OR circuits (A6A, A6B, and A3B; A6D, A6C, and A3A; A7A, A7B, and A3D; and A7D, A7C, and A3C) are each represented by the composite exclusive-OR symbol. The strobe pulse counter is a two stage synchronous ripple

counter. One part of the processor self-test gate counter is a six-stage straight ripple counter, and the other is a four-stage paired synchronous ripple counter whose first two stages are clocked by the output of the sixth stage of the first part. For information pertinent to ripple and synchronous ripple counters, refer to paragraph 2-10. For information pertinent to exclusive-OR circuits, refer to paragraph 2-8.

10-5. Target Video Card 1A2A1A4 (fig. 24-22)

a. The target video card contains the target video selection reshaping, digital delay, and tail trigger generation circuits which are used in the display video interface circuits (fig. 24-12). The functional operation of the target video selection circuit is described in paragraph 7-7. The functional operation of the target video reshaping circuit is described in paragraph 7-8. The functional operation of the digital delay circuit is described in paragraph 7-9. The functional operation of the tail trigger generation circuit is described in paragraph 7-11.

b. The circuits contained on the target video card consist of inverters, gates, flip-flops, and shift registers. In figure 24-12, inverters were sometimes combined with gates for clarity and simplicity. Also the three 8-bit shift registers were combined and represented by a single shift register logic symbol. For information pertinent to shift registers, refer to paragraph 2-10. For information pertinent to inverters, gates, and flip-flops, refer to paragraphs 2-5, 2-7, 2-9, and 2-10, respectively.

10-6. Display Video Card 1A2A1A5 (fig. 24-23)

a. The display video card contains target generation and processor bypass, friend generation, and IFF video reshaping and output circuits which are used by the display video interface circuits (fig. 24-12). The functional operation of the target generation and processor bypass circuit is described in paragraph 7-10. The functional operation of the friend generation circuit is described in paragraph 7-11. The functional operation of the IFF video reshaping and output circuit is described in paragraph 7-13.

b. The circuits contained on the display video card consist of inverters, gates, flip-flops, and single shots. In figure 24-12 inverter A2C was combined with AND A1B for simplicity. For information pertinent to inverters, gates, flip-flops, and single-shots, refer to paragraphs 2-5, 2-7, 2-9, 2-10, and 2-11, respectively.

10-7. Low Level Line Driver Card 1A2A1A6

a. The low level line driver card contains seven inverter (line driver) stages, Q1 through Q7, which are used to shift low inputs from the interface and coder-decoder modules to high outputs for delivery to the associated radar set, interrogator computer, and receiver-transmitter. Since the seven line driver stages are identical, only one (Q1) will be discussed.

b. When the input to the base of Q1 is high, diode CR1 is forward-biased, thereby holding the base at approximately +5 volts and maintaining Q1 in the cutoff state. This results in a low output at the collector of Q1. When the buffered receiver video input goes low, diode CR1 is reversed-biased, allowing Q1 to conduct at some point of the input pulse leading edge. After conduction starts, Q1 rapidly reaches saturation, where it remains for the duration of the low input pulse. The resultant positive-going pulse output at the collector of Q1, buffered receiver video, is made available for external use.

10-8. Buffer Circuit 2 Card 1A2A1A7

a. The buffer circuit 2 card contains radar trigger, mode 4 challenge video, and mode 4 gtc trigger amplitude limiting circuits, radar trigger and mode 4 pretrigger reshaping circuits, and a number of buffer-inverters. The functional operation of the radar trigger amplitude limiting and reshaping circuits and the mode 4 pretrigger reshaping circuit is shown in figure 24-4. The mode 4 challenge video and mode 4 gtc trigger amplitude limiting circuits are shown in figure 24-6. Since the three amplitude limiting circuits are identical (except for impedance matching), only the radar trigger amplitude limiter will be discussed.

b. When the radar trigger input is low (no radar trigger present), diode CR2 is forward-biased and the input to inverter A5B is low. The radar trigger can have any amplitude between +3 and +50 volts and the purpose of the amplitude limiting circuit is to prevent the radar trigger amplitude at the input of inverter A5B from exceeding +5 volts (high), above which the inverter might be damaged. When the radar trigger input begins to go positive, diode CR2 remains conductive until a level corresponding to a high input at inverter A5B is reached. When this occurs, the anode of CR2 is held at that level and the diode cuts off when the radar trigger input is sufficiently positive to reverse-bias the diode. The diode then remains cut off until a point on the trailing edge of the radar trigger conducts, making the input to inverter A5B low until the next radar trigger arrives. Diode CR1, in conjunction with resistor R8 and the —12-volt supply, clamps the cathode of diode CR2 slightly below ground to insure that the input to inverter A5B is low when there is no radar trigger present.

Diode CR1 also prevents any radar trigger negative overshoots.

c. Aside from the amplitude limiting circuits, the buffer circuit 2 card consists of inverters and singleshots. For information pertinent to inverters and single-shots, refer to paragraphs 2-5 and 2-11.

10-9. Buffer Circuit 1 Card 1A2A1A8 (fig. 24-26)

a. The buffer circuit 1 card contains the fault indication circuit logic, a mode 4 time decoded video amplifier, a processor self-test decision cancellation circuit, and a number of buffer-inverters. The functional operation of the fault indication circuits is shown in figure 24-13 and described in chapter 8. The function of the mode 4 time decoded video amplifier circuit is shown in figure 24-12. The functional operation of the processor self-test decision cancellation circuit, also shown in figure 24-12, is described in paragraph 7-18.

b. Mode 4 time decoded video amplifier Q5 (figure 24-12) was shown as a buffer-inverter for simplicity. When the mode 4 time decoded video input to the base of Q5 is low (no mode 4 time decoded video pulse present), Q5 conducts, and the output at its collector is high. When a positive-going time decoded video pulse arrives, Q5 is cut off and remains cut off for the duration of the pulse. The resultant negative-going (low) output at the collector of Q5 is applied as one input to OR A7D. Diode CR2 changes the output of Q5 at approximately —0.7 volt.

c. Inverters A3A, A3D, A3B and A3C were shown combined with their associated lamp drivers (Q1 through Q4, respectively) in figure 24-14, and inverter A4D was shown combined with OR A2A for clarity and simplicity. Each lamp driver, when conductive, supplies a ground path (low) for a corresponding FAULT indicator lamp on the synchronizer front panel.

d. The integrated circuits on the buffer circuit 1 card are inverters, gates, and an infinitely retriggerable single-shot. For information pertinent to inverters, gates, and single-shots, refer to paragraphs 2-5, 2-7, and 2-11.

Section II. CODER-DECODER MODULE 1A2A2

10-10. General (fig. 24-27)

The coder-decoder module contains eight printed wiring cards whose circuits provide the challenge encoding functions described in chapter 5 and the reply decoding functions described in chapter 6. The wiring interconnections between the printed wiring cards and the interconnections to and from the synchronizer chassis through the module connectors are shown in figure 24-27. The printed wiring cards except level shifter card 1A2A2A1, are described individually in the following paragraphs. The level shifter card is identical to (and interchangeable with) level shifter card 1A2A1A2, and is described in paragraph 10-3.

10-11. Correct Code 1 Card 1A2A2A2 (fig. 24-28)

The correct code 1 card contains gates and inverters which are used as sif reply code pulse detectors in the reply decoding circuits. The functional operation of these circuits is shown in figure 24-9 and described in paragraph 6-6. However, on figure 24-9, inverter logic elements were combined with gate logic elements on a functional basis for clarity and simplicity. For information pertinent to the operation of inverters and gates, refer to paragraphs 2-5 and 2-8.

10-12. Correct Code 2 Card 1A2A2A3 (fig. 24-29)

The correct code 2 card contains circuits which are used by the reply decoding circuits for sif code pulse decoding, bracket decoding, and correct code pulse generation. The functional operation of the code pulse decoding circuit is shown in figure 24-9 and described in paragraph 6-6. The functional operation of the bracket decoding circuit, also shown in figure 24-9 is described in paragraph 6-7. However, in figure 24-9 inverter logic elements are sometimes combined with gate logic elements on a functional

basis for clarity and simplicity. For additional information pertinent to the circuits contained on the correct code 2 card, refer to paragraphs 2–5, 2–7, 2–9, and 2–10.

10–13. Coder Card 1A2A2A4
(fig. 24–30)

a. The coder card contains seven of the challenge encoding circuits described in chapter 5: sif enabling circuit, sif P1 trigger selection circuit, sif challenge/reply enabling circuit, isls timing counter, isls pulse generation circuit, isls gate generation circuit, and 5-mc clock generation circuit. The coder board also contains mode C interlacing and mode C video selection circuits which are not used in the present design. The functional operation of the sif enabling circuit is shown in figure 24–6 and described in paragraph 5–5. The functional operation of the sif P1 trigger selection and sif challenge/reply enabling circuits, also shown in figure 24–6, are described in paragraph 5-9. The functional operation of the isls timing counter, isls pulse generation, isls gate generation, and 5-mc clock generation circuits, also shown in figure 24–6, are described in paragraph 5–10.

b. The circuits contained in the coder board consist of inverters, gates, and flip-flops. For information pertinent to inverters, gates, and flip-flops, refer to paragraphs 2–5, 2–7, and 2–9, respectively. The isls timing counter (flip-flops A7B, A7A, A11B, A11A and A15B) is shown in figure 24–6 as a rectangular block. This counter is a paired-synchronous ripple counter. For information pertinent to the operation of paired-synchronous ripple counters, refer to paragraph 2–10.

10–14. Challenge Video Card 1A2A2A5
(fig. 24–31)

a. The challenge video card contains nine of the challenge encoding circuits which are shown in figure 24–6 and described in chapter 5. The functional operation of the sif pretrigger selection and the self-test and sif pretrigger reshaping circuits is described in paragraph 5–6. The functional operation of the sif P1 and P3 reshaping, sif P2 reshaping, mode 4 challenge video reshaping, gtc trigger generation, and challenge video output circuits is described in paragraph 5–12. The functional operation of the mode 4 enabling and mode 4 sync pulse counter circuits is described in paragraph 5–11. The transponder suppression gate generation circuit is not used in the present design.

b. The circuits contained on the challenge video card consist of inverters, gates, flip-flops, and single-shots. For information pertinent to inverters, gates, flip-flops, and single-shots, refer to paragraphs 2–5, 2–7, 2–9 and 2–11. In figure 24–6, some inverters are combined with gates for clarity and simplicity. The mode 4 sync pulse counter (flip-flops A4B and A4A) is a two-stage synchronous counter. For information pertinent to the operation of synchronous counters, refer to paragraph 2–10.

10–15. Reply Video Card 1A2A2A6
(fig. 24–32)

a. The reply video card contains circuits which are used by the reply decoding circuits to decode transponder replies and by the challenge encoding circuits to time share delay line module 1A2A5 for challenge encoding and reply decoding. The functional operation of the delayed self-test pretrigger selection and delay line time-sharing control circuits is shown in figure 24–6 and described in paragraph 5–7. The functional operation of the delay line input selection and delay line driver circuits, also shown in figure 24–6, are described in paragraph 5–8; however, in figure 24–6, the delay line driver (Q2) is represented by a triangular logic symbol. The functional operation of the delay line driver is provided in *c* below. The functional operation of the video amplifier, 0.25 μsec pulse width discriminator, and receiver video reshaping circuits is shown in figure 24–9 and described in paragraph 6–5; however, in figure 24–9, the video amplifier (Q1) is represented by a triangular logic symbol. The functional operation of the video amplifier is provided in *d* below. The functional operation of the delay line buffers, triple pulse decoding, and triple pulse decoded video reshaping circuits, also shown in figure 24–9, is described in paragraph 6–8.

b. The logic circuits contained on the reply video card consist of inverters, gates, flip-flops, and single-shots. For information pertinent to the operation of inverters, gates, flip-flops, and single-shots, refer to paragraphs 2–5, 2–7, 2–9, and 2–11.

c. Delay line driver Q2 receives positive-going input pulses from OR A2B through coupling capacitor C7 and base current limiting resistor R11. Diode CR1 is a dc resistor diode for C7. The base circuit is returned to −12 volts, from which the emitter is biased positively by the 0.7-volt forward-biased voltage drop across diode CR2. The collector load is a parallel combination of collector return resistor R13 and the characteristic impedance of delay

line 1A2A5 (nominally also 180 ohms). Between positive-going pulses from OR A2B, the emitter bias from CR2 holds Q2 cut off. During each pulse, Q2 conducts heavily delivering the pulse as a negative-going 0.0 μsec delay line input pulse with an amplitude greater than 12 volts and a rise time less than 20 nanoseconds. Diode CR3 absorbs any positive-going overshoots at the trailing edges of the 0.0-μsec output pulses, such as might be caused by the inductive component of the delay line input impedance. Capacitor C8 is a decoupling capacitor which prevents the pulsed conduction of Q2 from appearing on the +5-volt supply line.

d. Video-amplifier Q1 receives the positive-going receiver video pulses from the receiver-transmitter through an input network in which the parallel combination of resistor R5 and video level adjustment R6 provides a 75-ohm effective cable termination, coupling capacitor C3 blocks the difference in dc potentials between the receiver video input line and the base circuit of Q1, and the parallel combination of resistor R8 and capacitor C4 sharpens the leading and trailing edges of each pulse. Before each receiver video pulse, Q1 is heavily conductive because of the base current supplied through resistors R7 and R8, and the voltage at its collector is approximately +4.5 volts (high). During each receiver video pulse large enough to be considered an actual transponder reply pulse (determined by the setting of R6), Q1 is cut off. With Q1 cut off, the input terminals of OR A6A and 0.25 μsec delay line DL1 in the pulse width discriminator circuit are driven low by the connection to −12 volts through resistor R9. If a receiver video pulse of lower amplitude than an actual transponder reply pulse arrives, Q1 is not completely cut off, and the pulse width discriminator inputs are not driven low enough although the pulse appears negative-going at the collector of Q1, it does not go low completely cut off, and its collector does not go low enough to produce a high output from OR A6A or, 0.25 μsec later, from inverter A3A. The setting of R6 thus determines the receiver video threshold level above which all pulses will be accepted for pulse width discrimination, and below which the pulses will be rejected as not valid transponder reply pulses.

10–16. I/p and Emergency Code Card 1A2A2A7

(fig. 24–33)

a. The i/p and emergency code card contains the reply decoding circuits used to decode sif i/p or emergency replies. The functional operation of the i/p and emergency decoding circuits is shown in figure 24–9 and explained in paragraph 6–10. However, in figure 24–9 the seven-stage short/long counter is shown as a rectangular block whose outputs are "air lined" to AND decoding gates A8 and A9, and inverters A3C and A13B have been combined with gates A3D and A13D, respectively, for clarity and simplicity. The counter is a paired synchronous ripple counter whose first five stages (flip-flops A5A, A5B, A4A, A4B and A1A) constitute the short count portion, and whose last two stages (flip-flops A1B and A2A), in conjunction with the first five stages, constitutes the long count portion. For information pertinent to inverters, gates, and flip-flops, refer to paragraphs 2–5, 2–7, and 2–9. For information pertinent to the operation of paired-synchronous ripple counters, refer to paragraph 2–11.

10–17. Coder-Decoder Self-Test Card 1A2A2A8

(fig. 24–34)

a. The coder decoder self-test card contains circuits which test the operation of the challenge encoding and reply decoding circuits and a fault accumulator circuit. The functional operation of the challenge encoding self-test circuit is shown in figure 24–6 and described in paragraph 5–13. The functional operation of the reply decoding self-test circuit is shown in figure 24–8 and described in paragraph 6–11. The functional operation of the fault accumulator circuit is shown in figure 24–6 and described in paragraph 5–14. On figure 24–6, inverter A2C is shown combined with AND A2D and, on figure 24–9, ANDs A11A and A11B are shown combined for simplicity.

b. The circuits contained in the coder-decoder self-test card consist of inverters, gates, and flip-flops. For information pertinent to inverters, gates, and flip-flops, refer to paragraphs 2–5, 2–7, and 2–9.

Section III. POWER SUPPLY MODULE 1A2A3

10–18. General

(fig. 24–35)

The power supply module contains three printed wiring cards, two of which have attached heat-sink plates for the parts which require heat-sinking. These cards provide the +12-volt, −5-volt, and −12-volt supplies for synchronizer operation as described in chapter 9. The wiring interconnections

between the cards and the filter parts within the power supply module connector are shown in figure 24–35. The three cards are described individually in the following paragraphs.

10–19. +12-Volt Regulator Card 1A2A3A1

(fig. 24–36)

a. The +12-volt regulator receives the +28-volt synchronizer power input and supplies a +12-volt output to the interface and coder-decoder modules. The +12-volt output is also supplied to the +5-volt regulator card, and a current limited +12-volt output is supplied to the −12-volt inverter card. The functional operation of the +12-volt regulator is shown in figure 24–15 and described in paragraph 9–2. However, in figure 24–15, circuits were combined and represented by logic symbols for clarity and simplicity.

b. The +28-volt input (fig. 24–36) is switched through regulator switch Q1 to flywheel circuit L1, C3, CR1 at a 10-kc rate in response to control pulses from switch driver Q2. The duration of the drive pulses, and therefore the on–off ratio of regulator switch Q1, is determined by the active state duration of voltage-controlled single-shot Q8, Q9, Q10, Q11 and Q12 which is triggered by 10-kc triggers supplied by the −12-volt inverter card. The active state duration of the single-shot is controlled by the error voltage output produced by differential amplifier Q14, in response to variations in the current limited +12-volt output voltage. The on–off ratio of Q1 is such that the 28-volt input is converted to +12 volts at the output of the flywheel circuit. The error voltage output of differential amplifier Q14 is the amplified result of a comparison between the fixed +5-volt reference developed across Zener diode VR5 and a sample of the +12-volt output developed across +12-volt adjustment potentiometer R27 which sets the conduction of duration control Q12 so that the active state to quiescent state ratio of the single-shot results in an output of +12 volts. That is, since regulator switch Q1 is on when the single-shot is in its quiescent state (switch drive Q2 on), the output voltage is reduced to +12 volts by increasing the active state duration, or is increased to +12 volts by decreasing the active state duration depending on the error voltage output of the differential amplifier. The +5-volt reference developed by Zener diode VR5 is also used on the +5-volt regulator card,

c. Voltage-controlled single-shot Q8, Q9, Q10, Q11 and Q12 is in the quiescent state when Q9 is on and Q10 is off. This condition exists just prior to a 10-kc trigger from the −12-volt inverter card. When a 10-kc trigger arrives, Q11 is turned on for the duration of the trigger turning off Q9, which turns on Q10 and thereby starts the active state. The single-shot remains in this state until capacitor C6 discharges sufficiently to allow Q9 to turn on, at which time Q10 is turned off returning the single-shot to the quiescent state. Since duration control Q12 is in the discharge path of capacitor C6, the time required for the capacitor to discharge to the point where Q9 turns on is determined by the conduction of Q12, which is controlled by the error voltage output of differential amplifier Q14.

d. When voltage-controlled single-shot Q8, Q9 Q10, Q11, and Q12 is in the quiescent state (Q9 on), buffer Q7 is cut off, and control amplifier Q5 is turned on. With Q5 on, switch driver Q2 is turned on, turning on regulator switch Q1. With Q1 on, the +28-volt input is passed to flywheel circuit L1, C3, CR1. When the single-shot is triggered into the active state (Q9 off) by a 10-kc trigger, buffer Q7 is turned on, cutting off control amplifier A5 and switch driver Q2. This cuts off regulator switch Q1 and interrupts the current flowing to the flywheel circuit. In this way, the average voltage applied to the flywheel circuit, determined by the on-off ratio of regulator switch Q1, establishes the output voltage.

e. If the +12-volt output rises above −12 volts the rise is sensed across potentiometer R27. The resultant increase in positive potential on the base of one half of the differential amplifier (Q14A) increases its conduction and, since the two halves share a common unbypassed emitter resistance (R29), the conduction of the other half (Q14B) is reduced by a corresponding amount. When the conduction of Q14B is reduced, the error voltage output of the difference amplifier becomes more positive which reduces the conduction of duration control Q12. This increases the discharge time of capacitor C6, thereby increasing the active state duration of single-shot Q8–Q12 and causing a corresponding increase in the off time of regulator switch Q1. When the off time of Q1 is increased, the average current applied to the flywheel circuit is decreased, thereby decreasing the output voltage. If the ±12-volt output falls below +12 volts, the drop in voltage is sensed across R27 and results in a less positive error voltage output from differential amplifier Q14. This increases the conduction of duration control Q12, which decreases the active state duration of the single-shot. A decrease in active state duration results in a decrease in the off time

of regulator switch Q1 and a corresponding increase in output voltage.

10-20. +5-Volt Regulator Card 1A2A3A2
(fig. 24-37)

The +5-volt regulator receives +12 volts from the +12-volt regulator card and supplies a regulated +5-volt output to the interface coder-decoder, and timing modules. The +5-volt regulator card also receives a +5-volt Zener reference voltage from the +12-volt regulator card and 10-kc triggers from the −12-volt inverter card. The functional operation of the +5-volt regulator board is shown in figure 24-15 and described in paragraph 9-3. However, in figure 24-15, circuits were combined and represented by logic symbols for clarity and simplicity. Except for voltage levels and reference designations, the circuit operation of the +5-volt regulator card is the same as that of the +12-volt regulator card described in paragraph 10-19.

10-21. −12-Volt Inverter Card 1A2A3A3
(fig. 24-38)

a. The −12-volt regulator card receives current limited +12 volts from the +12-volt regulator card and supplies −12 volts to the interface and coder-decoder modules. The −12-volt regulator card also supplies 10-kc triggers to the +12-volt and +5-volt regulator cards. The functional operation of the −12-volt regulator card is shown in figure 24-15 and described in paragraph 9-4. However, in figure 24-15 circuits were combined and represented by logic symbols for clarity and simplicity.

b. Initially, when +12 volts is first applied to the emitters of inverters Q1 and Q2, one inverter conducts more than the other because of slight circuit unbalance or the presence of noise. Let us assume that the conduction of inverter Q1 is initially slightly greater than the conduction of Q2. The greater conduction of Q1 through the primary of transformer T1 makes the top of the winding (pin 1) more positive than the bottom (pin 4). This results in a more positive potential at the top of the base feedback winding (pin 3) than at the bottom (pin 2). The more positive potential at pin 3 reduces the conduction of Q2 and the less positive potential at pin 2 increases the conduction of Q1, which makes pin 1 of the primary still more positive. This action continues until Q2 is cut off and Q1 is saturated. With Q1 saturated, the current flowing through the primary of T1 begins to approach the core saturation point. When this occurs, the voltage across the base feedback winding (pins 2 and 3) decreases. As the voltage at pin 2 becomes more positive, Q1 comes out of saturation, at which time the current flowing through the primary is reduced, which further reduces the voltage across the base feedback winding and thus further reduces the conduction of Q1. As this action progresses, a point is reached at which Q2 begins to conduct. The action then continues until Q1 is cut off and Q2 is saturated, at which time saturation of the core is again approached and the resultant decrease in secondary current repeats the cycle.

c. The action described in *b* above continues as long as +12 volts is applied to the emitters of Q1 and Q2 and results in a 10-kc square wave at the primary of transformer T1. The 10-kc square wave is rectified by diodes CR5 and CR6 and filtered by capacitors C2 and C3 to produce the −12-volt output. The positive excursions of the 10-kc square wave are also differentiated and buffered by trigger generator Q4 to produce positive-going 10-kc triggers which are supplied to the +12-volt and +5-volt regulator cards.

Section IV. TIMING MODULE 1A2A4

10-22. General
(fig. 24-39)

The timing module contains three printed wiring cards whose circuits provide the timing circuit functions shown in figure 24-4 and described in chapter 4. The wiring interconnections between these cards and the interconnections to and from the synchronizer chassis through the module connector are shown in figure 24-39. The printed wiring cards are individually described in the following paragraphs.

10-23. 10-Mc Clock and Counter A Card 1A2A4A1
(fig. 24-40)

The 10-mc clock and counter A card contains a 10-mc clock pulse generator, the first five stages of the 13-stage pretrigger timing counter, a counter control flip-flop, and the mode 4 pretrigger and processor start pretrigger decoding circuits. The functional operation of these circuits is shown in figure 24-4 and described in chapter 4. However,

in figure 24-4, circuits were condensed on a functional basis for clarity and simplicity. As a result, the 10-mc clock pulse generator was represented by two triangular logic symbols, and the first five stages of the pretrigger timing counter were shown as part of the overall counter by means of a rectangular block. The mode 4 and processor start pretrigger decoding circuits were shown as single AND gates with inputs "airlined" from the counter. This paragraph supplies supplementary information necessary to complete the description given in paragraph 2-3.

a. 10-mc Clock Pulse Generator. The 10-mc clock pulse generator consists of crystal-controlled Pierce oscillator Y1, Q1 and buffer Q2. The 10-mc sine wave signal generated in parallel resonant (tank) circuit C4, L1 at the collector of Q1 is coupled through capacitor C5 to the base of buffer Q2. The base bias for Q2 is established by resistor R2 and diode CR1, which clips the negative portion of the 10-mc sine wave at approximately −0.5 volt. This is sufficient to cut off Q2 during the negative half cycles of the sine wave signal. When the 10-mc sine wave swings positive, Q2 conducts and quickly reaches saturation for the duration of the positive half cycle. The resultant negative-going 10-mc square wave signal at the collector of Q2 ($\overline{10\text{ mc clock}}$) is further squared and inverted by inverter A4A to clock the pretrigger timing counter. It is also squared and inverted by inverter A4B for delivery to the coder-decoder module.

b. Pretrigger Timing Counter Stages. The five pretrigger timing counter stages on the 10-mc clock and counter A board are 2:1 countdown (toggling) flip-flop A2A and four-stage synchronous counter A3B, 3A3, A5 and A6. The toggling flip-flop counts 10-mc clock pulses from the 10-mc clock pulse generator and its output (2^0) clocks the four synchronous counter stages. The output of flip-flop A6 is supplied to the counter B board, where it clocks the second set of four synchronous counter stages of the pretrigger timing counter. For information pertinent to the operation of synchronous ripple counters, refer to paragraph 2-10. The Q and $\overline{Q}$ outputs of flip-flops A3B, A3, A5, and A6, in conjunction with the additional count inputs from the counter B board, are used to time the $\overline{\text{mode 4 pretrigger}}$ and $\overline{\text{processor start pretrigger}}$ outputs.

c. Pretrigger Decoding Circuits. The $\overline{\text{mode 4 pretrigger}}$ is generated in expanded AND decoding circuit A8A, A8B and A7B. The $\overline{\text{processor start pretrigger}}$ is generated in expanded AND decoding circuit A9A, A9B and A7A. Four of the 12 inputs required to decode the $\overline{\text{mode 4 pretrigger}}$ are applied to AND A8A and four are applied to AND A8B. The outputs of A8A and A8B are dot-ANDed and applied to the expander input of expandable AND A7B which also receives the remaining four decoding inputs. When the pretrigger timing counter reaches a count of 142, all inputs to ANDs A8A, A8B and A7B are high for a duration of 0.2 μsec, and a $\overline{\text{mode 4 pretrigger}}$ is generated. The processor start pretrigger decoding circuit operates in the same manner, with a different decode, however. For information pertinent to the operation of expanded AND circuits, refer to paragraph 2-8.

10-24. Counter B Card 1A2A4A2
(fig. 24-41)

a. The counter B card contains the last eight stages of the pretrigger timing counter and the self-test and sif pretrigger decoding circuits. The functional operation of these circuits is shown in figure 24-4 and described in chapter 4. However, in figure 24-4, circuits were condensed on a functional basis for clarity and simplicity. As a result, the last eight stages of the pretrigger timing counter were shown as part of the overall counter by means of a rectangular block, and the self-test and sif pretrigger decoding circuits were shown as single AND gates with inputs "airlined" from the counter.

b. The eight counter stages contained on the counter B card (flip-flops A1A, A1B, A5, A9, A4A, A4B, and A8) make up the last two four-stage synchronous counters of the pretrigger timing counter. The first four-stage synchronous counter is contained on the 10-mc clock and counter A board. The Q and $\overline{Q}$ output of the eight counter stages, in conjunction with the additional count inputs from the 10-mc clock and counter A board, are used to time the $\overline{\text{self-test pretrigger}}$ and $\overline{\text{sif pretrigger}}$ outputs. The $\overline{\text{self-test pretrigger}}$ is generated in expanded AND decoding circuit A3A, A3B and A7B, and the $\overline{\text{sif pretrigger}}$ is generated in expanded AND decoding circuit A2A, A2B and A7A. For information pertinent to the operation of expanded AND circuits, refer to paragraph 2-8. For information pertinent to the operation of synchronous ripple counters, refer to paragraph 2-10.

c. The particulars count inputs applied to the decoding circuits, and therefore the particular

timing of the self-test pretrigger and the sif pretrigger, are determined by the printed wiring jumpers within program connector P1. These jumpers are indicated schematically in figure 24-41.

10-25. Timing Self-Test Card 1A2A4A3
(fig. 24-42)

The timing self-test card contains the timing self-test circuit and the radar trigger test circuit shown in figure 24-4 and described in paragraphs 4-3 and 4-4. The circuits contained on the timing self-test board consist of inverters, gates, flip-flops, and infinitely retriggerable single-shots. For information pertinent to the operation of inverters, gates, flip-flops, and single-shots, refer to paragraphs 2-5, 2-7, 2-9, and 2-11.

Section V. MINOR COMPONENTS

10-26. Delay Line Module 1A2A5
(fig. 24-16)

The delay line module is time shared between the challenge encoding circuits (chapter 5) and the reply decoding circuits (ch. 6). It is shown functionally in figure 24-6 and described in paragraphs 5-8 and 6-6. The module consists of tapped 21.0-μsec lumped-constant delay line 1A2A5DL1 and a supporting metal frame that provides for plug-in attachment to the synchronizer chassis. The wiring connections from the solder terminals of 1A2A5DL1 to module connector 1A2A5P1 are included in the overall synchronizer schematic diagram, figure 24-16.

10-27. General
(fig. 24-16)

This filter is a sealed, nonrepairable power line filter at the 28-volt input to the power supply and power distribution circuits (ch. 9). The wiring connections to its terminals are included in the overall synchronizer schematic diagram (fig. 24-16).

10-28. General
(fig. 24-16)

This component board provides the physical support for the two meter multiplier resistors, the shunt resistor, and the meter calibration adjustments described in paragraph 9-5. Its terminal connections are included in the overall synchronizer schematic diagram (fig. 24-16).

CHAPTER 11

GENERAL MAINTENANCE INFORMATION

NOTE

This part of the manual contains information pertinent to DS, GS, and depot maintenance. The amount of repair that can be performed by units having DS, GS, and depot maintenance responsibility is limited only by the tools, test equipment, and replacement parts that are available, and the skill of the repairman.

Section I. INTRODUCTION

11–1. Purpose

a. General. The information contained in this chapter and in chapters 12 through 23 of this manual is intended to aid the repairman in locating and correcting equipment trouble causing abnormal operation and then checking the serviceability of repaired equipment in a minimum amount of time. This manual assumes that a synchronizer or synchronizer subassembly received from the using activity is defective. For information pertinent to localizing an IFF set trouble to the synchronizer, refer to TM 11–5895–687–12 and TM 11–5895–687–35–1.

b. Locating Trouble. A synchronizer trouble is first sectionalized to one of the six major functional circuits by using one of the overall troubleshooting charts. Then it is localized to a printed wiring card by using the troubleshooting chart for the circuit group. After the trouble has been localized to a defective printed wiring card it is isolated to the defective part by using the troubleshooting chart for the printed wiring card.

(1) *Overall troubleshooting charts.* The overall troubleshooting charts are based upon operation of the synchronizer as part of the functional equivalent (hot mockup) of an operational IFF set. There are three overall troubleshooting charts, based on three different types of external fault indications and the corresponding procedures required to sectionalize the trouble to a major functional circuit. They are as follows:

(*a*) *Single fault indication troubleshooting chart.* This troubleshooting chart assumes that, when a defective synchronizer is connected into an operational IFF set, one, (and only one) front panel FAULT lamp lights. Since most of the circuits in the synchronizer are self-tested, the majority of troubles result in a single FAULT lamp indication.

(*b*) *No fault indication troubleshooting chart.* This troubleshooting chart assumes that when a defective synchronizer is connected into an operational IFF set, no fault indicators light. This chart primarily handles faults in those circuits which are outside the self-test loops of all modules (level shifters, line drivers, etc).

(*c*) *Multiple fault indication troubleshooting chart.* This troubleshooting chart assumes that when a defective synchronizer is connected into an operational IFF set, two or more front panel FAULT lamps light. This chart handles those cases when an equipment trouble is detected by more than one self-test circuit.

(2) *Major functional circuit troubleshooting charts.* A functional circuit troubleshooting chart is provided in each functional circuit troubleshooting and repair chapter. Each chart assumes that the trouble is located within the circuit, and contains troubleshooting information which localizes the trouble to a defective printed wiring card.

(3) *Printed wiring card troubleshooting charts.* A separate troubleshooting chart is provided for each card in the subassembly troubleshooting and repair chapter. Each chart assumes that the card contains a de-

fective part, and gives the procedures which isolate the trouble to that part.

c. Correcting Trouble. Measures for correcting a trouble localized by a troubleshooting chart are given in the troubleshooting chart, unless they have already been given elsewhere. In such cases, their locations are referenced. Information for the adjustment of each control is provided in the troubleshooting and repair chapter for the circuit in which the control is located.

d. Checking Serviceability. Testing procedures which check the serviceability of repaired synchronizer subassemblies are provided in the circuit troubleshooting and repair chapters. Procedures for testing the entire synchronizer are provided in chapters 22 and 23.

11–2. Troubleshooting Techniques

a. General. To be effective, troubleshooting must be systematic. It is seldom possible to observe a symptom of trouble and immediately diagnose the cause. Generally, it will be necessary to perform a sequence of operational checks, observations, and measurements before the cause of a trouble is revealed. If the proper sequence is followed, the trouble will be traced first to a major functional circuit, then to a printed wiring card, and finally to the defective part. The sequence of steps is commonly referred to as sectionalization, localization and isolation of trouble.

b. Sectionalization. The first aim in troubleshooting is to sectionalize the trouble to a major functional circuit group. Sectionalization can be accomplished through visual checks (FAULT lamp indications and voltmeter indication), operational checks (mode changes), and measurements contained in the overall troubleshooting charts.

c. Localization. After the trouble has been sectionalized to a functional circuit by the applicable overall troubleshooting chart, a reference will be supplied to the functional circuit troubleshooting chart. The referenced troubleshooting chart will localize the trouble to a printed wiring card.

d. Isolation. After the trouble has been localized to a printed wiring card, the functional circuit troubleshooting chart references the applicable printed wiring card troubleshooting chart which will isolate the trouble to a defective part or stage on the printed wiring card.

11–3. Troubleshooting Data

a. General. In addition to the troubleshooting charts, other troubleshooting data are provided to help the repairman rapidly locate trouble. A list of the specific troubleshooting data which would help locate troubles in each particular functional system is given in the *reference data* paragraph in the first section of each functional system troubleshooting and repair chapter. The following types of troubleshooting data are supplied and should be consulted when necessary.

b. Block Diagrams. The block diagrams give the functional interrelationships of the functional circuits constituting the synchronizer. Each block on the overall block diagram represents a functional circuit which is represented by its own block and/or logic diagrams.

c. Overall Schematic Diagram. The synchronizer schematic diagram (fig. 24–15) shows the interconnections between modules and chassis mounted components. It also shows inputs from and outputs to other units of the IFF set and the associated radar set. This diagram will be useful when tracing trouble between modules.

d. Module Schematic Diagrams. The module schematic diagrams show the interconnections between the printed wiring cards in each module, as well as inputs from and outputs to other synchronizer modules and other units of the IFF set. These diagrams will be useful in localizing the trouble to a printed wiring card when performing the functional circuit troubleshooting procedures.

e. Printed Wiring Card Schematic Diagrams. The printed wiring card schematic diagrams show all of the circuitry contained on each printed wiring card. These diagrams will be useful in isolating a trouble to a defective part when performing the printed circuit board troubleshooting procedures. The printed wiring pattern and location of parts on each printed wiring card are shown adjacent to the card schematic diagram.

f. Logic Diagrams. The logic diagrams show functional circuit relationships in a manner that covers schematic details by symbolizing their purposes and effects so that a qualified repairman familiar with the contents of chapter 2 can read the circuit operation "at a glance." Although simplified, each logic diagram retains all the troubleshooting information, (test jacks, card pins, and adjustments) necessary to isolate a trouble to a defective stage or functionally integral group of

stages within the circuit represented by the logic diagram. The logic diagrams are discussed in chapters 4 through 9 of this manual.

g. Printed Wiring Card Layout Diagrams. The printed wiring card layout diagram adjacent to each printed wiring card schematic diagram shows the physical appearance, placement of parts, and printed wiring configuration of the printed wiring card. These diagrams will be useful in physically locating points of measurement and parts suspected of being defective. Also, when a part must be replaced, these diagrams provide the information necessary to insure that the replacement part is correctly installed.

h. Parts Location Illustrations. The parts location illustrations physically locate the parts mounted on the synchronizer chassis, the printed wiring cards within the modules, and the interconnection jacks and plugs. Also, these diagrams physically locate all adjustments and various points of measurement referenced in the troubleshooting and repair chapters.

i. Waveform Illustrations. The waveform illustrations show the normal waveforms observed with the specified conditions at all the points where wave-form observations are required in the various troubleshooting charts.

j. Voltage and Resistance Charts. The voltage and resistance charts supply voltage and resistance measurements at all printed wiring card pins. The voltage measurements will be useful as an aid in isolating a trouble to a defective part. The resistance measurements will be useful in checking a repaired printed wiring card for short circuits before installing the board in its module. The resistance charts for the module and chassis connector pins will similarly be useful in checking for short circuits in a repaired module before installing the module in its position on the chassis, or in a repaired synchronizer before applying power.

k. Normal Indications at Test Jacks. The normal indications at the test jacks in each functional circuit are contained in section I of the corresponding troubleshooting and repair chapter. This information will be useful in localizing and isolating a trouble.

l. Other Maintenance Information. The information referenced in the following chart will aid the repairman in maintaining the synchronizer. All of the references are to TM 11-5895-687-35-1.

Maintenance information	*Paragraph*
Reference designations	5-9
Parts locations	5-10
Replacing modules	5-11
Replacing printed wiring cards	5-12
Replacing integrated circuits	5-13
Replacing piece parts	5-14
Cable check and repair	5-16
Intermittents	5-19
Power short circuits	5-20
Transistor testing	5-21
Removal and replacement of conformal coating	5-22
Soldering techniques	5-23
Repair of printed wiring	5-24
The hot mockup	5-25

11-4. Waveform Analysis

a. Waveforms may be observed at all points within the synchronizer by using Oscilloscope AN / USM-281A. Detailed instructions for operating that oscilloscope are contained in TM 11-6625-1703-15. The normal waveforms at all points specified in the troubleshooting charts of this manual are shown in the printed wiring card troubleshooting and repair chapter (ch. 20), where a separate waveform illustration is provided for each printed wiring card. By comparing the observed waveforms with these normal waveforms in the sequence specified in the troubleshooting charts, a trouble can be quickly located.

b. Use Oscilloscope AN / USM-281A and follow the operating instructions in TM 11-6625-1703-15 to observe the specified waveforms. Before comparing an observed waveform with the normal waveform shown, carefully read the notes on the waveform illustration and exactly duplicate the conditions under which the normal waveform was obtained. If an observed waveform does not closely resemble the normal waveform, trouble is indicated.

c. A departure from the normal waveform indicates trouble in or near the stage producing the abnormal waveform, as defined by the troubleshooting chart. When a waveform is abnormal, the stage producing the waveform is not necessarily defective: the cause may be an abnormal or missing signal from another stage, or may be a short or open circuit in a later stage which receives the waveform as an input. It is therefore advisable to check for the presence of proper inputs to the stage, as directed in the troubleshooting chart. Then, if all inputs are normal, a check should be made for a defect at each destination of the waveform. When a trouble has finally been isolated to a stage, then if the stage is an integrated circuit with no associated discrete parts, replace it. If the stage has associated discrete parts, check the discrete parts before replacing the integrated circuit. If the stage is not an integrated circuit, check each of its parts and replace the one which is defective.

11-5. Voltage and Resistance Measurements

a. Voltage and resistance measurements may be made at all points within the synchronizer with Multimeter AN / PSM-6B. Detailed instructions for operating that multimeter are contained in TM 11-6625-475-10. Resistance measurements obtained at the rear connectors of a properly operating synchronizer are given in the synchronizer overall troubleshooting and repair chapter (ch. 12). Resistance measurements obtained at the bottom connector pins of properly operating synchronizer modules are given in the module troubleshooting and repair chapter (ch.19). Voltage and resistance measurements obtained at the printed wiring card pins in a properly operating synchronizer are given in the printed wiring card troubleshooting and repair chapter (ch. 20), where separate voltage measurement chart and resistance measurement charts are provided for each card.

b. Use Multimeter AN / PSM-6B and follow the operating instructions in TM 11-6625-475-10 to measure voltages or resistances at the connector pins listed. Measure the printed wiring card pin voltages with the card extended from its module on an extender board, and with the synchronizer connected into the "hot mockup" and turned on. The highest voltage at any point within the synchronizer is the nominal 28-volt dc input from the hot mockup power supply. Take resistance measurements only when the synchronizer is completely disconnected from the hot mockup.

Section II. TOOLS AND TEST EQUIPMENT REQUIRED FOR MAINTENANCE

11-6. Tools

The following tools are required for DS, GS, and depot maintenance of the synchronizer:

Quantity	*Tool*
1	Repair Kit, Printed Wiring Board MX-772 / U.
1	Tool Kit, Electronics Equipment TK-100 / G.
1	Tool Kit, Electronics Equipment TK-101 / G.
1	Tool Kit, Electronics Equipment TK-105 / G.
1	Heat Gun, Master Appliance Model HG-501L.
	Tools, Extraction, Insertion, and Crimping.

11-7. Test Equipment

The following test equipment is required for DS, GS, and depot maintenance of the synchronizer.

Test equipment	*Common name*	*Literature*
Test Facilities Set AN / TPM-24(V)3	Test facility set	TM 11-6625-2398-15-3
Radar Test Set AN / UPM-98A	Radar test set	TM 11-6625-403-15-1
Simulator, Test Set AN / APM-245A	Mode 4 word generator	TM 11-6625-1711-15
Oscilloscope AN / USM-281A, or equivalent.	Oscilloscope	TM 11-6625-1703-15
Voltmeter, Electronic, ME-202B, or equivalent.	Differential voltmeter	TM 11-6625-537-15-1
Multimeter AN / PSM-6B or equivalent	Multimeter	TM 11-6625-475-10
Counter, Electronic, Digital Readout AN / USM-207A.	Counter	NAVSHIPS 0969-125-0010
Power Supply PP-2953A / U	Power supply	TM 11-6130-233-12

CHAPTER 12

OVERALL SYNCHRONIZER TROUBLESHOOTING

Section I. INTRODUCTION

12-1. General

a. This chapter provides troubleshooting information which sectionalizes synchronizer troubles to the major functional circuit groups when either a complete synchronizer, or a complete interface module, or a complete coder-decoder module has been returned from the using activity for repair.

b. The troubleshooting procedures of this chapter are not necessary if a power supply module, or a timing module, or a delay line module, or any individual printed wiring cards are returned for repair.

(1) If a complete power supply module is returned, the trouble lies in the power supply circuits, and can be localized to one of the three printed wiring cards or the filter parts in the power supply module by the troubleshooting procedure given in chapter 18.

(2) If a complete timing module is returned, the trouble lies in the timing circuits, and can be localized to one of the three printed wiring cards in the timing module by the troubleshooting procedure given in chapter 13.

(3) If a complete delay line module is returned, only the module connector (1A2A5P1) or the wiring from the connector to the solder terminals of the delay line (1A2A5DL1) can be repaired. The delay line is a sealed, nonrepairable assembly and must be replaced if defective.

(4) If an individual printed wiring card is returned, the trouble can be isolated to the defective stage or part on the card by the troubleshooting procedure provided for the card in the corresponding section in chapter 20.

12-2. Troubleshooting Philosophy

a. All troubleshooting information in this technical manual is based on the following assumptions:

(1) The synchronizer is connected into an operational IFF set or the DS, GS, and depot maintenance equivalent (hot mockup).

(2) The synchronizer is defective, and the trouble is a failure in only one stage.

(3) All inputs to the synchronizer from other units of the IFF set or hot mockup are normal.

(4) The trouble is not a wiring failure nor a connector failure.

b. When a known defective synchronizer is installed in an operational IFF set or hot mockup, and turned on, one of the following four conditions will result:

(1) One front panel FAULT lamp lights. If this occurs, the lighted FAULT lamp usually identifies the defective module. Refer to the troubleshooting chart based on single fault indication (para 12-6), which will sectionalize the fault to a functional circuit in the defective module.

(2) More than one front panel FAULT lamp lights. If this occurs, the nature of the trouble is such that it results in fault outputs from more than one self-test circuit. Refer to the troubleshooting chart based on multiple fault indications (para 12-10). This chart lists the possible situations which can result in multiple FAULT lamp indications and sectionalizes the trouble to a functional circuit.

(3) No FAULT lamps light. If this occurs, the trouble is in a circuit which is not self-tested, or the self-test circuit which is supposed to supply a fault indication is itself defective. Refer to the troubleshooting chart based on no fault indications (para 12-11). This chart troubleshoots the circuits which are not self-tested, including

the self-test circuits, and sectionalizes the trouble to a functional circuit.

(4) The synchronizer POWER circuit breaker trips to OFF each time it is set to ON. If this occurs, the fault can be sectionalized to the power supply and power distribution circuits or identified as a short circuit (or equivalent severe overload) in a module other than the power supply module as follows:

(*a*) With the POWER circuit breaker tripped or set to OFF, remove timing module 1A2A4. Then attempt to set the POWER circuit breaker to ON. If the POWER circuit breaker remains at ON, the timing module contains a short circuit or equivalent overload.

(*b*) If the POWER circuit breaker trips to OFF with the timing module removed, remove coder-decoder module 1A2A2. Then again attempt to set the POWER circuit breaker to ON. If the POWER circuit breaker remains at ON, the coder-decoder module contains a short circuit or equivalent overload.

(*c*) If the POWER circuit breaker trips to OFF with the timing and coder-decoder modules removed, remove interface module 1A2A1. Then again attempt to set the POWER circuit breaker to ON. If the POWER circuit breaker trips to OFF, the trouble lies in the power supply and power distribution circuits; refer to chapter 18.

(*d*) If the POWER circuit breaker remains at ON with the timing, coder-decoder, and interface modules removed, set the POWER circuit breaker to OFF, and install an interface module known to be in satisfactory operating condition. Then again attempt to set the POWER circuit breaker to ON. If the POWER circuit breaker remains at ON, the removed interface module contains a short circuit or equivalent overload. If, instead, the POWER circuit breaker again trips to OFF, the trouble lies in the metering circuit of the power supply and power distribution circuits; refer to chapter 18.

c. In some cases, it is possible to sectionalize the trouble to a functional circuit without reference to an overall troubleshooting chart by reasoning the relationship between the trouble symptom, if any, and the fault indication. An obvious example is a power supply fault. If one or more of the +5V, +12V, or −12V positions of front panel voltage selector 1A2S1 does not produce a reading within the green band on front panel meter 1A2M1, then the trouble lies in the power supply circuits, and the repairman can refer directly to the power supply and power distribution troubleshooting and repair chapter, chapter 18. Another example is a timing circuit fault. If the TIMING FAULT lamp lights, the trouble is in the timing module and, since the timing module contains only timing circuits, the overall troubleshooting charts can be disregarded, and the repairman can refer directly to the timing circuit troubleshooting and repair chapter, chapter 13. Still another example is a challenge encoding circuit fault. If no FAULT lamps light when the CHALLENGE switch on the control box is at OFF, or when it is held at TEST, but the CODER DECODER FAULT lamp lights when the CHALLENGE switch is held at ON, then the trouble is in the Challenge encoding circuits, and the repairman can refer directly to the challenge encoding circuit troubleshooting and repair chapter, chapter 14.

Section II. SYNCHRONIZER TROUBLESHOOTING BASED ON SINGLE FAULT INDICATION

12–3. General

This section assumes that when a defective synchronizer is installed and turned on in an operational IFF set or hot mockup one, and only one, front panel FAULT lamp lights.

12–4. Test Equipment Required

The following test equipment is required to perform the troubleshooting based on single fault indication procedures. (For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.)

a. Oscilloscope.

b. Mode 4 word generator.

c. Radar test set.

d. Test facilities set.

e. 28-volt dc power supply.

12-5. Preparation for Troubleshooting

a. If the item to be repaired is a module, proceed as follows:

(1) Check the defective module for short circuits by comparing resistance measurements at its module connector pins with the values given in the corresponding section of chapter 19. Remove all short circuits, if any, before continuing with this procedure.

(2) Set the hot mockup synchronizer POWER circuit breaker to OFF.

(3) Install the defective module in the hot mockup synchronizer in place of the known good module in that synchronizer.

(4) Connect all equipment as shown in figure 24-16.

b. If the item to be repaired is an entire synchronizer, proceed as follows:

(1) Check the defective synchronizer for short circuits by comparing resistance measurements at its rear connector pins with the values given in paragraph 12-13. Remove all short circuits, if any, before continuing with this procedure.

(2) Set the POWER circuit breaker of the defective synchronizer to OFF.

(3) Remove the hot mockup synchronizer from the hot mockup, and install the defective synchronizer in its place.

(4) Connect all equipment as shown in figure 24-16.

c. Set the switches on the control box as follows:

(1) CODE SELECT:	
MODE 1	73
MODE 2	7777
MODE 3/A	7777
(2) CHALLENGE	OFF (released)
(3) GTC	OFF
(4) PANEL	(Immaterial)
(5) POWER	OFF
(6) PROCESSOR	IN
(7) MODE SELECT	3/A
(8) SIF REPLIES	CODED (released)
(9) MODE 4	A

d. On power control panel of interrogator group case, set POWER circuit breaker to ON.

e. Set the controls on the radar test set as follows:

(1) POWER	ON
(2) DISPLAY panel and SWEEP & INTEN MARK panel controls	(Immaterial)
(3) XTAL MARK & SYNC panel controls:	
SWEEP DELAY	(Immaterial)

TRIGGER DELAY—RANGE	50–750
—COARSE and FINE	(Approximately 500 μsec when DELAYED TRIGGER is connected to TRIGGER INPUT of SIF CODER; approximately 180 μsec when DELAYED TRIGGER is connected to EXT TRIG of mode 4 word generator. Procedures for making these settings are given in paragraph 12–17 for reference.)
SYNC SELECT	INT +
XTAL MARK LEVEL	(Immaterial)
PRF	(375 triggers per second. A procedure for making this setting is given in paragraph 12–15 for reference.)
SUP	(Immaterial)

(4) SIF CODER panel controls:

CODE (A, B, C, D)	7777
SUB PULSE SELECT	OFF
FUNCTION	N
LEVEL	HI
SUB PULSE POS	O (immaterial)
PULSE WIDTH	.45 (μsec)
AMPLITUDE	(Fully counter-clockwise).

(5) MARK X CODER panel controls:

PULSE POS	O
MOD INPUT 75Ω	OUT
TRIGGER INPUT 75Ω	(Immaterial)
MODE SELECT	M–3
FUNCTION	EXT HIGH
PULSE WIDTH	(Immaterial)

(6) CAL-CONTROL panel controls:

VIDEO OUT	DEMOD SG MON
CAL ADJ	(Immaterial)
METER SELECT and WM SENS	(As required for PRF and SG FREQUENCY settings; procedures for making those settings are given in paragraphs 12–15 and 12–16 for reference.)
TRIGGER	DEMOD

(7) WAVEMETER INPUT switch ..... SIG GEN
(8) WAVEMETER FREQUENCY ..... (1090 mc; obtain setting from radar test set wavemeter calibration chart.)
(9) SG FREQUENCY ..... (1090 mc; a procedure for making this setting is given in paragraph 12-16 for reference.)
(10) ATTENUATION 50.0

f. Prepare the oscilloscope for operation as directed in TM 11-6625-1703-15, setting the controls for DC channel B vertical amplifier input (unless AC is specified for V / CM given on the waveform illustrations), with voltage and time per screen division, sync, and sweep delay settings as specified on the waveform illustrations.

g. At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

h. To obtain simulated mode 4 signals from the mode 4 word generator, the EXT TRIG and MODE 4 REPLY connections shown by broken lines in figure 24-16 must be completed, and the controls must be set as listed below. However, before completing the connections and setting the Power ON-OFF switch to ON, make certain that the existing setting of the TEST WORD AM, control will result in a safe TEST WORD amplitude (less than 25 volts at 1A2A1A7-34 in the synchronizer). This requires a setting which is not more clockwise than the midposition between the counterclockwise and clockwise limits of adjustment. If there is any doubt, turn the TEST WORD AM. control to a point between its counterclockwise limit and its midposition. Then set the mode 4 word generator controls as follows:

(1) TEST WORD switches 1 through 4	On (up)
(2) TEST WORD switch 5	Off (down)
(3) TEST WORD switches 6 through 37	(one or more at On).
(4) Power ON-OFF	ON
(5) GO-OFF-NO-GO	OFF
(6) PRF SEL	EXT
(7) INT PRF FREQ ADJ	(Immaterial)
(8) TEST WORD AM	For TEST WORD amplititude of 4.5 volts at 1A2A1A7-34 within synchronizer. (A procedure for making this setting is included in paragraph 12-17*c* for reference.)
(9) MODE 4 REPLY controls:	
ON-OFF	ON
AM	(Approximately to midposition).
DELAY	(For a value such that the first pulse of the simulated mode 4 reply appears at 1A2A2A6J1-3 within synchronizer as a receiver video pulse 470 μsec after the O TRIGGER (simulated radar trigger) applied to 1J1 on the interrogator group.

case. A procedure for making this setting is given in paragraph 12–19 for reference.)

(10) AUXILIARY PULSE controls:

ON–OFF	OFF
AM	(Fully clockwise)
DELAY	(Fully clockwise)

(11) DISPARITY controls:

DL1–OFF–DL2	DL2
AM. control	(Approximately to midposition).
DL2	(For a value such that the MODE 4 DISPARITY pulse appears at 1A2A1A7–36 within synchronizer approximately 387 μsec after the O TRIGGER (simulated radar trigger) applied to 1J1 on the interrogator group case. A procedure for making this setting is given in paragraph 12–18 for reference.)
(12) METER switches	(Immaterial)

i. Turn on the 28-volt dc power supply, and adjust it for an output of 28 volts dc.

12–6. Troubleshooting Chart Based on Single Fault Indication

a. Preliminary Procedure. With the synchronizer connected into the hot mockup shown in figure 24–16, and with the controls set as directed in paragraph 12–5, set the synchronizer POWER circuit breaker to ON. Then set the POWER circuit breaker on the control box to ON and, when the 60-second receiver-transmitter warmup delay has ended, find the lighted FAULT lamp in the following chart and take the corrective measures indicated.

b. Overall Troubleshooting Chart Based on Single Fault Indication.

Symptom	*Corrective measures*
RADAR TRIGGER FAULT lamp lighted.	Proceed as follows: *a.* Check radar trigger fault level at 1A2A1A8–16. If high, trouble is in timing circuits; refer to chapter 13. If not high, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. *b.* Observe SYN SELF TEST lamp at control box. It should be lighted when the radar trigger fault level at 1A2A1A8–16 is high. If it is not, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
TIMING FAULT lamp lighted	Proceed as follows: *a.* Check timing fault level at 1A2A1A8–18. If high, trouble is in timing circuits; refer to chapter 13. If not high, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

Symptom	*Corrective measures*
	b. Observe SYN SELF TEST lamp at control box. It should be lighted when the timing fault level at 1A2A1A8-18 is high. If it is not, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
CODER DECODER FAULT lamp lighted.	If fault is indicated only while challenging (CHALLENGE switch on control box held at ON) the trouble is in the challenge encoding circuits; refer to chapter 14. If fault is indicated whether challenging or not, release the CHALLENGE switch (to OFF), and proceed as follows: *a.* Check coder-decoder fault level at 1A2A2A8J1-6. If high, the trouble is either in the challenge encoding or reply decoding circuits. Perform steps *c* through *j* to localize the trouble to the faulty circuits. If not high, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. ***Note.*** **If the CODER-DECODER FAULT lamp is lighted continuously, the coder-decoder fault level at 1A2A2A8J1-6 will be a continuously high level. However, if the fault is intermittent, occurring every other prp, the oscilloscope display will also show the low baseline (no-fault) level.** *b.* Observe SYN SELF TEST lamp at control box. It should be lighted when the coder-decoder fault level at 1A2A2A8J1-6 is high. If it is not, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. *c.* Observe the delay line input signal ($\overline{0.0\ \mu sec}$; P, fig. 20-12) at 1A2A2A6-40. If abnormal, trouble is in the challenge encoding circuits; refer to chapter 14. *d.* Observe the 17 delay line output signals at each of the following points in any convenient order. If any are abnormal, delay line module 1A2A5 is defective; refer to chapter 19, section VI. (1) 1A2A2A3-10, $\overline{1.45\ \mu sec}$ (K, fig. 20-9) (2) 1A2A2A6-26, $\overline{1.8\ \mu sec}$ (N, fig. 20-12) (3) 1A2A2A3-8, $\overline{2.9\ \mu sec}$ (H, fig. 20-9) (4) 1A2A2A6-12, $\overline{3.6\ \mu sec}$ (J, fig. 20-12) (5) 1A2A2A3-9, $\overline{4.35\ \mu sec}$ (J, fig. 20-9) (6) 1A2A2A3-7, $\overline{5.8\ \mu sec}$ (G, fig. 20-9) (7) 1A2A2A2-39, $\overline{7.25\ \mu sec}$ (T, fig. 20-8) (8) 1A2A2A2-35, $\overline{8.7\ \mu sec}$ (R, fig. 20-8) (9) 1A2A2A2-32, $\overline{11.6\ \mu sec}$ (Q, fig. 20-8) (10) 1A2A2A2-37, $\overline{13.05\ \mu sec}$ (S, fig. 20-8) (11) 1A2A2A2-9, $\overline{14.5\ \mu sec}$ (L, fig. 20-8) (12) 1A2A2A2-7, $\overline{15.95\ \mu sec}$ (K, fig. 20-8) (13) 1A2A2A2-12, $\overline{17.4\ \mu sec}$ (M, fig. 20-8) (14) 1A2A2A4-30, $\overline{18.0\ \mu sec}$ (S, fig. 20-10) (15) 1A2A2A2-5, $\overline{18.85\ \mu sec}$ (J, fig. 20-8) (16) 1A2A2A3-6, $\overline{20.3\ \mu sec}$ (F, fig. 20-9) (17) 1A2A2A4-37, $\overline{21.0\ \mu sec}$ (Y, fig. 20-10) *e.* Observe $\overline{\text{gtc trigger}}$ at 1A2A2A8J1-4. It should be a continuously high level. *f.* Observe $\overline{\text{isls gate}}$ at 1A2A2A8-28. It should be a continuously high level. *g.* Observe $\overline{\text{challenge video}}$ at 1A2A2A8J1-5. It should be a continuously high level. *h.* Observe 5-mc clock signal at 1A2A2A8-12 (same as Q, fig. 20-10) and its complement ($\overline{\text{5-mc clock}}$) at 1A2A2A8-7.

Symptom	*Corrective measures*
	i. Observe buffered 21.0 μsec pulse at 1A2A2A4J2–7 (K, fig. 20–10).
	j. If the results of steps *e* through *i* were all normal, the trouble lies in the reply decoding circits; refer to chapter 15. If any one was abnormal, the trouble is in the challenge encoding circuits; refer to chapter 14.
INTERFACE FAULT lamp lighted.	Proceed as follows:
	a. Check interface fault level at 1A2A1A8–14. If high, proceed to step *b*. If not high, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
	Note. If the INTERFACE FAULT lamp is lighted continuously, the interface fault level at 1A2A1A8–14 will be a continuously high level. However, if the fault is intermittent, occurring every other prp, the oscilloscope will also show the low baseline (no-fault) level.
	b. Observe SYN SELF TEST lamp at control box. It should be lighted when the interface fault level at 1A2A1A8–14 is high. If it is not, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
	c. Observe reshaped mode 4 pretrigger at 1A2A1A7J3 (C, fig. 20–6). If normal, trouble is in display video interface circuits; refer to chapter 16. If abnormal, buffer circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII.

Section III. SYNCHRONIZER TROUBLESHOOTING BASED ON MULTIPLE OR NO FAULT INDICATIONS

12–7. General

This section assumes that when a defective synchronizer is installed and turned on in an operational IFF set or hot mockup, either two or more front panel FAULT lamps light, or none of the FAULT lamps light.

12–8. Test Equipment Required

The test equipment required to perform troubleshooting based on multiple or no fault indications is the same as that listed in paragraph 12–4 for troubleshooting based on single fault indication.

12–9. Preparation for Troubleshooting

Preparation for troubleshooting based on multiple or no fault indications is the same as that given in paragraph 12–5 for troubleshooting based on single fault indication.

12–10. Troubleshooting Chart Based on Multiple Fault Indications

a. Preliminary Procedure. With the synchronizer connected into the hot mockup shown in figure 24–16, and with the controls set as directed in paragraph 12–5, set the synchronizer POWER circuit breaker to ON. Then set the POWER circuit breaker on the control box to ON and, after the 60-second receiver-transmitter warmup delay has ended, find the combination of two or more FAULT lamps in the following chart and take the corrective measures indicated.

b. Overall Troubleshooting Chart Based on Multiple Fault Indications.

Symptom	*Corrective measures*
TIMING FAULT and INTERFACE FAULT lamps both lighted.	Trouble is in timing circuits. Refer to chapter 13.
TIMING FAULT and CODER DECODER FAULT lamps both lighted.	Trouble is in timing circuits. Refer to chapter 13.
CODER DECODER FAULT and INTERFACE FAULT lamps both lighted.	Observe 10-mc clock pulses at 1A2A4A1–22 (L, fig. 20–18). If normal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If abnormal, inverter A4B on 10-mc clock and counter A card 1A2A4A1 is defective; refer to chapter 20, section XX.

Symptom	*Corrective measures*
RADAR TRIG, TIMING, CODER DECODER, and INTERFACE FAULT lamps all lighted.	Trouble is in power supply circuits. Refer to chapter 18.

12-11. Troubleshooting Chart Based on No Fault Indications

a. Preliminary Procedure. With the synchronizer connected into the hot mockup shown in figure 24-16, and with the controls set as directed in paragraph 12-5, set the synchronizer POWER circuit breaker to ON. Then set the POWER circuit breaker on the control box to ON and, when the 60-second receiver-transmitter warmup delay has ended, proceed as directed in the following chart:

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Front panel meter selector switch at +12.	Front panel meter	Within center portion of green band.	Trouble is in power supply circuits. Refer to chapter 18.
2	Front panel meter selector switch at +5.	Front panel meter	Within center portion of green band.	Same as step 1.
3	Front panel meter selector switch at −12.	Front panel meter	Within center portion of green band.	Same as step 1.
4	1A2A2A4J1-2	Oscilloscope	Sif enable (high)	Trouble is in challenge encoding circuits. Refer to chapter 14.
5	1A2A1A6-27	Oscilloscope	Challenge video (D, fig. 20-5)	Same as step 4.
6	1A2A1A6-21	Oscilloscope	Gtc trigger (C, fig. 20-5)	Same as step 4.

STEPS 4 THROUGH 13 ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 3/A, CODE 7777, AND RECEIVING A MODE 3/A CODE 7777 NORMAL REPLY:

- AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "3/A," AND WITH "MODE 3/A CODE SELECT" SWITCHES AT "7777."
- AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.

7	1A2A1A6-33	Oscilloscope	Isls gate (E, fig. 20-5)	Same as step 4.
8	1A2A2A4-14	Oscilloscope	Mode 2, 3/A enable (high)	Same as step 4.
9	1A2A2A5-18	Oscilloscope	Sif reply enable (K, fig. 20-11).	Same as step 4.
10	1A2A2A6J1-5	Oscilloscope	Buffered receiver video (D, fig. 20-12).	Trouble is in reply decoding system. Refer to chapter 15.
11	1A2A2A3-38	Oscilloscope	Sif correct code video (R, fig. 20-9).	Same as step 10.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
12	1A2A2A3-36	Oscilloscope	Sif bracket decoded video (Q, fig. 20-9).	Same as step 10.
13	1A2A1A5-6	Oscilloscope	IFF display video (H, fig. 20-4).	Trouble is in display vileo interface circuits. Refer to chapter 16.
			STEPS 14, 15, AND 16 ARE TO BE CARRIED OUT WHILE OPERATING IN THE TEST TARGET MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
14	1A2A1A3J1-6	Oscilloscope	Test target video (F, fig. 20-2).	Same as step 13.
15	1A2A1A5-6	Oscilloscope	IFF display video (J, fig. 20-4).	Same as step 13.
16	1A2A1A8J1-2	Oscilloscope	Spoof counter video (A, fig. 20-7).	Same as step 10.
			STEP 17 IS TO BE CARRIED OUT WHILE CHALLENGING IN MODE 4 AND RECEIVING A MODE 4 REPLY.	
			• AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "4."	
			• MODIFY HOT MOCKUP TO SIMULATE AN RF MODE 4 REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 460 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.	
17	1A2A2A6-22	Oscilloscope	Triple pulse decoded video (M, fig. 20-12).	Same as step 10.

Section IV. REFERENCE INFORMATION AND PROCEDURES

12-12. General

This section presents resistance measurements taken at the rear connector pins of a properly operating synchronizer, two views of the synchronizer which locate the electrical parts on the top and bottom of the chassis, and procedures for making hot mockup control settings.

12–13. Synchronizer Rear Connector Resistance Measurements

a. Conditions of Measurement. The following chart gives the resistance values measured at the connector pins of a properly operating synchronizer complete with all modules and their printed wiring cards installed. These values were measured with the synchronizer removed and disconnected from the interrogator group case, and with POWER circuit breaker 1A2CB1 at ON, voltage selector 1A2S1 at OUT. The measurements were taken with respect to pin 1A2P1–20, which normally serves as the +28-volt return pin when the synchronizer is installed. For the forward resistance measurements, the negative probe of the multimeter (operated as an ohmmeter) was connected to pin 1A2P1–20, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 1A2P1–20, and the negative probe was touched to each of the listed pins. For the measurements at coaxial pins, the inner contacts of the pins were touched carefully, so as not to damage them.

b. Synchronizer Rear Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2P1–1	RX100	1700	RX1	150
1A2P1–2	RX10K	700K	RX1	50
1A2P1–3	RX1	0.0	RX1	0.0
1A2P1–20	RX1	0.0	RX1	0.0
1A2P1–22	RX1	0.0	RX1	0.0
1A2P1–23	RX1	200	RX1	35
1A2P2–A1	RX100	4500	RX100	5000
1A2P2–A2	RX100	5000	RX100	5000
1A2P2–A3	RX100	5000	RX100	5000
1A2P2–A4	RX100	5000	RX100	5000
1A2P2–A5	RX100	4800	RX100	5000
1A2P2–A6	RX100	4800	RX100	5000
1A2P2–A7	RX100	5000	RX100	5000
1A2P2–A8	RX100	5000	RX100	5000
1A2P2–A9	RX100	4800	RX100	5000
1A2P2–A10	RX100	4800	RX100	5000
1A2P2–A11	RX1	0.0	RX1	0.0
1A2P2–A12	RX10,000	130K	RX100	900
1A2P2–A13	RX10,000	5 Mego	RX100	1000
1A2P2–A14	RX10,000	1 Mego	RX100	1800
1A2P2–A15	RX10,000	800K	RX100	1500
1A2P2–A16	RX10,000	800K	RX100	1700
1A2P2–A17	RX10,000	1 Mego	RX100	1600
1A2P2–A18	RX10,000	800K	RX100	1500
1A2P2–A19	RX1	0.0	RX1	0.0
1A2P2–A21	RX10,000	5 Mego	RX100	900
1A2P2–A22	RX10,000	5 Mego	RX100	1000
1A2P2–A23	RX1	0.0	RX1	0.0
1A2P2–B1	RX1	70	RX1	70
1A2P2–B2	RX100	5000	RX100	5000
1A2P2–B3	RX100	3000	RX100	10K
1A2P2–B4	RX100	5000	RX100	5000
1A2P2–B5	RX100	3000	RX100	10K
1A2P2–B6	RX100	5000	RX100	5000
1A2P2–B7	RX100	3500	RX100	10K
1A2P2–B8	RX100	5000	RX100	5000
1A2P2–B9	RX100	3200	RX100	10K
1A2P2–B10	RX100	5000	RX100	5000
1A2P2–B11	RX100	1700	RX100	10K
1A2P2–C1	RX1	70	RX1	16
1A2P2–C2	RX100	4500	RX100	4500
1A2P2–C3	RX1	100	RX1	100
1A2P2–C4	RX100	5000	RX1	5000
1A2P2–C5	RX1	80	RX1	17
1A2P2–C6	RX100	5000	RX100	5000
1A2P2–C7	RX1	80	RX1	17
1A2P2–C8	RX100	5000	RX100	5000
1A2P2–C9	RX100	3500	RX100	10K
1A2P2–C10	RX100	15000	RX100	900
1A2P2–C11	RX100	3500	RX100	10K

12–14. Synchronizer Chassis Part Locations (figs. 12–1 and 12–2)

Figure 12–1 is a top view of the synchronizer with all five plug-in modules removed, identifying the electrical parts visible from the top. Figure 12–2 is a bottom view which identifies the parts visible from the bottom.

12-15. Radar Test Set PRF Setting

a. The PRF control on the XTAL MARK & SYNC panel of the radar test set is adjusted to obtain simulated radar triggers from the O TRIGGER receptacle at a prf of 375 pulses per second, as indicated on the CAL-CONTROL panel meter.

b. With the radar test set turned on, set the METER SELECT switch on the CAL-CONTROL panel to 500 PRF.

c. Adjust the PRF control on the XTAL MARK & SYNC panel for a reading of 375 (pps) on the CAL-CONTROL panel meter.

12-16. Radar Test Set SG FREQUENCY Setting

a. The SG FREQUENCY control on the radar test set is adjusted after the WAVEMETER FREQUENCY control has been set for 1090 mc (as given in the radar test set wavemeter calibration chart), and after the PRF setting of paragraph 12-15 has been made. The adjustment is made for maximum wavemeter output, as indicated on the CAL-CONTROL panel meter.

b. With the radar test set turned on and warmed up for at least 20 minutes, set the METER SE-

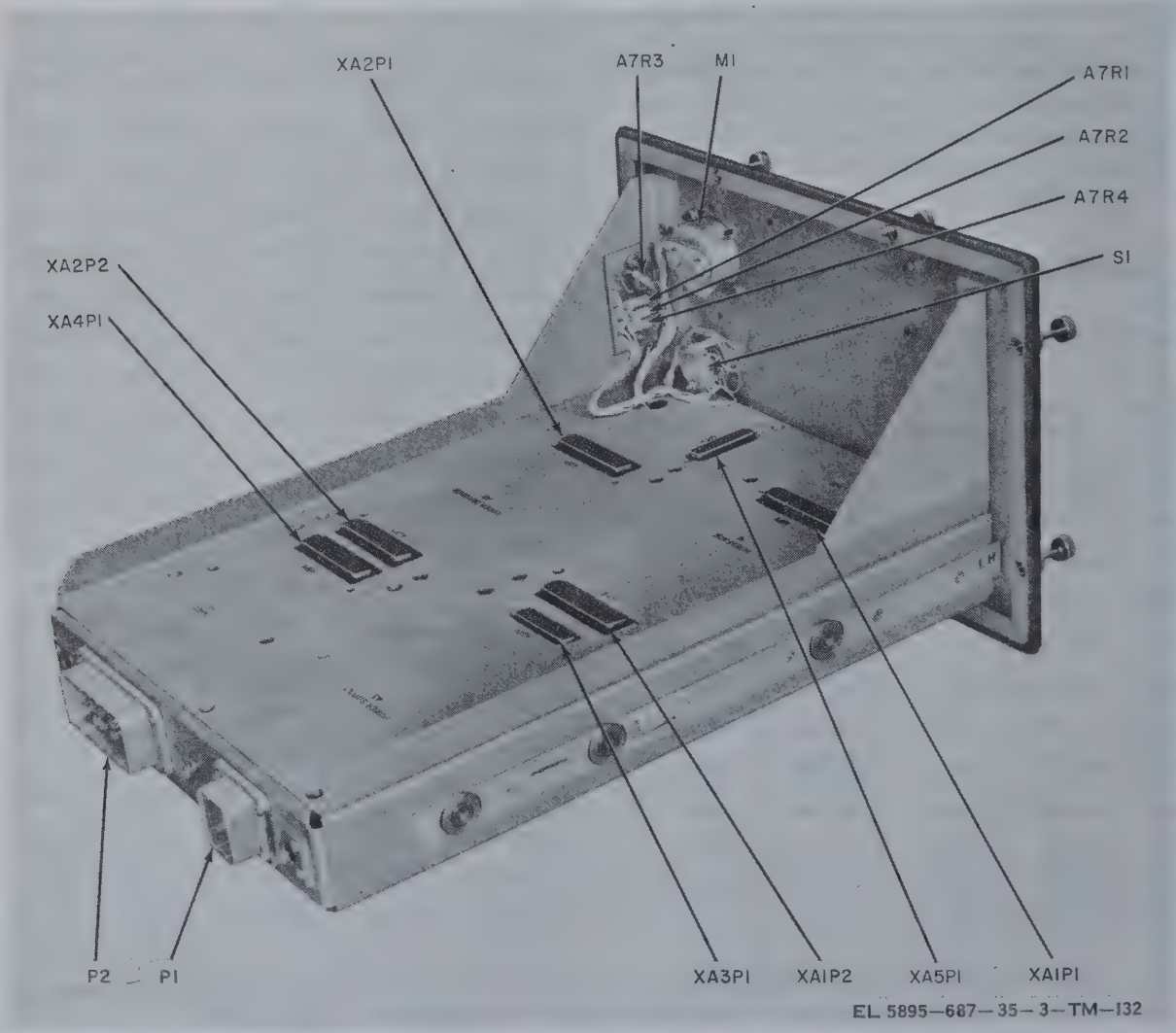


Figure 12-1. Synchronizer 1A2, top of chassis with modules removed.

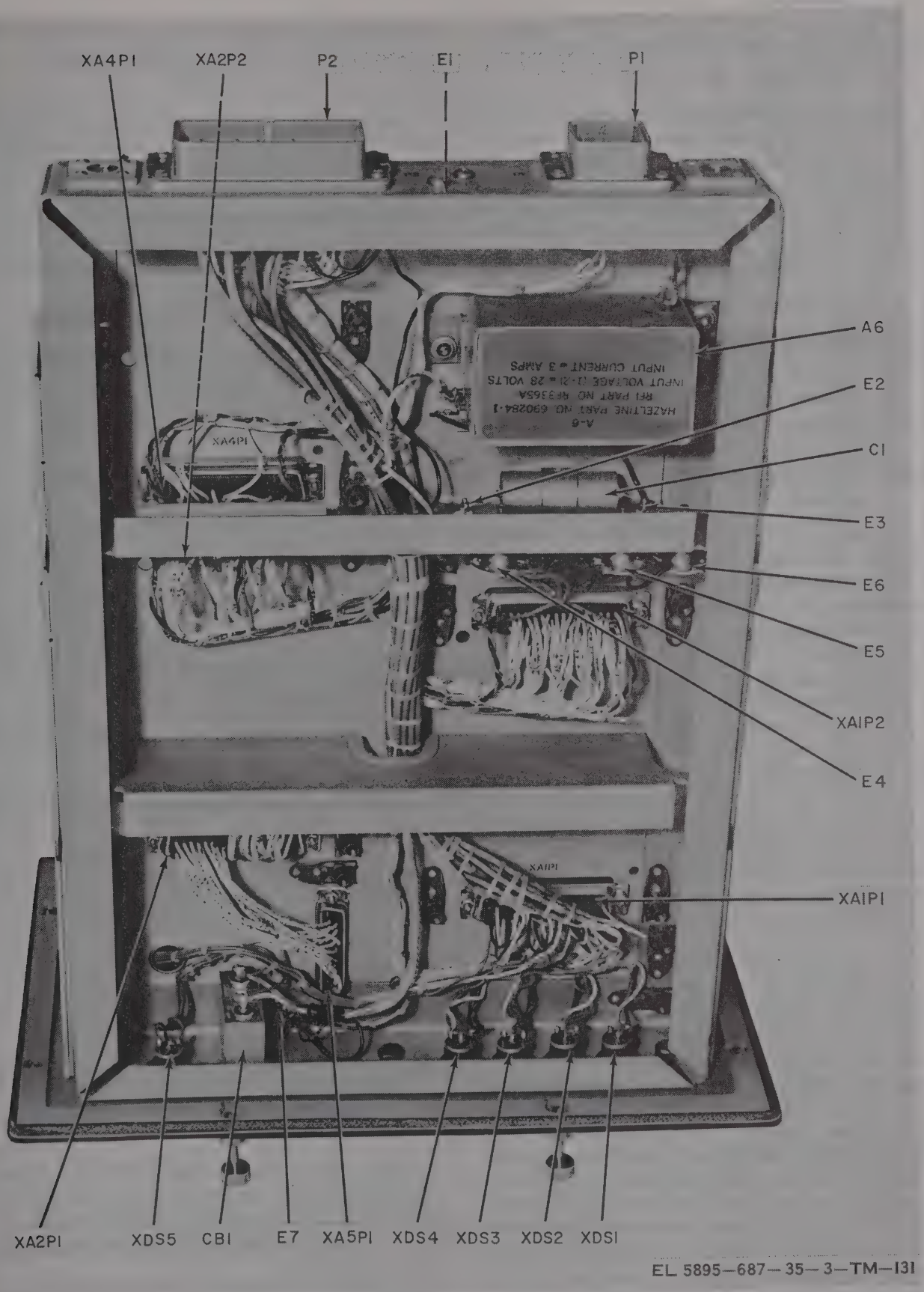


Figure 12-2. Synchronizer 1A2, bottom view.

LECT switch on the CAL-CONTROL panel to WM, and turn the WM SENS control approximately to its midposition.

c. Turn the SG FREQUENCY control to increase or decrease the signal generator frequency until the lowest possible reading ("dip") is obtained on the CAL-CONTROL panel meter. If the reading goes below midscale, adjust the WM SENS control to bring the reading up-scale. Continue to adjust SG FREQUENCY and WM SENS until the best possible dip is obtained at or near midscale on the meter. If the reading goes below midscale after the WM SENS limit has been reached, temporarily change the CODE (A, B, C, D) switch settings on the SIF CODER panel from 7777 to 0000 until the best dip has been obtained. Then return the CODE (A, B, C, D) switch settings to 7777.

12-17. Radar Test Set TRIGGER DELAY Settings

a. Purpose. Two TRIGGER DELAY settings within the RANGE 50-750 μsec are required during testing or troubleshooting of the synchronizer, each corresponding to one of the alternative DELAYED TRIGGER connections indicated in figure 24-16. The DELAYED TRIGGER connection to the SIF CODER shown by an unbroken line is made for each test or troubleshooting step in which a simulated sif reply is required, and the TRIGGER DELAY setting for this connection is accordingly referred to below as the sif reply delay setting. The alternative connection to the mode 4 word generator shown by a broken line is made for each test or troubleshooting step in which simulated mode 4 challenging is required, and the TRIGGER DELAY setting for this connection is accordingly referred to below as the mode 4 challenge delay setting.

b. Sif Reply Delay Setting. When the radar test set is connected to simulate an sif reply, the COARSE and FINE TRIGGER DELAY controls on the XTAL MARK & SYNC panel are adjusted so that the first pulse of the reply pulse train, observed at 1A2A2A6J1-3 within the synchronizer, occurs 500 μsec after the O TRIGGER (simulated radar trigger) applied to RADAR TRIG receptacle 1J1 on the interrogator group case. Because the path to 1A2A2A6J1-3 includes the signal generator of the radar test set, the PRF and SG FREQUENCY settings of paragraphs 12-15 and 12-16 must be made before the sif reply delay setting. In addition, because the path also includes the hot mockup receiver-transmitter, the IFF set must be supplied with power (28 volts dc), turned on, and challenging in an sif mode. To make the sif reply delay setting, proceed as follows:

NOTE

This procedure gives all steps that must be performed initially, when the hot mockup is first assembled. Thereafter, only the last four steps are required to check the setting from time to time or to return to the setting (from the mode 4 challenge delay setting) during a test or troubleshooting procedure.

(1) Connect the test equipment listed in paragraph 12-4 as shown in figure 24-16, using a synchronizer known to be capable of producing a normal gtc trigger output when challenging in mode 3/A.

(2) Set the switches on the control box as directed in paragraph 12-5*c*.

(3) On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

(4) At the radar test set, make all control settings except COARSE and FINE TRIGGER DELAY as directed in paragraph 12-5*e*.

(5) Set the controls on the oscilloscope as directed in paragraph 12-5*f*.

(6) At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

(7) Turn on the 28-volt dc power supply and adjust it for an output of 28 volts dc.

(8) At the synchronizer, set the POWER circuit breaker to ON.

(9) At the control box, set the POWER circuit breaker to ON.

(10) At the radar test set, make the SIF CODER connections shown by unbroken lines in figure 24-16.

(11) At the control box, after the 60-second receiver-transmitter warmup delay has ended, hold the CHALLENGE switch at ON (with the MODE SELECT switch at 1, 2, or 3/A).

(12) At the synchronizer, use the oscilloscope (set as for waveform B of fig. 20-12) to

observe the receiver video at 1A2A2A6J1-3.

(13) On the XTAL MARK & SYNC panel of the radar test set, carefully adjust the COARSE and FINE TRIGGER DELAY controls to position the first pulse of the simulated sif reply pulse train in the receiver video at the left-hand end of the oscilloscope sweep. With an oscilloscope sweep delay of 500 μsec, the sif reply delay is then 500 μsec.

c. Mode 4 Challenge Delay Setting. When the mode 4 word generator is connected to simulate mode 4 signals, the COARSE and FINE TRIGGER DELAY controls on the XTAL MARK & SYNC panel of the radar test set are adjusted so that the first pulse of the TEST WORD output (simulated mode 4 challenge video) from the mode 4 word generator, observed at 1A2A1A7-34 within the synchronizer, occurs 182 μsec after the O TRIGGER (simulated radar trigger) applied to RADAR TRIG receptacle 1J1 on the interrogator group case. Because the TEST WORD output of the mode 4 word generator is observed during the mode 4 challenge delay setting procedure, the procedure also includes a step for adjusting the TEST WORD AM. control. To make the mode 4 challenge delay and TEST WORD AM. control settings, proceed as follows:

NOTE

This procedure gives all steps that must be performed initially, when the hot mock-up is first assembled. Thereafter, only the last five steps are required to check the settings from time to time or to make the mode 4 challenge delay setting for a test or troubleshooting step requiring mode 4 challenging.

(1) Connect the test equipment listed in paragraph 12-4 as shown in figure 24-16.

(2) Set the switches on the control box as directed in paragraph 12-5*c*.

(3) On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

(4) At the radar test set, make all control settings except COARSE and FINE TRIGGER DELAY as directed in paragraph 12-5*e*.

(5) Set the controls on the oscilloscope as directed in paragraph 12-5*f*.

(6) At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

(7) At the mode 4 word generator, make all control settings except TEST WORD AM., MODE 4 REPLY DELAY, and DISPARITY DL2 as directed in paragraph 12-5*h*.

(8) Between the radar test set and the mode 4 word generator, make the connections shown by broken lines in figure 24-16.

(9) At the synchronizer use the oscilloscope (set as for waveform G of fig. 20-11) to observe the simulated mode 4 challenge video at 1A2A1A7-34.

(10) On the XTAL MARK & SYNC panel of the radar test set, carefully adjust the COARSE and FINE TRIGGER DELAY controls to position the first pulse of the simulated mode 4 challenge video pulse train at the left-hand end of the oscilloscope sweep. With an oscilloscope sweep delay of 182 μsec, the mode 4 challenge delay is then 182 μsec.

(11) While observing the simulated mode 4 challenge video waveform, adjust the TEST WORD AM. control on the mode 4 word generator for a pulse amplitude of 4.5 volts. This is the required TEST WORD AM. setting.

(12) If the adjustment of the TEST WORD AM. control has affected the position of the simulated mode 4 challenge video, repeat the mode 4 challenge delay setting of (10) above.

12-18. Mode 4 Word Generator DISPARITY DL2 Setting

a. When the mode 4 word generator is connected to simulate mode 4 signals, the MODE 4 DISPARITY pulse (simulated mode 4 gtc trigger) should occur approximately 387 μsec after the 0 TRIGGER (simulated radar trigger) applied to RADAR TRIG receptacle 1J1 on the interrogator group case. The DISPARITY DL2 setting determines the delay of the MODE 4 DISPARITY pulse with respect to the MODE 4 TRIG input. The AUX

PULSE output connected to the MODE 4 TRIG input is delayed from the first pulse of the TEST WORD by approximately 10 μsec when the AUXILIARY PULSE DELAY control is fully clockwise. The TEST WORD, in turn, is delayed by an amount (182 μsec) determined during the mode 4 challenge delay setting of paragraph 12–17*c*. The mode 4 challenge delay setting must therefore be made before the DISPARITY DL2 setting.

b. To make the DISPARITY DL2 setting, proceed as follows:

NOTE

The DISPARITY DL2 setting must be made initially, when the hot mockup is first assembled, but is not changed during any test or troubleshooting procedures, and therefore need not be repeated each time the mode 4 word generator is connected.

(1) Make the mode 4 challenge delay and TEST WORD AM. control settings as directed in paragraph 12–17*c*.

(2) At the synchronizer, use the oscilloscope (set as for waveform L of fig. 20–14) to observe the simulated mode 4 gtc trigger at 1A2A1A7–36.

(3) At the mode 4 word generator, adjust the DISPARITY DL2 control to position the simulated mode 4 gtc trigger at the left-hand end of the oscilloscope sweep. With an oscilloscope sweep delay of 387 μsec, the delay of the simulated mode 4 gtc trigger is then 387 μsec.

12–19. Mode 4 Word Generator MODE 4 REPLY DELAY Setting

a. When the mode 4 word generator is connected to simulate mode 4 signals, the simulated mode 4 reply is applied to the synchronizer in the same manner as a simulated sif reply: through the rf link composed of the signal generator of the radar test set, the hybrid attenuator of the test facilities set, and the hot mockup receiver-transmitter. Therefore, all of the following settings must be made before the MODE 4 REPLY DELAY setting:

(1) PRF setting (para 12–15);

(2) SG FREQUENCY setting (para 12–16);

(3) Mode 4 challenge delay setting (para 12–17*c*);

(4) DISPARITY DL2 setting (para 12–18).

b. To make the MODE 4 REPLY DELAY setting, proceed as follows:

NOTE

The MODE 4 REPLY DELAY setting must be made initially, when the hot mockup is first assembled, but is not changed during any test or troubleshooting procedures, and therefore need not be repeated each time the mode 4 word generator is connected.

(1) Connect the test equipment listed in paragraph 12–4 as shown in figure 24–16, using a synchronizer known to be capable of delivering a mode 4 gtc trigger when challenging in mode 4. Make the alternative mode 4 word generator connections shown by broken lines.

(2) Set the switches on the control box as directed in paragraph 12–5*c*.

(3) On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

(4) Set the controls on the radar test set as directed in paragraph 12–5*e*, using the procedure of paragraph 12–17*c* for the COARSE and FINE TRIGGER DELAY settings.

(5) Set the controls on the oscilloscope as directed in paragraph 12–5*f*.

(6) At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

(7) At the mode 4 word generator, make all control settings except MODE 4 REPLY DELAY as directed in paragraph 12–5*h*.

(8) Turn on the 28-volt dc power supply and adjust it for an output of 28 volts dc.

(9) At the synchronizer, set the POWER circuit breaker to ON.

(10) At the control box, set the POWER circuit breaker to ON. Then, after the 60-second receiver-transmitter warmup delay has ended, set the MODE SELECT switch to 4, and hold the CHALLENGE switch at ON.

(11) At the synchronizer, use the oscilloscope (set for EXT DC + sync, 1 v/cm, 2 μsec/cm, and 470 μsec sweep delay) to observe the receiver video at 1A2A2A6J1-3.

NOTE

The individual pulses of the simulated mode 4 reply in the receiver video will resemble those of the sif reply shown in waveform B, figure 20-12. However, the mode 4 reply will contain only three pulses (rather than 14), and their spacing will be 1.8 μsec (rather than 1.45 μsec).

(12) At the mode 4 word generator, adjust the MODE 4 REPLY DELAY control to position the first pulse of the simulated mode 4 reply in the receiver video at the left-hand end of the oscilloscope sweep. With an oscilloscope sweep delay of 470 μsec, the MODE 4 REPLY DELAY is then 470 μsec.

CHAPTER 13

TIMING CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. TIMING CIRCUIT TROUBLESHOOTING INFORMATION

13-1. General

a. This chapter provides a troubleshooting procedure to localize any trouble in the timing circuits to a defective printed wiring card, and a test procedure to test the timing circuits after repair. The timing circuits include all parts within timing module 1A2A4 and some parts on two printed wiring cards within interface module 1A2A1. The troubleshooting procedure is based on the assumptions listed in paragraph 12-2 and the further assumption that the trouble is definitely known to lie in the timing circuits, either because it has been sectionalized to these circuits by one of the troubleshooting charts in chapter 12 or because the defective item returned from the using activity is a complete timing module or is one of the three timing module printed wiring cards.

b. This section indexes the timing circuit data located in other parts of this manual, and provides a list of the normal timing circuit test indications. Section II provides the timing circuit troubleshooting procedure, and section III provides timing circuit test information.

c. The timing circuits contain no controls or adjustments.

13-2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the timing circuits:

Reference	*Data*
Chapter 4	Timing circuit functioning.
Fig. 20-5	Low level line driver card 1A2A1A6 waveforms.
Fig. 20-6	Buffer circuit 2 card 1A2A1A7 waveforms.
Fig. 20-18	10-mc clock and counter A card 1A2A4A1 waveforms.
Fig. 20-19	Counter B card 1A2A4A2 waveforms.
Fig. 20-20	Timing self-test card 1A2A4A3 waveforms.
Fig. 24-4	Timing circuit logic diagram.
Fig. 24-17	Synchronizer 1A2 schematic diagram.
Fig. 24-18	Interface module 1A2A1 schematic diagram.
Fig. 24-24	Low level line driver card 1A2A1A6 schematic diagram.
Fig. 24-25	Buffer circuit 2 card 1A2A1A7 schematic diagram.
Fig. 24-39	Timing module 1A2A4 schematic diagram.
Fig. 24-40	10-mc clock and counter A card 1A2A4A1 schematic diagram.
Fig. 24-41	Counter B card 1A2A4A2 schematic diagram.
Fig. 24-42	Timing self-test card 1A2A4A3 schematic diagram.

13-3. Normal Test Indications

The following chart lists the normal input, output, and card-to-card signals which are of significance in troubleshooting or testing the timing circuits. The chart also references illustrations which show the locations of all points of measurement other than card pins.

Point of measurement	Location (fig. No.)	Normal indication
1A2A1A6-13	----	Reshaped mode 4 pretrigger (B, fig. 20-5).
1A2A1A7J2	19-1	Reshaped radar trigger (B, fig. 20-6).
1A2A1A7J3	19-1	$\overline{\text{Reshaped mode 4 pretrigger}}$ (C, fig. 20-6).
1A2A1A7J4	19-1	Radar trigger (same as at 1J1).
1A2A1A7-6	----	$\overline{\text{Self-test pretrigger}}$ (same as L, fig. 20-19, except inverted).
1A2A1A7-8	----	Self-test pretrigger (same as L, fig. 20-19).

Point of measurement	Location (fig. No.)	Normal indication
1A2A1A7-10	----	Processor start pretrigger (same as J, fig. 20-18, except inverted).
1A2A1A7-12	----	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20-18).
1A2A1A7-28	----	Mode 4 pretrigger (same as K, fig. 20-18, except inverted).
1A2A4A1-22	----	10-mc clock (L, fig. 20-18).
1A2A4A2P1-B27	19-9	Counter stop (2^{12}) (G, fig. 20-19).
1A2A4A3J1-2	19-9	$\overline{\text{Reshaped radar trigger}}$ (same as J, fig. 20-19).
1A2A4A3J1-3	19-9	$\overline{\text{Self-test pretrigger}}$ (same as L, fig. 20-19).
1A2A4A3J1-4	19-9	$\overline{\text{Sif pretrigger}}$ (same as K, fig. 20-19).
1A2A4A3J1-6	19-9	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20-18).
1A2A4A3J1-7	19-9	$\overline{\text{Mode 4 pretrigger}}$ (same as K, fig. 20-18).
1A2A4A3-36	----	Timing fault (low level).
1A2A4A3-38	----	Radar trigger fault (low level).
1A2A4A3-40	----	$\overline{\text{Radar trigger fault}}$ (high level).

Section II. TIMING CIRCUIT TROUBLESHOOTING CHART

13-4. General

The timing circuits operate and deliver their outputs continuously for as long as the synchronizer is turned on and radar triggers are supplied at an acceptable prf, whether the IFF set is challenging or not. For troubleshooting or testing of the timing circuits, therefore, the only synchronizer inputs required from the hot mockup are 28-volt dc power and simulated radar triggers.

13-5. Test Equipment Required

a. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facility set are not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set (only to supply "0" TRIGGER output to 1J1).

(3) 28-volt dc power supply.

(4) Test facilities set (only for cables W32, W41, W42, and W47).

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

13-6. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, disregard step *b* and proceed with step *c* below.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24-16.

c. Set the switches on the control box as directed in paragraph 12-5*c*.

d. At the interrogator group case, set the POWER circuit breaker to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12-5*e*(3).

f. Set the controls on the oscilloscope as directed in paragraph 12-5*f*.

g. Turn on the 28-volt dc power supply.

13-7. Troubleshooting Chart

a. Preliminary procedure. With the synchronizer

connected into either the complete hot mockup shown in figure 24-16 or the partial hot mockup established in paragraph 13-6*b*, set the synchronizer POWER circuit breaker to ON. Then set the POWER circuit breaker on the control box to ON and observe the timing circuit signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the corrective measures column.

NOTE

The troubleshooting steps may be undertaken immediately. It is not necessary to wait for the receiver-transmitter 60-second warmup delay to end.

b. Timing Circuit Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	1A2A4A3-38	Oscilloscope	Radar trigger fault (low)	If abnormal, perform step 3.
2	1A2A4A3-40	Oscilloscope	Radar trigger fault (high)	If normal, proceed to step 4. If abnormal, perform step 3.
3	1A2A1A7J2	Oscilloscope	Reshaped radar trigger (B, fig. 20-6).	If abnormal, buffer circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII. If normal, timing self-test card 1A2A4A3 is defective; refer to chapter 20, section XXII.
4	1A2A4A3-36	Oscilloscope	Timing fault (low)	If abnormal, perform steps 5 through 11. If normal proceed to step 12.
5	1A2A4A3J1-2	Oscilloscope	Reshaped radar trigger (same as J, fig. 20-19).	If abnormal, inverter A6B on counter B card 1A2A4A2 is defective; refer to chapter 20, section XXI.
6	1A2A4A1-22	Oscilloscope	10-mc clock pulses (L, fig. 20-18).	If abnormal, 10-mc clock and counter A card 1A2A4A1 is defective; refer to chapter 20, section XX.
7	1A2A4A3J1-7	Oscilloscope	Mode 4 pretrigger (same as K, fig. 20-18).	If normal, proceed to step 9. If abnormal, perform step 8.
8	1A2A4A2P1-B27	Oscilloscope	Counter stop (2^{12}) (G, fig. 20-19).	If normal, AND A7B, A8 on 10-mc clock and counter A card 1A2A4A1 is defective; refer to chapter 20, section XX. If abnormal (continuously high or low, or pulse interval a multiple of normal), check for the presence of 2^4 count square wave at 1A2A4A2J1-B19. If present, counter B card 1A2A4A2 is defective; refer to chapter 20, section XXI. If absent, or if square wave period is not 3.2 μsec, 10-mc clock and counter A card 1A2A4A1 is defective; refer to chapter 20, section XX.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
9	1A2A4A3J1-6	Oscilloscope	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20-18).	If abnormal, AND A7A, A9 on 10-mc clock and counter A card 1A2A4A1 is defective; refer to chapter 20, section XX.
10	1A2A4A3J1-3	Oscilloscope	$\overline{\text{Self test pretrigger}}$ (same as L, fig. 20-19).	If abnormal, AND A7B, A3 on counter B card 1A2A4A2 is defective; refer to chapter 20, section XXI.
11	1A2A4A3J1-4	Oscilloscope	$\overline{\text{Sif pretrigger}}$ (same as K, fig. 20-19).	If abnormal, AND A7A, A2 on counter B card 1A2A4A2 is defective; refer to chapter 20, section XXI. If normal, timing self-test card 1A2A4A3 is defective; refer to chapter 20, section XXII.
			STEPS 12 THROUGH 17 ASSUME THAT A FAULT IS PRESENT IN THE TIMING SYSTEM, BUT THE "TIMING FAULT" INDICATOR IS NOT LIGHTED.	
12	1A2A1A6-13	Oscilloscope	Reshaped mode 4 pretrigger (B, fig. 20-5).	If abnormal, observe $\overline{\text{reshaped mode 4 pretrigger}}$ at 1A2A1A7J3 (C, fig. 20-6). If normal, line driver Q2 on low level line driver card 1A2A1A6 is defective; refer to chapter 20, section VII. If abnormal, buffer circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII.
13	1A2A1A7-28	Oscilloscope	Mode 4 pretrigger (same as K, fig. 20-18, except inverted).	If abnormal, inverter A3A on buffer circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII.
14	1A2A1A7-12	Oscilloscope	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20-18).	If abnormal, buffer circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII.
15	1A2A1A7-10	Oscilloscope	Processor start pretrigger (same as J, fig. 20-18, except inverted).	Same as step 14.
16	1A2A1A7-6	Oscilloscope	Self test pretrigger (same as L, fig. 20-19, except inverted).	Same as step 14.
17	1A2A1A7-8	Oscilloscope	$\overline{\text{Self test pretrigger}}$ (same as L, fig. 20-19).	Same as step 14.

Section III. TIMING CIRCUIT ADJUSTMENT AND TESTING

13-8. Test Equipment and Preparation

There are no adjustments in the timing circuits, and there are no special procedures required to test the timing circuits, other than observations of the timing circuit outputs to the other synchronizer circuits and to the processor. The timing circuit outputs can be observed with the synchronizer connected and turned on in the same hot mockup as is used for troubleshooting. Therefore, the test equipment required is the same as that referenced in paragraph 13-5, and the preparation for testing is the same as the preparation for troubleshooting given in paragraph 13-6.

13-9. Test Procedure

To verify that the timing circuits are performing satisfactorily, prepare the hot mockup as for troubleshooting the timing circuits (para 13-6), turn on the synchronizer POWER circuit breaker, and turn on the POWER circuit breaker on the control box. Then use the oscilloscope to check for normal timing circuit signals at all of the following points in any desired order.

Point measurement	*Location (Fig. No.)*	*Signal*
(1) 1A2A1A7J2	19-1	Reshaped radar trigger (B, fig. 20-5).
(2) 1A2A4A3J1-7	19-9	Mode 4 pretrigger (same as K, fig. 20-18).
(3) 1A2A4A3J1-3	19-9	Self-test pretrigger (same as L, fig. 20-19).
(4) 1A2A4A3J1-4	19-9	Sif pretrigger (same as K, fig. 20-19).
(5) 1A2A4A3J1-6	.....	Processor start pretrigger (same as J, fig. 20-18).
(6) 1A2A4A3-36	.....	Timing fault (low level).
(7) 1A2A4A3-38	.....	Radar trigger fault (low level).
(8) 1A2A4A3-40	.....	Radar trigger fault (high level).
(9) 1A2A4A1-22	.....	10-mc clock (L, fig. 20-18).
(10) 1A2A1A7-28	.....	Mode 4 pretrigger (same as K, fig. 20-18, except inverted).
(11) 1A2A1A7-6	.....	Self-test pretrigger (same as L, fig. 20-19, except inverted).
(12) 1A2A1A7-8	.....	Self-test pretrigger (same as L, fig. 20-19).
(13) 1A2A1A7-10	.....	Processor start pretrigger (same as J, fig. 20-18, except inverted).
(14) 1A2A1A7-12	.....	Processor start pretrigger (same as J, fig. 20-18).
(15) 1A2A1A6-13	.....	Reshaped mode 4 pretrigger (B, fig. 20-5).

CHAPTER 14

CHALLENGE ENCODING CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. CHALLENGE ENCODING CIRCUIT TROUBLESHOOTING INFORMATION

14–1. General

a. This chapter provides a troubleshooting procedure to localize any trouble in the challenge encoding circuits to a printed wiring card and a test procedure to test the challenge encoding circuits after repair. Most of the challenge encoding circuit parts are physically contained in coder-decoder module 1A2A2. The other parts include delay line module 1A2A5, which is time shared with the reply decoding circuits, and some of the parts on four printed wiring cards within interface module 1A2A1. The troubleshooting procedure is based on the assumptions listed in paragraph 12–2 and the further assumption that the trouble is definitely known to lie in the challenge encoding circuits. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12.

b. This section indexes the challenge encoding circuit data located in other parts of this manual, and provides a list of the normal challenge encoding circuit test indications. Section II provides the challenge encoding circuit troubleshooting procedure, section III provides challenge encoding circuit adjustment procedures, and section IV provides the challenge encoding circuit test procedure.

14–2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the challenge encoding circuits:

Reference	*Data*
Chapter 5	Challenge encoding circuit functioning.
Fig. 20–5	Low level line driver card 1A2A1A6 waveforms.
Fig. 20–10	Coder card 1A2A2A4 waveforms.
Fig. 20–11	Challenge video card 1A2A2A5 waveforms.
Fig. 20–12	Reply video card 1A2A2A6 waveforms.
Fig. 20–14	Coder-decoder self-test card 1A2A2A8 waveforms.
Fig. 24–5	Challenge encoding circuit block diagram.
Fig. 24–6	Challenge encoding circuit logic diagram.
Fig. 24–7	Challenge encoding circuit timing diagrams.
Fig. 24–17	Synchronizer 1A2 schematic diagram.
Fig. 24–18	Interface module 1A2A1 schematic diagram.
Fig. 24–20	Level shifter card 1A2A1A2 schematic diagram.
Fig. 24–22	Target video card 1A2A1A4 schematic diagram.
Fig. 24–24	Low level line driver card 1A2A1A6 schematic diagram.
Fig. 24–25	Buffer circuit 2 card 1A2A1A7 schematic diagram.
Fig. 24–27	Coder-decoder module 1A2A2 schematic diagram.
Fig. 24–30	Coder card 1A2A2A4 schematic diagram.
Fig. 24–31	Challenge video card 1A2A2A5 schematic diagram.
Fig. 24–32	Reply video card 1A2A2A6 schematic diagram.
Fig. 24–34	Coder-decoder self-test card 1A2A2A8 schematic diagram.

14–3. Adjustments

The challenge encoding circuits contain three adjustment potentiometers, all physically located in coder-decoder module 1A2A2 (fig. 19–3) on challenge video card 1A2A2A5. Two potentiometers on that card, R3 (sif P1, P3 adjust) and R2 (sif P2 adjust), are adjusted so that the corresponding sif challenge video pulses (D, fig. 20–5) are delivered with a pulse width of 0.77 μsec. The third potentiometer, R1 (mode 4 challenge video adjust) is adjusted so that the mode 4 challenge video pulses

are delivered with a pulse width of 0.47 μsec. The adjustment procedures are given in paragraphs 14–11 and 14–12.

14–4. Normal Test Indications

The following chart lists the normal input, output, and card-to-card signals which are of significance in troubleshooting or testing the challenge encoding circuits. The chart also references illustrations which show the locations of all points of measurement other than card pins.

Point of measurement	Location (fig. No.)	Normal indication
1A2A1A2J1–1	19–1	Mode 1 enable (high in mode 1).
1A2A1A2J1–2	19–1	Mode 2 enable (high in mode 2).
1A2A1A2J1–3	19–1	Mode 3/A enable (high in mode 3/A).
1A2A1A2J1–4	19–1	Mode 4 enable (high in mode 4).
1A2A1A2–6	----	$\overline{\text{Mode 1 enable}}$ (ground from control box in mode 1).
1A2A1A2–10	----	$\overline{\text{Mode 2 enable}}$ (ground from control box in mode 2).
1A2A1A2–14	----	$\overline{\text{Mode 3/A enable}}$ (ground from control box in mode 3/A).
1A2A1A2–18	----	$\overline{\text{Mode 4 enable}}$ (ground from control box in mode 4).
1A2A1A4–3	----	Mode 4 enable (high in mode 4).
1A2A1A6–21	----	Gtc trigger (C, fig. 20–5).
1A2A1A6–27	----	Challenge video (D, fig. 20–5, in mode 3/A).
1A2A1A6–33	----	Isls gate (E, fig. 20–5).
1A2A1A7–34	----	Mode 4 challenge video (same as applied at 1J4–E).
1A2A1A7–36	----	Mode 4 gtc trigger (same as applied at 1J4–F).
1A2A2A4J1–2	19–3	Sif enable (high in modes 1, 2, and 3/A).
1A2A2A4J1–10	19–3	$\overline{\text{Sif isls (P2) trigger}}$ (D, fig. 20–10).
1A2A2A4–5	----	Reply enable 1 (same as R, fig. 20–10, except inverted).
1A2A2A4–6	----	Buffered 15.95 μsec (same as A, fig. 20–8).
1A2A2A4–11	----	Buffered 13.05 μsec (same as F, fig. 20–8).
1A2A2A4–14	----	Mode 2, 3/A enable (high in modes 2 and 3/A).
1A2A2A4–18	----	$\overline{\text{Mode 4 isls trigger}}$ (P, fig. 20–10).
1A2A2A4–24	----	5-mc clock (Q, fig. 20–10).
1A2A2A4–25	----	Isls pulse inhibit (low from receiver-transmitter).
1A2A2A4–26	----	$\overline{\text{5-mc clock}}$ (complement of 5-mc clock: Q, fig. 20–10).
1A2A2A4–34	----	$\overline{\text{Isls gate}}$ (W, fig. 20–10).
1A2A2A4–35	----	$\overline{\text{Sif enable}}$ (low in modes 1, 2, and 3/A).
1A2A2A4–37	----	$\overline{\text{21.0 μsec}}$ (Y, fig. 20–10).
1A2A2A4–39	----	10-mc clock (same as L, fig. 20–18).
1A2A2A5J1–2	19–3	$\overline{\text{Challenge video}}$ (A or B, fig. 20–11).
1A2A2A5J1–4	19–3	$\overline{\text{Isls gate}}$ (same as W, fig. 20–10).
1A2A2A5–6	----	Reshaped self-test and sif pretriggers (H, fig. 20–11).
1A2A2A5–16	----	$\overline{\text{Mode 4 fourth sync pulse}}$ (J, fig. 20–11).
1A2A2A5–18	----	$\overline{\text{Sif reply enable}}$ (K, fig. 20–11).
1A2A2A5–21	----	$\overline{\text{Self-test pretrigger}}$ (same as L, fig. 20–19).

Point of measurement	Location (fig. No.)	Normal indication
1A2A2A5-24	----	Self-test pretrigger (same as L, fig. 20-19, except inverted).
1A2A2A5-32	----	$\overline{\text{Sif}}$ pretrigger (same as K, fig. 20-19).
1A2A2A5-33	----	$\overline{\text{Sif P1}}$ trigger (same as T, U, or V, fig. 20-10, except inverted).
1A2A2A5-34	----	$\overline{\text{Sif P3}}$ trigger (same as X, fig. 20-10).
1A2A2A5-36	----	Mode 4 enable (high in mode 4).
1A2A2A5-37	----	Processor start pretrigger (same as J, fig. 20-18, except inverted).
1A2A2A5-38	----	Mode 4 pretrigger (same as K, fig. 20-18, except inverted).
1A2A2A5-40	----	$\overline{\text{Suppression gate}}$ (L, fig. 20-11).
1A2A2A5-43	----	$\overline{\text{Gtc}}$ trigger (M, fig. 20-11).
1A2A2A6-5	----	$\overline{\text{Mode 4}}$ pretrigger (same as K, fig. 20-18).
1A2A2A6-18	----	Mode 4 enable (high in mode 4).
1A2A2A6-40	----	0.0 μsec (P, fig. 20-12).
1A2A2A8J1-4	19-3	$\overline{\text{Gtc}}$ trigger (same as M, fig. 20-11).
1A2A2A8-11	----	Coder-decoder fault (high level).
1A2A2A8-14	----	$\overline{\text{Radar trigger fault}}$ (high input level).

Section II. CHALLENGE ENCODING CIRCUIT TROUBLESHOOTING CHART

14-5. General

Most of the troubleshooting or testing of the challenge encoding circuits can be carried out in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. However, for those circuits which are exercised only in the other modes, the troubleshooting procedure specifies mode switching at the appropriate steps.

14-6. Test Equipment Required

The challenge encoding circuit troubleshooting procedure is based on operation of the defective synchronizer as part of the complete hot mockup shown in figure 24-16. The test equipment required is therefore the same as shown in that figure and listed in paragraph 12-4. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

14-7. Preparation for Troubleshooting

The preparation required for troubleshooting of the challenge encoding circuits is the same as for overall synchronizer troubleshooting (para 12-5). Therefore, if the synchronizer is already connected into the complete hot mockup shown in figure 12-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, proceed as directed in paragraph 12-5.

14-8. Troubleshooting Chart

a. Preliminary Procedure

(1) After all preparations have been made for troubleshooting the challenge encoding circuits, set the synchronizer POWER circuit breaker to ON and the control box POWER circuit breaker to ON.

NOTE

The procedure of (2) below, and the appropriate steps of the troubleshooting chart may be started immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(2) At the control box, hold the CHALLENGE switch at ON and turn the MODE SELECT switch to 1, 2, 3/A, and 4 in any

order, observing the SYN SELF TEST lamp for at least two seconds in each position.

(*a*) If the SYN SELF TEST lamp lights for longer than one second in any of the three sif modes (1, 2, and 3/A), but not in mode 4, hold the CHALLENGE switch at ON with the MODE SELECT switch at 3/A, and proceed with steps 1 through 11 of the following chart. Observe the signals at the indicated test points, proceeding in step number order unless otherwise directed in the corrective measures column.

(*b*) If the SYN SELF TEST LAMP lights for longer than one second in mode 4, hold the CHALLENGE switch at ON with the MODE SELECT switch at 4. Then disregard steps 1 through 11 of the following chart, and proceed with steps 12 through 16. Observe the signals at the indicated test points in step number order unless otherwise directed in the corrective measures column.

(*c*) If the SYN SELF TEST lamp does not light for longer than one second in any mode, hold the CHALLENGE switch at ON with the MODE SELECT switch at 3/A. Then disregard steps 1 through 16 of the following chart, and proceed with steps 17 through 26. Observe the signals at the indicated test points in step number order unless otherwise directed in the corrective measures column.

b. Challenge Encoding Circuit Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	1A2A2A5J1–2	Oscilloscope	$\overline{\text{Challenge video}}$ (A, fig. 20–11).	If normal, proceed with step 10. If one or more pulses are missing, proceed with step 2. If all pulses are present but one or more pulses are wider or narrower than 0.77 μsec, adjust 1A2A2A5R3 for the P1 and P3 pulses and/or 1A2A2A5R2 for the P2 pulse as directed in paragraph 14–11.
2	1A2A2A5–33	Oscilloscope	$\overline{\text{Sif P1 trigger}}$ (same as T, fig. 20–10, except inverted).	If abnormal, proceed with step 4.
3	1A2A2A5–34	Oscilloscope	$\overline{\text{Sif P3 trigger}}$ (same as X, fig. 20–10).	If normal, proceed with step 9. If abnormal, proceed with step 4.
4	1A2A2A4–37	Oscilloscope	$\overline{\text{21.0 μsec pulse}}$ (Y, fig. 20–10).	If normal, proceed with step 8. If abnormal, perform step 5.
5	1A2A2A6–40	Oscilloscope	$\overline{\text{0.00 μsec pulse}}$ (P, fig. 20–12).	If normal, delay line module 1A2A5 is defective. If abnormal, proceed with step 6.
6	1A2A2A6–38	Oscilloscope	Reshaped self-test and sif pretriggers (same as H, fig. 20–11).	If abnormal, measure sif enable level at 1A2A2A4J1–2 (high). If high, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If not high, check for high mode 3/A

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				enable at 1A2A1A2J1-3. If high at 1A2A1A2J1-3, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If not high at 1A2A1A2J1-3, level shifter Q3 on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
7	1A2A2A6-5	Oscilloscope	Mode 4 pretrigger (same as K, fig. 20-18).	If normal, reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV. If abnormal, inverter A13C on challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII.
8	1A2A2A4-11	Oscilloscope	Buffered 13.05 μsec (same as F, fig. 20-8).	If normal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If abnormal, correct code 1 card 1A2A2A2 is defective; refer to chapter 20, section X.
9	1A2A2A5-20	Oscilloscope	Sif isls (P2) trigger (same as D, fig. 20-10).	If normal, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If abnormal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII.
10	1A2A2A8J1-4	Oscilloscope	Gtc trigger (same as M, fig. 20-11).	If abnormal, OR A7D or inverter A7C on challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII.
11	1A2A2A5J1-4	Oscilloscope	Isls gate (same as W, fig. 20-10).	If abnormal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If normal, coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.
			STEPS 12 THROUGH 16 ASSUME THAT THE "CODER-DECODER FAULT" LAMP IS LIGHTED IN MODE 4. THEREFORE, AT CONTROL BOX, SET "MODE SELECT" SWITCH TO "4," AND HOLD "CHALLENGE" SWITCH AT "ON" FOR THOSE STEPS.	

Step No.	Test point	Test equipment	Normal indication	Corrective measures
12	1A2A2A5J1-2	Oscilloscope	Challenge video (B, fig. 20-11).	If normal, proceed to step 16. If no pulses are present check for mode 4 challenge video at 1A2A2A5J1-9 (G, fig. 20-11). If present without isls pulse at 1A2A2A5J1-9, proceed with step 13. If not present at 1A2A2A5J1-9, buffer-circuit 2 card 1A2A1A7 is defective; refer to chapter 20, section VIII. If first four (sync) pulses are present at 1A2A5J1-2 but fifth (isls) pulse is missing, proceed with step 14. If all pulses are present at 1A2A2A5J1-2 but pulse width is greater or less than 0.47 μsec, adjust 1A2A2A5R1 as directed in paragraph 14-12.
13	1A2A2A5-36	Oscilloscope	Mode 4 enable (high)	If high, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If not high, check mode 4 enable at 1A2A1A2J1-4 (high). If high at 1A2A1A2J1-4, target video card 1A2A1A4 is defective; refer to chapter 20, section V. If not high at 1A2A1A2J1-4, level shifter Q4 on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
14	1A2A2A5-28	Oscilloscope	Mode 4 isls trigger (same as P, fig. 20-10).	If normal, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If abnormal, proceed with step 15.
15	1A2A2A5-16	Oscilloscope	Mode 4 fourth sync pulse (J, fig. 20-11).	If normal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If abnormal, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII.
16	1A2A2A8J1-4	Oscilloscope	Gtc trigger (same as M, fig. 20-11).	If abnormal, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If normal, coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
			STEPS 17 THROUGH 26 ASSUME THAT THE "CODER-DECODER FAULT" LAMP IS NOT LIGHTED IN ANY MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "3/A" FOR THESE STEPS.	
17	1A2A1A6-27	Oscilloscope	Challenge video (D, fig. 20-5).	If normal, proceed with step 20. If absent proceed with step 18. If all three pulses are present, but one or more are wider or narrower than 0.77 μsec, adjust 1A2A2A5R3 and/or 1A2A2A5R2 as directed in paragraph 14-11.
18	1A2A2A5J1-2	Oscilloscope	Challenge video (A, fig. 20-11).	If normal, line driver Q4 on low level line driver card 1A2A1A6 is defective; refer to chapter 20, section VII. If no pulses are present, proceed with step 19.
19	1A2A2A4J1-2	Oscilloscope	Sif enable (high)	If high, AND A2A on challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If not high, coder card 1A2A2A4 is defective; refer to chapter 20, section XII.
20	1A2A1A6-21	Oscilloscope	Gtc trigger (C, fig. 20-5)	If abnormal, line driver Q3 on low level line driver card 1A2A1A6 is defective; refer to chapter 20, section VII.
21	1A2A1A6-33	Oscilloscope	Isls gate (E, fig. 20-5)	If abnormal, line driver Q5 on low level line driver card 1A2A1A6 is defective; refer to chapter 20, section VII.
22	1A2A2A5-18	Oscilloscope	Sif reply enable (K, fig. 20-11).	If normal, proceed with step 25. If abnormal, proceed with step 23.
23	1A2A2A5-22	Oscilloscope	Reply enable 1 (same as R, fig. 20-10, except inverted).	If normal, AND A6D on challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII. If abnormal, proceed with step 24.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
24	1A2A2A5-24	Oscilloscope	$\overline{\text{Self-test pretrigger}}$ (same as L, fig. 20-19).	If normal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If abnormal, challenge video card 1A2A2A5 is defective; refer to chapter 20, section XIII.
25	1A2A2A4-14	Oscilloscope	Mode 2, 3/A enable (high)	If high, proceed with step 26. If not high, OR A9D on coder card 1A2A2A4 is defective; refer to chapter 20, section XII.
26	1A2A2A4-35	Oscilloscope	$\overline{\text{Sif enable}}$ (low)	If not low, inverter A12A on coder card 1A2A2A4 is defective; refer to chapter 20, section XII. If low, coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.

Section III. ADJUSTMENT OF CHALLENGE ENCODING CIRCUITS

14-9. General

The challenge encoding circuit adjustments are the challenge video pulse width adjustments made by means of the three potentiometers on challenge video card 1A2A2A5. The sif adjustments are made by challenging in one of the sif modes, observing the resulting challenge video waveform, and correcting the pulse widths if they are not 0.77 μsec. The mode 4 adjustment is made by challenging in mode 4, observing the resulting challenge video waveform, and correcting the pulse width if other than 0.47 μsec.

14-10. Test Equipment and Preparation

Like the troubleshooting procedure given in section II of this chapter, the adjustment procedures are based on operation of the synchronizer as part of the complete hot mockup shown in figure 24-16. The test equipment required is therefore the same as listed in paragraph 12-4, and the preparation procedure is the same as given for overall synchronizer troubleshooting in paragraph 12-5.

14-11. Sif Challenge Video Pulse Width Adjustments

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON. Then, after the receiver-transmitter 60-second warmup delay has ended, set the MODE SELECT switch to 3/A, and hold the CHALLENGE switch at ON.

c. Observe the resulting sif challenge video pulses at 1A2A1A6-27 (D, fig. 20-5), using the oscilloscope.

d. If the first (P1) and third (P3) pulses are not 0.77 μsec wide at the half-amplitude points, adjust 1A2A2A5R3 (fig. 19-3) to correct the width to 0.77 μsec.

e. If the second (P2) pulse is not 0.77 μsec wide at the half-amplitude points, adjust 1A2A2A5R2 (fig. 19-3) to correct the width to 0.77 μsec.

14-12. Mode 4 Challenge Video Pulse Width Adjustment

a. After all preparations have been made for adjustment of the challenge encoding circuits, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON. Then, after the receiver-transmitter 60-second warmup delay has ended, set the MODE SELECT switch to 4, and hold the CHALLENGE switch at ON.

c. Observe the resulting mode 4 challenge video pulses at 1A2A1A6-27 (similar to B, fig. 20-11, except inverted), using the oscilloscope.

d. If the pulse width is not 0.47 μsec at the half-amplitude points, adjust 1A2A2A5R1 (fig. 19-3) to correct the width to 0.47 μsec.

Section IV. CHALLENGE ENCODING CIRCUIT TESTING

14–13. General

The challenge encoding circuits are most effectively tested by observing their outputs to other synchronizer circuits and to other parts of the IFF set, using an oscilloscope. Most of the observations can be made in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. The remaining observations, made in the other modes, check only the functions which are not adequately checked in mode 3/A.

14–14. Test Equipment and Preparation

Like the troubleshooting procedure given in section II of this chapter, the challenge encoding circuit test observations are made with the synchronizer in operation as part of the complete hot mockup shown in figure 24–16. The test equipment required is therefore the same as listed in paragraph 12–4, and the preparation procedure is the same as given for overall synchronizer troubleshooting in paragraph 12–5.

14–15. Test Procedure

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON. Then, when the receiver-transmitter 60-second warmup delay has ended, set the MODE SELECT switch to 3/A and hold the CHALLENGE switch at ON.

c. At the synchronizer, use the oscilloscope to observe the signals at all of the following points in any desired order.

Point of measurement	*Signal*
(1) 1A2A1A6–21	Gtc trigger (C, fig. 20–5).
(2) 1A2A1A6–27	Challenge video (D, fig. 20–5).
(3) 1A2A1A6–33	Isls gate (E, fig. 20–5).
(4) 1A2A2A4J1–2	Sif enable (high in modes 1, 2, and 3/A).
(5) 1A2A2A4–5	Reply enable 1 (same as R, fig. 20–10, except inverted).
(6) 1A2A2A4–14	Mode 2/3/A enable (high in modes 2 and 3/A).
(7) 1A2A2A4–24	5 mc clock (Q, fig. 20–10).
(8) 1A2A2A4–26	$\overline{\text{5 mc clock}}$ (compliment of 5-mc clock, Q, fig. 20–10).
(9) 1A2A2A4–35	$\overline{\text{Sif enable}}$ (low in modes 1, 2, and 3/A).
(10) 1A2A2A5–6	Reshaped self-test and sif pretriggers (H, fig. 20–11).
(11) 1A2A2A5–18	$\overline{\text{Sif reply enable}}$ (K, fig. 20–11).

d. At the control box, turn the MODE SELECT switch to 1, and continue to hold the CHALLENGE switch at ON.

e. At the synchronizer, use the oscilloscope to observe the mode 1 P1 trigger at 1A2A2A4–31 (V, fig. 20–10).

f. At the control box, turn the MODE SELECT switch to 2, and continue to hold the CHALLENGE switch at ON.

g. At the synchronizer, use the oscilloscope to observe the mode 2 P1 trigger at 1A2A2A4–31 (U, fig. 20–10).

h. At the control box, turn the MODE SELECT switch to 4, and continue to hold the CHALLENGE switch at ON.

i. At the synchronizer, use the oscilloscope to observe the signals at the following two points in any order:

(1) 1A2A2A5J1–2	$\overline{\text{Challenge video}}$, (B, fig. 20–11).
(2) 1A2A2A5–43	$\overline{\text{Gtc trigger}}$, (N, fig. 20–11).

CHAPTER 15

REPLY DECODING CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. REPLY DECODING CIRCUIT TROUBLESHOOTING INFORMATION

15–1. General

a. This chapter provides a troubleshooting procedure to localize any trouble in the reply decoding circuits to a printed wiring card, and a test procedure to test the reply decoding circuits after repair. Most of the reply decoding circuits are physically located in coder-decoder module 1A2A2. The other parts include delay line module 1A2A5, which is time shared with the challenge encoding circuits, and some of the parts on three printed wiring cards within interface module 1A2A1. The troubleshooting procedure is based on the assumptions listed in paragraph 12–2 and the further assumption that the trouble is definitely known to lie in the reply decoding circuits. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12.

b. This section indexes the reply decoding circuit data located in other parts of this manual, and provides a list of the normal reply decoding circuit test indications. Section II provides the reply decoding circuit troubleshooting procedure, section III provides the reply decoding circuit adjustment procedure, and section IV provides the reply decoding circuit test procedure.

15–2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the reply decoding circuits:

Reference	*Data*
Chapter 6	Reply decoding circuit functioning.
Fig. 20–5	Low level line driver card 1A2A1A6 waveforms.
Fig. 20–7	Buffer circuit 1 card 1A2A1A8 waveforms.
Fig. 20–8	Correct code 1 card 1A2A2A2 waveforms.
Fig. 20–9	Correct code 2 card 1A2A2A3 waveforms.
Fig. 20–12	Reply video card 1A2A2A6 waveforms.
Fig. 20–13	I/p and emergency code card 1A2A2A7 waveforms.
Fig. 20–14	Coder-decoder self-test card 1A2A2A8 waveforms.
Fig. 24–8	Reply decoding circuit block diagram.
Fig. 24–9	Reply decoding circuit logic diagram.
Fig. 24–10	Reply decoding circuit timing diagrams.
Fig. 24–17	Synchronizer 1A2 schematic diagram.
Fig. 24–18	Interface module 1A2A1 schematic diagram.
Fig. 24–20	Level shifter card 1A2A1A2 or 1A2A2A1 schematic diagram.
Fig. 24–22	Target video card 1A2A1A4 schematic diagram.
Fig. 24–24	Low level line driver card 1A2A1A6 schematic diagram.
Fig. 24–26	Buffer circuit 1 card 1A2A1A8 schematic diagram.
Fig. 24–27	Coder-decoder module 1A2A2 schematic diagram.
Fig. 24–28	Correct code 1 card 1A2A2A2 schematic diagram.
Fig. 24–29	Correct code 2 card 1A2A2A3 schematic diagram.
Fig. 24–30	Coder card 1A2A2A4 schematic diagram.
Fig. 24–32	Reply video card 1A2A2A6 schematic diagram.
Fig. 24–33	I/p and emergency code card 1A2A2A7 schematic diagram.
Fig. 24–34	Coder-decoder self-test card 1A2A2A8 schematic diagram.

15–3. Adjustments

The reply decoding circuits contain only one ad-

justment potentiometer, physically located in coder-decoder module 1A2A2 (fig. 19-3). In that module, video level adjust potentiometer 1A2A2A6R6 sets the receiver video amplitude threshold at a nominal value of +1.5 volt. That threshold is the level at and above which receiver video pulses from the receiver-transmitter will be accepted, and below which they will be rejected. The received video threshold adjustment procedure is given in paragraph 15-11.

15-4. Normal Test Indications

The following chart lists the normal input, output, and card-to-card signals which are of significance in troubleshooting or testing the reply decoding circuits. The chart also references illustrations which show the location of all points of measurement other than card pins.

Point of measurement	Location (fig. No.)	Normal indication
1A2A1A2J1-4	19-1	Mode 4 enable (high in mode 4).
1A2A1A2J1-5	19-1	Code digit D2 enable (high in sif modes for D2).
1A2A1A2J1-7	19-1	Code digit D4 enable (high in sif modes for D4).
1A2A1A2-18	----	$\overline{\text{Mode 4 enable}}$ (ground from control box in mode 4).
1A2A1A2-22	----	$\overline{\text{Code digit D2 enable}}$ (low from control box for D2).
1A2A1A2-26	----	$\overline{\text{Code digit D4 enable}}$ (low from control box for D4).
1A2A1A4-1	----	Mode 4 enable (high in mode 4).
1A2A1A4-3	----	Mode 4 enable (high in mode 4).
1A2A1A6-7	----	Buffered receiver video (A, fig. 20-5, for an sif code 7777 normal reply).
1A2A1A6-39	----	Triple pulse decoded video (F, fig. 20-5, for a mode 4 reply).
1A2A1A8J1-2	19-1	$\overline{\text{Spoof counter video}}$ (A, fig. 20-7 in test target mode).
1A2A1A8-13	----	(same as at 1A2A1A8J1-2, above).
1A2A2A1J1-1	19-3	Code digit A1 enable (high in sif modes for A1).
1A2A2A1J1-2	19-3	Code digit A2 enable (high in sif modes for A2).
1A2A2A1J1-3	19-3	Code digit A4 enable (high in sif modes for A4).
1A2A2A1J1-4	19-3	Code digit B1 enable (high in sif modes for B1).
1A2A2A1J1-5	19-3	Code digit B2 enable (high in sif modes for B2).
1A2A2A1J1-6	19-3	Code digit C2 enable (high in sif modes for C2).
1A2A2A1J1-7	19-3	Code digit B4 enable (high in sif modes for B4).
1A2A2A1J1-8	19-3	Code digit C1 enable (high in sif modes for C1).
1A2A2A1J1-9	19-3	Code digit C4 enable (high in sif modes for C4).
1A2A2AJ1-10	19-3	Code digit D1 enable (high in sif modes for D1).
1A2A2A1-6	----	$\overline{\text{Code digit A1 enable}}$ (low from control box for A1).
1A2A2A1-10	----	$\overline{\text{Code digit A2 enable}}$ (low from control box for A2).
1A2A2A1-14	----	$\overline{\text{Code digit A4 enable}}$ (low from control box for A4).
1A2A2A1-18	----	$\overline{\text{Code digit B1 enable}}$ (low from control box for B1).
1A2A2A1-22	----	$\overline{\text{Code digit B2 enable}}$ (low from control box for B2).
1A2A2A1-26	----	$\overline{\text{Code digit B4 enable}}$ (low from control box for B4).
1A2A2A1-30	----	$\overline{\text{Code digit C1 enable}}$ (low from control box for C1).

Point of measurement	Location (fig. No.)	Normal indication
1A2A2A1-34	----	Code digit C2 enable (low from control box for C2).
1A2A2A1-38	----	Code digit C4 enable (low from control box for C4).
1A2A2A1-42	----	Code digit D1 enable (low from control box for D1).
1A2A2A2-5	----	18.95 μsec (J, fig. 20-8).
1A2A2A2-7	----	15.95 μsec (K, fig. 20-8).
1A2A2A2-9	----	14.5 μsec (L, fig. 20-8).
1A2A2A2-12	----	17.4 μsec (M, fig. 20-8).
1A2A2A2-14	----	Buffered 15.95 μsec (same as A, fig. 20-8).
1A2A2A2-22	----	C1 through D1 go (N, fig. 20-8).
1A2A2A2-23	----	C1 through D1 kill (P, fig. 20-8).
1A2A2A2-32	----	11.6 μsec (Q, fig. 20-8).
1A2A2A2-35	----	8.7 μsec (R, fig. 20-8).
1A2A2A2-37	----	13.05 μsec (S, fig. 20-8).
1A2A2A2-38	----	Buffered 13.05 μsec (same as F, fig. 20-8).
1A2A2A2-39	----	7.25 μsec (T, fig. 20-8).
1A2A2A3-6	----	20.3 μsec (F, fig. 20-9).
1A2A2A3-7	----	5.8 μsec (G, fig. 20-9).
1A2A2A3-8	----	2.9 μsec (H, fig. 20-9).
1A2A2A3-9	----	4.35 μsec (J, fig. 20-9).
1A2A2A3-10	----	1.45 μsec (K, fig. 20-9).
1A2A2A3-11	----	0.0 μsec (same as P, fig. 20-12).
1A2A2A3-15	----	Buffered 0.0 μsec (same as A, fig. 20-12).
1A2A2A3-23	----	Sif correct code video (M, fig. 20-9).
1A2A2A3-33	----	10-mc clock (same as L, fig. 20-18).
1A2A2A3-36	----	Sif bracket decoded video (P, fig. 20-9).
1A2A2A3-38	----	Sif correct code video (Q or R, fig. 20-9).
1A2A2A6J1-3	19-3	Level adjusted receiver video (B, fig. 20-12, for an sif code 7777 reply).
1A2A2A6J1-8	19-3	Buffered receiver video (G, fig. 20-12, for an sif code 7777 reply).
1A2A2A6-12	----	3.6 μsec (J, fig. 20-12).
1A2A2A6-17	----	Spoof counter video (same as A, fig. 20-7, except inverted; observed in test target mode).
1A2A2A6-18	----	Mode 4 enable (high in mode 4).
1A2A2A6-22	----	Triple pulse decoded video (M, fig. 20-12).
1A2A2A6-24	----	Test target video (same as F, fig. 20-2).
1A2A2A6-26	----	3.6 μsec (N, fig. 20-12).
1A2A2A7-8	----	5-mc clock (same as Q, fig. 20-10).
1A2A2A7-34	----	Reply enable 1 (same as R, fig. 20-10, except inverted).
1A2A2A7-39	----	Mode 2, 3/A enable (high in modes 2 and 3/A).
1A2A2A7-40	----	I/p or emergency video (M or N, fig. 20-13).
1A2A2A8J1-4	19-3	Gtc trigger (same as M or N, fig. 20-11; high when IFF set is not challenging).
1A2A2A8J1-5	19-3	Challenge video (same as A or B, fig. 20-11; high when IFF set is not challenging).
1A2A2A8J2-2	19-3	Reply decoding fault (K, fig. 20-14).
1A2A2A8-5	----	Self-test pretrigger (same as L, fig. 20-19).

Point of measurement	Location (fig. No.)	Normal indication
1A2A2A8-6	----	$\overline{\text{Sif pretrigger}}$ (same as K, fig. 20-19).
1A2A2A8-7	----	$\overline{\text{5-mc clock}}$ (complement of 5-mc clock: Q, fig. 20-10).
1A2A2A8-9	----	$\overline{\text{Code override}}$ (R, fig. 20-14).
1A2A2A8-13	----	Mode 4 pretrigger (same as K, fig. 20-18, except inverted).
1A2A2A8-17	----	Reshaped self-test and sif pretriggers (same as H, fig. 20-11).
1A2A2A8-19	----	$\overline{\text{Reshaped self-test pretrigger}}$ (S, fig. 20-14).
1A2A2A8-20	----	$\overline{\text{Reshaped self-test pretrigger}}$ (same as S, fig. 20-14).
1A2A2A8-22	----	$\overline{\text{Code override}}$ (same as E, fig. 20-14 except inverted).
1A2A2A8-28	----	$\overline{\text{Isls gate}}$ (same as W, fig. 20-10 in mode 3/A; high when IFF set is not challenging).

Section II. REPLY DECODING CIRCUIT TROUBLESHOOTING CHART

15-5. General

Most of the troubleshooting or testing of the reply decoding circuits can be carried out in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. However, for those circuits which are exercized only in other modes, the troubleshooting procedure specifies mode switching at the appropriate steps.

15-6. Test Equipment Required

The reply decoding circuit troubleshooting procedure is based on operation of the defective synchronizer as part of the complete hot mockup shown in figure 24-16. The test equipment required is therefore the same as shown in that figure and listed in paragraph 12-4. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

15-7. Preparation for Troubleshooting

The preparation required for troubleshootiing of the reply decoding circuits is the same as for overall synchronizer troubleshooting (para 12-5). Therefore, if the synchronizer is already connected into the complete hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, proceed as directed in paragaph 12-5.

15-8. Troubleshooting Chart

a. Preliminary procedure.

(1) After all preparations have been made for troubleshooting the reply decoding circuits, set the synchronizer POWER circuit breaker, the control box POWER circuit breaker and the interrogator group POWER circuit breaker to ON.

(2) If the CODER DECODER FAULT lamp on the front panel of the synchronizer is lighted continuously with the CHALLENGE switch on the control box released (at OFF), proceed with steps 1 through 11 of the following chart. These steps may be undertaken immediately; it is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended. Observe the signals at the indicated test points, proceeding in step number order unless otherwise directed in the corrective measures column.

(3) If the CODER DECODER FAULT lamp is not lighted, wait until the receiver-transmitter warmup delay has ended. Then disregard steps 1 through 11 of the following chart, prepare the hot mockup as directed for steps 12 through 31 in the chart, and proceed with step 12. Observe the signals at the indicated test points in step number order unless otherwise directed in the corrective measures column.

b. Reply Decoding Circuit Troubleshooting Chart.

Step	Test point	Test equipment	Normal indication	Corrective measures
1	1A2A2A8-20	Oscilloscope	$\overline{\text{Reshaped self-test pretrigger}}$ (S, fig. 20-14).	Coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.
2	1A2A2A8-19	Oscilloscope	$\overline{\text{Reshaped self-test pretrigger}}$ (same as S, fig. 20-14).	Coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.
3	1A2A2A8-22	Oscilloscope	$\overline{\text{Code override}}$ (same as R, fig. 20-14 except inverted).	If normal, proceed with step 8. If abnormal, proceed with step 4.
4	1A2A2A8-9	Oscilloscope	$\overline{\text{Code override}}$ (R, fig. 20-14).	If abnormal, proceed with step 5. If normal proceed to step 7.
5	1A2A2A8-10	Oscilloscope	Sif correct code video (same as M, fig. 20-9).	If abnormal, proceed as follows: *a.* Measure level at 1A2A2A3-40 (high). If not high, i/p and emergency code card 1A2A2A7 is defective; refer to chapter 20, section XV. *b.* Observe $\overline{\text{C1-D1}}$ go pulse at 1A2A2A3-5 (Same as N, fig. 20-8). If normal, correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section XI. If abnormal, correct code 1 card 1A2A2A2 is defective; refer to chapter 20, section X.
.6	1A2A2A8-18	Oscilloscope	Sif bracket decoded video (same as P, fig. 20-9, except inverted).	If abnormal, correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section XI. If normal self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI.
7	1A2A2A8-3	Oscilloscope	Triple pulse decoded video (same as F, fig. 24-5).	If normal, coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI. If abnormal, reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV.
8	1A2A2A8-15	Oscilloscope	Buffered 1.8 μsec (same as L, fig. 20-12).	If abnormal, reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV.
9	1A2A2A8-8	Oscilloscope	Buffered 3.6 μsec (same as K, fig. 20-12).	If abnormal, reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV.

Step	Test point	Test equipment	Normal indication	Corrective measures
10	1A2A2A8-24	Oscilloscope	$\overline{\text{C1-D1}}$ kill (eight negative-going pulses: same as L, fig. 20-9).	If abnormal, observe eight C1-D1 kill pulses at 1A2A2XA3-26 (same as P, fig. 20-8). If normal, correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section XI. If abnormal, correct code 1 card 1A2A2A2 is defective; refer to chapter 20, section X.
11	1A2A2A8-21	Oscilloscope	$\overline{\text{B2-D4}}$ kill (four negative-going pulses: same as N, fig. 20-9).	If normal, coder-decoder self-test card 1A2A2A8 is defective; refer to chapter 20, section XVI. If abnormal, correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section XI.

STEPS 12 THROUGH 31 ASSUME THAT A REPLY DECODING FAULT IS PRESENT, BUT THAT THE "CODER DECODER FAULT" LAMP IS NOT LIGHTED. THESE STEPS ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 3/A AND RECEIVING A CORRECTLY CODED MODE 3/A REPLY:

AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "3/A," AND WITH "CODE SELECT" SWITCHES AT "7777."

AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.

FOR STEP 27, CHANGE SIMULATED MODE 3/A REPLY TO I/P (CODE 7777) AT RADAR TEST SET.

FOR STEP 28, CHANGE SIMULATED MODE 3/A REPLY TO EMERGENCY (CODE 7700) AT RADAR TEST SET. THEN, AT CONTROL BOX, CHANGE "MODE 3/A CODE SELECT" SWITCH SETTINGS TO "7700."

12	1A2A2A6J1-8	Oscilloscope	Buffered receiver video (G, fig. 20-12).	If abnormal, perform adjustment procedure for video level adjust potentiometer 1A2A2A6R6 as described in paragraph 15-11. If still abnormal, reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV.
13	1A2A2A3-36	Oscilloscope	Sif bracket decoded video (P, fig. 20-9).	If abnormal, inverter A13D on correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section XI.
14	1A2A2A3-38	Oscilloscope	Sif correct code video (Q, fig. 20-9).	If abnormal, proceed with step 15. If normal, the fault is a mode 4 reply decoding fault; disregard steps 15 through 28, and proceed with step 29.
15	1A2A2A3-37	Oscilloscope	Sif correct code enable (high).	If abnormal, coder card 1A2A2A4 is defective; refer to chapter 20, section XII.

Step	Test point	Test equipment	Normal indication	Corrective measures
16	1A2A2A3-40	Oscilloscope	I/p or emergency video (high).	If abnormal, i/p and emergency code card 1A2A2A7 is defective; refer to chapter 20, section XV.
17	1A2A2A1J1-8	Oscilloscope	A1 enable (high)	If not high, level shifter card 1A2A2A1 is defective; refer to chapter 20, section III.
18	1A2A2A1J1-1	Oscilloscope	A2 enable (high)	Same as step 15.
19	1A2A2A1J1-6	Oscilloscope	A4 enable (high)	Same as step 15.
20	1A2A2A1J1-2	Oscilloscope	B1 enable (high)	Same as step 15.
21	1A2A2A1J1-9	Oscilloscope	B2 enable (high)	Same as step 15.
22	1A2A2A1J1-3	Oscilloscope	C2 enable (high)	Same as step 15.
23	1A2A2A1J1-4	Oscilloscope	B4 enable (high)	Same as step 15.
24	1A2A2A1J1-10	Oscilloscope	C1 enable (high)	Same as step 15.
25	1A2A2A1J1-5	Oscilloscope	C4 enable (high)	Same as step 15.
26	1A2A2A1J1-7	Oscilloscope	D1 enable (high)	Same as step 15.
27	1A2A1A2J1-5	Oscilloscope	D2 enable (high)	If not high, level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
28	1A2A1A2J1-7	Oscilloscope	D4 enable (high)	Same as step 25.
29	1A2A2A3-38	Oscilloscope	Sif correct code video (R, fig. 20-9).	If normal proceed with step 31. If abnormal proceed with step 30.
30	1A2A2A3-40	Oscilloscope	I/p or emergency video (same as M, fig. 20-13).	If abnormal i/p and emergency code card 1A2A2A7 is defective; refer to chapter 20, section XV. If normal AND A13A on correct code 2 card 1A2A2A3 is defective; refer to chapter 20, section II.
31	1A2A2A3-40	Oscilloscope	I/P or emergency video (same as N, fig. 20-13).	If abnormal, i/p and emergency code card 1A2A2A7 is defective; refer to chapter 20. section X. If normal, the fault is a mode 4 reply decoding fault; proceed with step 32.
			STEPS 32 THROUGH 37 ASSUME THAT A MODE 4 REPLY DECODING FAULT IS PRESENT. BUT THAT THE "CODER DECODER FAULT" LAMP IS NOT LIGHTED. THEREFORE STEPS 29 THROUGH 32 ARE TO BE	

Step	Test point	Test equipment	Normal indication	Corrective measures
			CARRIED OUT WHILE CHALLENGING IN MODE 4 AND RECEIVING A MODE 4 REPLY: MODIFY HOT MOCKUP TO SIMULATE AN RF MODE 4 REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 470 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "4." FOR STEPS 36 AND 37, SELECT TEST TARGET MODE BY HOLDING "CHALLENGE" SWITCH AT "TEST."	
32	1A2A1A6-93	Oscilloscope	Triple pulse decoded video (F, fig. 20-5).	If normal, proceed with step 36. If abnormal, proceed with step 33.
33	1A2A2A6-22	Oscilloscope	Spoof counter video (same as M, fig. 20-12 except inverted).	If normal, line driver Q6 on low level line driver card 1A2A1A6 is defective; refer to chapter 20, section VII. If abnormal, proceed with step 34.
34	1A2A2A6-18	Oscilloscope	Mode 4 enable (high)	If high, AND A2A on reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV. If not high, proceed with step 35.
35	1A2A1A2J1-4	Oscilloscope	Mode 4 enable (high)	If high, inverter A13A or A13B on target video card 1A2A1A4 is defective; refer to chapter 20, section V. If not high, level shifter Q4 on shifter board 1A2A1A2 is defective; refer to chapter 20, section III.
36	1A2A1A8J1-2	Oscilloscope	Spoof counter video (A, fig. 20-7, observed in test target mode).	If abnormal, proceed with step 37.

Step	Test point	Test equipment	Normal indication	Corrective measures
37	1A2A2A6–23 _____	Oscilloscope _____	Spoof counter video (same as A, fig. 20–7, except inverted; also observed in test target mode).	If normal, inverter A4A on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. If abnormal, OR A8B on reply video card 1A2A2A6 is defective; refer to chapter 20, section XIV.

Section III. ADJUSTMENT OF REPLY DECODING CIRCUITS

15–9. General

The only reply decoding circuit adjustment is the receiver video threshold adjustment made by means of video level adjust potentiometer 1A2A2A6R6 on the reply video card. This potentiometer is adjusted so that each receiver video pulse having an amplitude greater than 1.5 volt and a width greater than 0.25 μsec at the 1.5-volt amplitude points will be accepted as a potentially valid reply pulse. The acceptance is indicated by the appearance of the pulse as a buffered receiver video pulse at BUFFERED VIDEO receptacle 1J3 on the interrogator group case.

15–10. Test Equipment and Preparation

a. Like the troubleshooting procedure given in section II of this chapter, the receiver video threshold adjustment is based on operation of the synchronizer as part of a hot mockup. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator is not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set.

(3) 28-volt dc power supply.

(4) Test facilities set.

b. For complete test equipment nomenclature and a list of test equipment manuals, refer to paragraph 11–7.

c. If the synchronizer is not already connected into a complete hot mockup, make all connections shown in figure 24–16 except do not connect the mode 4 word generator shown in that figure.

d. Set the hot mockup controls as directed in paragraph 12–5, except disregard the mode 4 word generator control settings given in paragraph 12–5*h*. (If the mode 4 word generator is already connected, set its power ON–OFF switch to OFF.)

15–11. Receiver Video Threshold Adjustment

a. After all preparations have been made, set the synchronizer POWER circuit breaker and interrogator set POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON. Then, after the receiver-transmitter 60-second warmup delay has ended, set the MODE SELECT switch to 3/, and hold the CHALLENGE switch at ON.

c. At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

d. Using the oscilloscope, observe the receiver video pulses on the front panel of the receiver-transmitter, at pin F of TEST receptacle 1A3J1, to verify that their amplitude is at least 1.5 volt. The waveform should be similar to A, figure 20–5.

e. Reconnect the oscilloscope to observe the buffered receiver video pulses (A, fig. 20–5) at BUFFERED VIDEO receptacle 1J3 on the rear of the interrogator group case, terminating 1J3 in 75 ohms ±10 percent resistive.

NOTE

Buffered receiver video pulses will not appear at 1J3 if video level adjust potentiometer 1A2A2A6R6 is turned too far coun-

terclockwise. If the pulses do not appear, and if they cannot be made to appear by clockwise rotation of 1A2A2A6R6, reply video card 1A2A2A6 or low level line driver card 1A2A1A6 is defective. Refer to section II.

f. Adjust video level adjust potentiometer 1A2A2A6R6: first counterclockwise until the buffered receiver video pulses at 1J3 disappear; then slowly clockwise until the buffered receiver video pulses just reappear, and an additional 1½ turns clockwise.

Section IV. REPLY DECODING CIRCUIT TESTING

15–12. General

The reply decoding circuits are most effectively tested by observing their outputs to other synchronizer circuits and to other parts of the IFF set, using an oscilloscope. Most of the observations can be made in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. The remaining observations, made in other modes, check only the functions which are not adequately checked in mode 3/A.

15–13. Test Equipment and Preparation

Like the troubleshooting procedure given in section II of this chapter, the reply decoding circuit test observations are made with the synchronizer in operation as part of the complete hot mockup shown in figure 24–16. The test equipment required is therefore the same as listed in paragraph 12–4, and the preparation procedure is the same as given for overall synchronizer troubleshooting in paragraph 12–5.

15–14. Test Procedure

a. After all preparations have been made, set the synchronizer POWER circuit breaker and interrogator set POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON, and note that the SYN SELF TEST lamp does not light; or, if it does light, that it does not remain lighted for longer than one second.

c. At the synchronizer, use the oscilloscope to observe the signals at all of the following points in any desired order.

NOTE

These observations may be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(1) 1A2A2A2–14: buffered 15.95 μsec (same as A, fig. 20–8).

(2) 1A2A2A2–38: buffered 13.05 μsec (same as F, fig. 20–8).

(3) 1A2A2A3–36: $\overline{\text{sif}}$ bracket decoded video (P, fig. 20–9).

(4) 1A2A2A3–38: $\overline{\text{sif}}$ correct code video (Q, fig. 20–9).

(5) 1A2A2A8J2–2: reply decoding fault (K, fig. 20–14).

d. At the control box, set the MODE SELECT switch to 3/A, and hold the CHALLENGE switch at ON.

e. At the radar test set after the receiver-transmitter 60-second warmup delay has ended, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse (B, fig. 20–12) 500 μsec after the simulated radar trigger applied to 1J1.

f. At the synchronizer, use the oscilloscope to observe the signals at both of the following two points in any desired order:

(1) 1A2A2A6J1–8: buffered receiver video (G, fig. 20–12).

(2) 1A2A1A6–7: buffered receiver video (A, fig. 20–5).

g. At radar test set, change the simulated mode 3/A normal reply to a mode 3/A code 7777 i/p reply.

h. At the synchronizer, use the oscilloscope to observe one i/p or emergency video pulse (M, fig. 20–13) at 1A2A2A7–40.

i. At the radar test set, change the simulated mode 3/A i/p reply to a mode 3/A emergency reply (code 7700).

j. At the control box, change the MODE 3/A CODE SELECT switch settings to 7700.

k. At the synchronizer, use the oscilloscope to observe three i/p or emergency video pulses (N, fig. 20–13) at 1A2A2A7–40.

l. At the control box, release the CHALLENGE switch (to OFF).

m. Modify the hot mockup to simulate an RF mode 4 reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 470 μsec after the simulated radar trigger applied to 1J1.

n. At the control box, set the MODE SELECT switch to 4, and hold the CHALLENGE switch at ON.

o. At the synchronizer, use the oscilloscope to observe one triple pulse decoded video pulse (F, fig. 20–5) at 1A2A1A6–39.

p. At the control box, select the test target mode by holding the CHALLENGE switch at TEST.

q. At the synchronizer, observe the spoof counter video pulses (same as A, fig. 20–7) at 1A2A1A8–13.

CHAPTER 16

DISPLAY VIDEO INTERFACE CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. DISPLAY VIDEO INTERFACE CIRCUIT TROUBLESHOOTING INFORMATION

16-1. General

a. This chapter provides troubleshooting procedure to localize any trouble in the display video interface circuits to a printed wiriing card, and a test procedure to test the display video interface circuits after repair. The display video interface circuits are physically located within interface module 1A2A1. The troubleshooting procedure is based on the assumptions listed in paragraph 12-2 and the further assumption that the trouble is definitely known to lie in the display video interface circuits. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12.

b. This section indexes the display video interface circuit data located in other parts of this manual, and provides a list of the normal display video interface circuit test indications. Section II provides the display video interface circuit troubleshooting procedure, section III provides the display video interface circuit adjustment procedures, and section IV provides the display video interface circuit test procedure.

16-2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the display video interface circuits:

Reference	*Data*
Chapter 7	Display video interface circuit functioning.
Fig. 20-1	Interface self-test card 1A2A1A1 waveforms.
Fig. 20-2	Test target generator card 1A2A1A3 waveforms.
Fig. 20-3	Target video card 1A2A1A4 waveforms.
Fig. 20-4	Display video card 1A2A1A5 waveforms.
Fig. 20-7	Buffer circuit 1 card 1A2A1A8 waveforms.
Fig. 24-11	Display video interface circuit block diagram.
Fig. 24-12	Display video interface logic diagram.
Fig. 24-13	Display video interface timing diagrams.
Fig. 24-17	Synchronizer 1A2 schematic diagram.
Fig. 24-18	Interface module 1A2A1 schematic diagram.
Fig. 24-19	Interface self-test card 1A2A1A1 schematic diagram.
Fig. 24-20	Level shifter card 1A2A1A2 schematic diagram.
Fig. 24-21	Test target generator card 1A2A1A3 schematic diagram.
Fig. 24-22	Target video card 1A2A1A4 schematic diagram.
Fig. 24-23	Display video card 1A2A1A5 schematic diagram.
Fig. 24-26	Buffer circuit 1 card 1A2A1A8 schematic diagram.

16-3. Controls and Adjustments

The display video interface circuits contain four adjustment potentiometers within interface module 1A2A1 (fig. 19-1). Potentiometer 1A2A1A3R2 on the test target generator card is adjusted for a display gate width of 178 μsec by means of the display gate width adjustment procedure given in paragraph 16-11. The three potentiometers on the display video card are adjusted by means of the IFF display video adjustment procedure given in paragraph 16-12: 1A2A1A5R1 for a target present pulse width of 1.0 μsec; 1A2A1A5R2 for a friend pulse amplitude of 5.0 volts; and 1A2A1A5R3 for a friend pulse width of 5.0 μsec.

16-4. Normal Test Indications

The following chart lists the normal input, output, and card-to-card signals which are of significance in troubleshooting the display video interface circuits. For the physical locations of points of measurement other than card pins, refer to figure 19-1.

Point of measurement	*Normal indication*
1A2A1A1J1-4	Delayed video fault (B, fig. 20-1).
1A2A1A1J1-7	Decoded reply fault (E, fig. 20-1).
1A2A1A1J1-10	Friend fault (high level).
1A2A1A1J2-6	Target fault (high level).
1A2A1A1-5, or 1A2A1A4-5.	Sif bracket decoded video (same as Q, fig. 20-9).
1A2A1A1-6, or 1A2A1A4-19.	Sif correct code video (same as R, fig. 20-9).
1A2A1A1-14	Reshaped mode 4 pretrigger (same as C, fig. 20-6).
1A2A1A1-20, or 1A2A1A3-22, or 1A2A1A5-22.	Processor start pretrigger (same as J, fig. 20-18).
1A2A1A1-32	Self-test pretrigger (same as M, fig. 20-19, except inverted).
1A2A1A1-34 or 1A2A1A8-12.	Eyelash enable (low level).
1A2A1A1-35	Interface fault (low level).
1A2A1A2J1-4	Mode 4 enable (high in mode 4).
1A2A1A2J1-6	Bracket decode enable (high when SIF REPLIES switch on control box is held at ALL).
1A2A1A2J1-8, or 1A2A1A8-33.	Processor bypass enable (high when PROCESSOR switch on control box is at BYPASS).
1A2A1A2J1-9	Test target enable (high when CHALLENGE switch on control box is held at TEST).
1A2A1A2-18	Mode 4 enable (ground from control box in mode 4).
1A2A1A2-30	Processor bypass enable (ground from control box when PROCESSOR switch is at BYPASS).
1A2A1A2-34	Bracket decode enable (ground from control box when SIF REPLIES switch is held at ALL).
1A2A1A2-38	Test target enable (ground from control box when CHALLENGE switch is held at TEST).
1A2A1A3J1-6	Test target video (F, fig. 20-2).
1A2A1A3-12	Display gate (J, fig. 20-2).
1A2A1A4-3	Mode 4 enable (high in mode 4).
1A2A1A4-12	Mode 4/test target enable (low in mode 4 and low when CHALLENGE switch on control box is held at TEST).
1A2A1A4-13	Sif reply enable (same as K, fig. 20-11, except inverted).
1A2A1A4-18	Sif reply enable (same as K, fig. 20-11).
1A2A1A4-22	Friend reset (H, fig. 20-3).
1A2A1A4-30	Delayed target video (J, fig. 20-3).
1A2A1A4-31	Delayed target video (same as J, fig. 20-3, except inverted).
1A2A1A4-33	5-mc clock (complement of 5-mc clock: same as Q, fig. 20-10).
1A2A1A4-34	Friend threshold (same as L, fig. 20-3, except inverted).
1A2A1A4-35	Decoded reply video (K, fig. 20-3).
1A2A1A4-36	Friend threshold (L, fig. 20-3).
1A2A1A4-37	Friend (M, fig. 20-3).
1A2A1A4-40, or 1A2A1A5-20.	Tail trigger (N, fig. 20-3).
1A2A1A4-43	Friend (same as M, fig. 20-3, except inverted).
1A2A1A5J1-9	Friend pulse (F, fig. 20-4).
1A2A1A5-6	IFF display video (H or J, fig. 20-4).
1A2A1A5-28	Target present trigger (K, fig. 20-4).
1A2A1A5-36	Friend stored (same as L, fig. 20-4, except inverted).
1A2A1A8J1-9	Target (B, fig. 20-7).
1A2A1A8-5	Sif enable (low in modes 1, 2, and 3/A).

Point of measurement	*Normal indication*
1A2A1A8-9	Eyelash enable (high level).
1A2A1A8-24	$\overline{\text{Target gated}}$ (same as C, fig. 20-7, except inverted).
1A2A1A8-27	Target gated (C, fig. 20-7).
1A2A1A8-30	$\overline{\text{Processor self-test gate}}$ (same as D, fig. 20-7, except inverted).
1A2A1A8-31	Processor self-test gate (D, fig. 20-7).
1A2A1A8-32	Mode 4 time decoded video (same as F, fig. 20-5).
1A2A1A8-34	$\overline{\text{Processor bypass enable}}$ (low when PROCESSOR switch on control box is at BYPASS).
1A2A1A8-36	$\overline{\text{Target}}$ (same as B, fig. 20-7, except inverted).
1A2A1A8-37	Mode 4 time decoded/test target video (same as F, fig. 20-5, in mode 4; same as F, fig. 20-2, except inverted, in test target mode).
1A2A1A8-39	$\overline{\text{Strobe}}$ (same as E, fig. 20-7, except inverted).
1A2A1A8-40	Strobe (E, fig. 20-7).

Section II. DISPLAY VIDEO INTERFACE CIRCUIT TROUBLESHOOTING CHART

16-5. General

Most of the troubleshooting or testing of the display video interface circuits can be carried out in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. However, for those circuits which are exercised only in other modes, the troubleshooting procedure specifies mode switching at the appropriate steps.

16-6. Test Equipment Required

The display video interface circuit troubleshooting procedure is based on operation of the defective synchronizer as part of the complete hot mockup shown in figure 24-16. The test equipment is therefore the same as shown in that figure and listed in paragraph 12-4. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

16-7. Preparation for Troubleshooting

The preparation required for troubleshooting of the display video interface circuits is the same as for overall synchronizer troubleshooting (para 12-5). Therefore, if the synchronizer is already connected into the hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, proceed as directed in paragraph 12-5.

16-8. Troubleshooting Chart

a. Preliminary Procedure. After all preparations have been made for troubleshooting the display video interface circuits, proceed as follows:

(1) Set the POWER circuit breakers on synchronizer, control box, and interrogator group case to ON.

(2) At the control box, enable the test target mode by holding CHALLENGE switch at TEST. At the synchronizer, use the oscilloscope to verify the friend threshold and friend input signals at the following points in either order:

NOTE

It is not necessary to wait for the receiver-transmitter 60-second warmup delay to end before observing these signals.

(*a*) 1A2A1A4-36, $\overline{\text{friend threshold}}$ (L, fig. 20-3).

(*b*) 1A2A1A4-37, $\overline{\text{friend}}$ (M, fig. 20-3).

(3) At the control box, after the receiver-transmitter 60-second warmup delay has ended, challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first pulse appears at 1A2A2A6J1-

3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) At the synchronizer, use the oscilloscope to verify the processor self-test gate, target, and strobe input signals at the following points in any desired order:

(*a*) 1A2A1A8–30, processor self-test gate (same as D, fig. 20–7, except inverted).

(*b*) 1A2A1A8–36 target (same as B, fig. 20–7, except inverted).

(*c*) 1A2A1A8–39 strobe (same as E, fig. 20–7, except inverted).

(6) If the INTERFACE FAULT lamp on the front panel of the synchronizer is lighted, proceed with steps 1 through 10 of the following chart. Observe the signals at the indicated test points, proceeding in step number order unless otherwise directed in the corrective measures column.

(7) If, instead, the INTERFACE FAULT lamp is not lighted, disregard steps 1 through 10 of the following chart, and proceed with step 11. Observe the signals at the indicated test points in step number order unless otherwise directed in the corrective measures column.

b. Display Video Interface Circuit Troubleshooting Chart.

Step	Test point	Test equipment	Normal indication	Corrective measures
1	1A2A1A1J1–7	Oscilloscope	Decoded reply fault (E, fig. 20–1).	If normal, proceed with step 3. If abnormal, perform step 2.
2	1A2A1A1–10	Oscilloscope	Decoded reply video (same as K, fig. 20–3).	If normal, interface self-test card 1A2A1A1 is defective; refer to chapter 20, section II. If abnormal, target video card 1A2A1A4 is defective; refer to chapter 20, section V.
3	1A2A1A1J1–4	Oscilloscope	Delayed video fault (B, fig. 20–1).	If normal, proceed with step 5. If abnormal, perform step 4.
4	1A2A1A1–11	Oscilloscope	Delayed target video (same as J, fig. 20–3, except inverted).	If normal, interface self-test card 1A2A1A1 is defective; refer to chapter 20, section II. If abnormal, target video card 1A2A1A4 is defective; refer to chapter 20, section V.
5	1A2A1A1J2–6	Oscilloscope	Target fault (high)	If normal, proceed with step 8. If abnormal, proceed with step 6.
6	1A2A1A1–22	Oscilloscope	Target present trigger (same as K, fig. 20–4).	If normal, interface self-test card 1A2A1A1 is defective; refer to chapter 20, section II. If abnormal, perform step 7.
7	1A2A1A1–36	Oscilloscope	Target gated (same as C, fig. 20–7).	If normal, display video card 1A2A1A5 is defective: refer to chapter 20, section VI. If abnormal, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

Step	Test point	Test equipment	Normal indication	Corrective measures
			STEPS 8 THROUGH 10 ASSUME THAT MODE 4 FAULT IS PRESENT IN THE DISPLAY VIDEO INTERFACE CIRCUITS AND THE "INTERFACE FAULT" LAMP IS LIGHTED. FOR THESE STEPS, HOLD "CHALLENGE" SWITCH ON CONTROL BOX AT "TEST."	
8	1A2A1A1J1–10	Oscilloscope	Friend fault (high)	If normal, interface self-test card 1A2A1A1 is defective; refer to chapter 20, section II. If abnormal, proceed with step 9.
9	1A2A1A1–24	Oscilloscope	Friend stored (same as L, fig. 20–4, except inverted).	If normal, interface self-test card 1A2A1A1 is defective; refer to chapter 20, section II. If abnormal, proceed with step 10.
10	1A2A1A5–12	Oscilloscope	Friend reset (same as H, fig. 20–3).	If normal, display video card 1A2A1A5 is defective; refer to chapter 20, section VI. If abnormal, target video card 1A2A1A4 is defective; refer to chapter 20, section V.
			STEPS 11 THROUGH 34 ASSUME THAT A FAULT IS PRESENT IN THE DISPLAY VIDEO INTERFACE CIRCUITS, BUT THE "INTERFACE FAULT" LAMP IS NOT LIGHTED. THESE STEPS ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 3/A AND BRACKET DECODING AN SIF REPLY WITH THE PROCESSOR BYPASSED: *a.* AT CONTROL BOX, SET "PROCESSOR" SWITCH TO "BYPASS." THEN HOLD "CHALLENGE" SWITCH AT "ON" AND "SIF REPLIES" SWITCH AT "ALL." *b.* AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT	

Step	Test point	Test equipment	Normal indication	Corrective measures
			1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.	
11	1A2A1A4-35	Oscilloscope	Decoded reply video (K, fig. 20-3).	If normal, proceed with step 14. If abnormal, proceed with step 12.
12	1A2A1A2J1-6	Oscilloscope	Bracket decode enable (high)	If abnormal, level shifter Q8 and/or its associated circuitry on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III. If normal, proceed with step 13.
13	1A2A1A4-13	Oscilloscope	Sif reply enable (same as K, fig. 20-11, except inverted).	If normal, interface self-test card 1A2A1A1 and target video card 1A2A1A4 are defective; refer to chapter 20, sections II and V. If abnormal, inverter A14C on target video card 1A2A1A4 is defective; refer to chapter 20, section V.
14	1A2A1A5-6	Oscilloscope	IFF display video (H, fig. 20-4).	If normal, proceed with step 23. If abnormal, adjust target present pulse width potentiometer 1A2A1A5R1 as described in paragraph 16-12. If still abnormal, proceed with step 15.
15	1A2A1A5-30	Oscilloscope	Display gate (same as J, fig. 20-2).	If abnormal, observe processor self-test gate at 1A2A1A8-31 (D, fig. 20-7). If normal, display gate generation circuit on test target generator card 1A2A1A3 is defective; refer to chapter 20, section IV. If abnormal, inverter A6D and/or A6C on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
16	1A2A1A5-39	Oscilloscope	Delayed target video (same as J, fig. 20-3).	If abnormal, target video card 1A2A1A4 is defective; refer to chapter 20, section V.
17	1A2A1A5-10	Oscilloscope	Strobe (same as E, fig. 20-7).	If abnormal, inverter A7C on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

Step	Test point	Test equipment	Normal indication	Corrective measures
18	1A2A1A5-24	Oscilloscope	Target gated (same as C, fig. 20-7, except inverted).	If abnormal, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
19	1A2A1A5-16	Oscilloscope	Target gated (same as C, fig. 20-7).	If abnormal, inverter A6A on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
20	1A2A1A2J1-8	Oscilloscope	Processor bypass enable (high).	If abnormal, level shifter Q7 and/or its associated circuitry on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
21	1A2A1A5-27	Oscilloscope	Processor bypass enable (low).	If abnormal, inverter A7A on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
22	1A2A1A5-28	Oscilloscope	Target present trigger (K, fig. 20-4).	If normal, IFF video reshaping circuit on display video card 1A2A1A5 is defective; refer to chapter 20, section VI. If abnormal, interface self-test card 1A2A1A1 and the target generation circuit on display video card 1A2A1A5 are defective; refer to chapter 20, sections II and VI.
			FOR STEPS 23 THROUGH 32, HOLD "CHALLENGE" SWITCH ON CONTROL BOX AT "TEST."	
23	1A2A1A5J1-9	Oscilloscope	Friend pulse (F, fig. 20-4)	If normal, proceed with step 30. If abnormal, adjust friend pulse width potentiometer 1A2A1A5R3 as described in paragraph 16-12. If still abnormal, proceed with step 24.
24	1A2A1A4J1-3		Mode 4 time decoded video/ test target video (same as F, fig. 20-2, except inverted).	If normal, proceed with step 28. If abnormal, proceed with step 25.
25	1A2A1A4-9		Mode 4 time decoded video/ test target video (same as F, fig. 20-2, except inverted).	If normal, proceed with step 27. If abnormal, proceed with step 26.
26	1A2A1A3J1-6		Test target video (F, fig. 20-2).	If normal, A7D or Q5 and/or its associated circuitry on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. If abnormal, test tar-

Step	Test point	Test equipment	Normal indication	Corrective measures
				get generator card 1A2A1A3 is defective; refer to chapter 20, section IV.
27	1A2A1A2J1-9	Oscilloscope	Test target enable (high)	If normal, interface self-test card 1A2A1A1 and target video card 1A2A1A4 are defective; refer to chapter 20, sections II and V. If abnormal, level shifter Q9 and/or its associated circuitry on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
28	1A2A1A5-26		Eyelash enable (high)	If normal, proceed with step 29. If abnormal, AND A4C on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.
29	1A2A1A5-18		Friend (same as M, fig. 20-3, except inverted).	If normal, display video card 1A2A1A5 is defective; refer to chapter 20, section VI. If abnormal, AND A16A or AND A16D on target video card 1A2A1A4 is defective; refer to chapter 20, section V.
30	1A2A1A5-6	Oscilloscope	IFF Display video (J, fig. 20-4).	If normal, proceed to step 33. If abnormal, proceed to step 31.
31	1A2A1A5-27		Processor bypass enable (high).	If normal, AND A7A on display video card 1A2A1A5 is defective; refer to chapter 20, section VI. If abnormal, proceed to step 32.
32	1A2A1A2J1-8		Processor bypass enable (low).	If normal, AND A7A on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. If abnormal, level shifter Q7 and/or its associated circuitry on level shifter card 1A2A1A2 is defective; refer to chapter 20, section III.
			STEPS 33 AND 34 ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 4. AT CONTROL BOX, SET "MODE SELECT" SWITCH TO 4. AND HOLD "CHALLENGE" SWITCH AT "ON."	

Step	Test point	Test equipment	Normal indication	Corrective measures
33	1A2A1A5-38 _____	Oscilloscope _____	Mode 4/Test target enable (high).	If normal, the trouble is a mode 4 time decoded video fault. Either AND A7D or video amplifier Q5 and/or its associated circuitry or buffer circuit 1 card is defective; refer to chapter 20, section IX. If abnormal, proceed to step 34.
34	1A2A1A2J1-4 _____	_____	Mode 4 enable (high) _____	If normal, inverter A13A or inverter A13B on target video card 1A2A1A4 is defective; refer to chapter 20, section V. If abnormal, level shifter Q4 and/or its associated circuitry on level shifter 1A2A1A2 is defective; refer to chapter 20, section III.

Section III. ADJUSTMENT OF DISPLAY VIDEO INTERFACE CIRCUITS

16-9. General

The display video interface circuit adjustments are the display gate width adjustment made by means of the one potentiometer on test target generator card 1A2A1A3 and the IFF display video adjustments made by means of the three potentiometers on display video card 1A2A1A5. Neither challenging nor simulated replies are required for these adjustments, because the display gate width adjustment is made with the IFF set not challenging, and the IFF display video adjustments are made with the IFF set operating in the test target mode. The display gate width adjustment is made by observing the display gate and setting its width to 178 μsec. For the IFF display video adjustments, the IFF display video is observed in the test target mode, and the superimposed target present and friend pulses are examined. Then the target present pulse width is adjusted to 1.0 μsec, the friend pulse width is adjusted to 5.0 μsec, and the friend pulse amplitude is adjusted to 5.0 volts.

16-10. Test Equipment and Preparation

a. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facility set are not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set (only to supply "O" TRIGGER output to 1J1).

(3) 28-volt dc power supply.

(4) Test facilities set (only for cables W32, W41, W42, and W47).

b. For complete test equipment nomenclature and a list of test equipment manuals, refer to paragraph 11-7.

c. At the synchronizer, turn POWER circuit breaker OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, disregard step *d* and proceed with step *e*.

d. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24-16.

e. At the control box, turn OFF the POWER circuit breaker, and check that the CHALLENGE switch is released (to OFF). The other switch settings are immaterial for purposes of display video interface circuit adjustment.

f. At the interrogator group case, set the POWER circuit breaker to ON.

g. At the radar test set, turn ON the POWER switch, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12-5*e*(3).

h. Set the controls on the oscilloscope as directed in paragraph 12-5*f*.

i. Turn on the 28-volt dc power supply.

16-11. Display Gate Width Adjustment

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON.

NOTE

Steps *c* and *d* may be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

c. Observe the display gate (J, fig. 20-2) at 1A2A1A3-12, using the oscilloscope.

d. If the display gate width is not 178 μsec, adjust 1A2A1A3R2 (fig. 19-1) to correct the width to 178 μsec.

16-12. IFF Display Video Adjustments

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON, and hold the CHALLENGE switch at TEST.

NOTE

Steps *c* through *f* may be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

c. Connect the oscilloscope to observe the positive-going IFF display video at DISPLAY VIDEO receptacle 1J2 on the rear of the interrogator group case. Use internal triggering (INT) and a sweep speed of 0.5 μsec per centimeter (undelayed), with a vertical sensitivity of 2 volts per centimeter. Note that the woveform consists of target present (narrow) and friend (wide) pulses superimposed on each other and baselined by the intervals when neither are present.

d. If the target present pulse width is not 1.0 μsec, adjust 1A2A1A5R1 (fig. 19-1) to correct the width to 1.0 μsec.

e. If the friend pulse amplitude is not 5.0 volts, adjust 1A2A1A5R2 (fig. 19-1) to correct the amplitude to 5.0 volts.

f. If the friend pulse width is not 5.0 μsec, adjust 1A2A1A5R3 (fig. 19-1) to correct the width to 5.0 μsec.

Section IV. DISPLAY VIDEO INTERFACE CIRCUIT TESTING

16-13. General

The display video interface circuits are most effectively tested by observing their outputs to other synchronizer circuits and to other parts of the IFF set in each possible mode of operation, using an oscilloscope. Most of the observations can be made in one sif mode, and mode 3/A was the sif mode chosen for the purposes of this manual. The remaining observations, made in the other modes, check only the functions which are not adequately checked in mode 3/A.

16-14. Test Equipment and Preparation

Like the troubleshooting procedure given in section II of this chapter, the display video interface circuit test observations are made with the synchronizer in operation as part of the complete hot mockup shown in figure 24-16. The test equipment required is therefore the same as listed in paragraph 12-4, and the preparation procedure is the same as given for overall synchronizer troubleshooting in paragraph 12-5, except that the input to receptacle 1J1 is terminated across a 75-ohm load.

16-15. Test Procedure

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON, check that the CHALLENGE switch is released (to OFF), and check that the SIF REPLIES switch is released (to CODED).

NOTE

Step *c* may be undertaken immediately. It is not necessary to wait until the receiver-

transmitter 60-second warmup delay has ended for this step.

c. At the synchronizer, observe the enable levels at the following three points in any desired order. The oscilloscope may be used to check these levels.

(1) 1A2A1A1-35: interface fault (should be low).

(2) 1A2A1A4-3: mode 4 enable (should be low).

(3) 1A2A1A4-12: $\overline{\text{mode 4/test target enable}}$ (should be high).

d. At the control box, after the receiver-transmitter warmup delay has ended, challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

e. At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1-3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

f. At the synchronizer, use the oscilloscope to observe the signals at the following five points in any desired order:

(1) 1A2A1A1-35: interface fault (should be low).

(2) 1A2A1A4-3: mode 4 enable (should be low).

(3) 1A2A1A4-12: $\overline{\text{mode 4/test target enable}}$ (should be high).

(4) 1A2A1A4-35: $\overline{\text{decoded reply video}}$ (K, fig. 20-3).

(5) 1A2A1A5-6: IFF display video (H, fig. 20-4).

g. At the control box, change the MODE 3/A CODE SELECT switch settings to a code other than 7777, but continue to challenge in mode 3/A.

h. At the synchronizer, use the oscilloscope to observe the signals at each of the following two points while the SIF REPLIES switch on the control box is alternately held at ALL and released (to CODED):

(1) 1A2A1A4-35: $\overline{\text{decoded reply video}}$ (K, fig. 20-3, in each position of the SIF REPLIES switch).

(2) 1A2A1A5-6: IFF display video (H, fig. 20-4, while the SIF REPLIES switch is held at ALL, but not present (continuously low) while the SIF REPLIES switch is at CODED).

i. At the control box, return the MODE 3/A CODE SELECT switches to 7777, and continue to challenge in mode 3/A.

j. At the processor, set the POWER circuit breaker to OFF. Loosen the eight captive screws that secure the processor to the interrogator group case, and pull the processor outward approximately an inch to disconnect its rear connectors.

k. At the synchronizer, use the oscilloscope to observe the IFF display video at 1A2A1A5-6 while the PROCESSOR switch on the control box is set alternately to IN and BYPASS. The IFF display video should appear as in H, figure 20-4, while the PROCESSOR switch is at BYPASS, but should not be present while the PROCESSOR switch is at IN. Slide the processor back into position and tighten the eight captive screws at the edges of its front panel.

l. At the processor, set the POWER circuit breaker to ON.

m. At the control box, set the PROCESSOR switch to IN, and then place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

n. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any desired order:

(1) 1A2A1A1-35: interface fault (should be low).

(2) 1A2A1A3J1-6: $\overline{\text{test target video}}$ (F, fig. 20-2).

(3) 1A2A1A4-3: mode 4 enable (should be low).

(4) 1A2A1A4-12: $\overline{\text{mode 4/test target enable}}$ (should be low).

(5) 1A2A1A5-6: IFF display video (J, fig. 20-4).

o. At the control box, challenge in mode 4 by holding the CHALLENGE switch at ON with the MODE SELECT switch at 4.

p. At the synchronizer, observe the enable levels at the following three points in any desired order. The oscilloscope may be used to check these levels.

(1) 1A2A1A1-35: interface fault (should be low).

(2) 1A2A1A4-3: mode 4 enable (should be high).

(3) 1A2A1A4-12: mode 4/test target enable (should be low).

CHAPTER 17

FAULT INDICATION CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. FAULT INDICATION CIRCUIT TROUBLESHOOTING INFORMATION

17-1. General

a. This chapter presents a troubleshooting procedure and a test procedure for the fault indication circuits. These circuits consist of the four FAULT lamps on the synchronizer front panel and some of the parts on one printed wiring card in interface module 1A2A1. The troubleshooting procedure is based on the assumptions listed in paragraph 12-2 and the further assumption that the trouble is definitely known to lie in the fault indication circuits. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12.

b. This section indexes the fault indication circuit data located in other parts of this manual, and provides a list of the normal fault indication circuit test indications. Section II provides the fault indication circuit troubleshooting procedure, and section III provides the fault indication circuit test procedure.

c. The fault indication circuits contain no controls or adjustments.

17-2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the fault indication circuits:

Reference	*Data*
Chapter 8	Fault indication circuit functioning.
Fig. 24-14	Fault indication circuit logic diagram.
Fig. 24-17	Synchronizer 1A2 schematic diagram.
Fig. 24-18	Interface module 1A2A1 schematic diagram.
Fig. 24-26	Buffer circuit 1 card 1A2A1A8 schematic diagram.

17-3. Normal Test Indications

The following chart lists the fault indications and signals which are of significance in troubleshooting the fault indication circuits:

Point of observation	*Normal indication*
RADAR TRIG FAULT lamp 1A2DS1.	Visually indicates level of radar trigger fault input at 1A2A1A8-16; lights when that level is high (fault), but does not light when that level is low (no-fault).
TIMING FAULT lamp 1A2DS2	Visually indicates level of timing fault input at 1A2A1A8-18, unless inhibited by high radar trigger fault input at 1A2A1A8-16; lights when timing fault input is high (fault) and radar trigger fault input is simultaneously low (no-fault), but does not light if timing fault input is low (no-fault) or if radar trigger fault input is high (fault).
CODER DECODER FAULT lamp 1A2DS3.	Visually indicates level of coder-decoder fault input at 1A2A1A8-20, unless inhibited by high radar trigger fault input at 1A2A1A8-16; lights when coder-decoder fault input is high (fault) and radar trigger fault input is simultaneously low (no-fault), but does not light if coder-decoder fault input is low (no-fault) or if radar trigger fault input is high (fault).
INTERFACE FAULT lamp 1A2DS4	Visually indicates level of interface fault input at 1A2A1A8-14, unless inhibited by high radar trigger fault input at 1A2A1A8-16; lights when interface fault input is high (fault) and radar trigger fault input is simultaneously low (no-fault), but does not light if interface fault input is low (no-fault) or if radar trigger fault input is high (fault).

Point of observation	*Normal indication*
1A2A1A8-11	Synchronizer fault indicator enable: ground (fault) or open circuit (no-fault) output to control box; open circuit as long as all four fault inputs listed below are low (no-fault) and have been low for at least 0.8 seconds; grounded when, and for as long as, any of the four fault inputs is high, or for 0.8 second, whichever is longer.
1A2A1A8-14	Interface fault input: high (fault) or low (no-fault) level from interface module 1A2A1.
1A2A1A8-16	Radar trigger fault input: high (fault) or low (no-fault) level from timing module 1A2A4.
1A2A1A8-18	Timing fault input: high (fault) or low (no-fault) level from timing module 1A2A4.
1A2A1A8-20	Coder-decoder fault input: high (fault) or low (no-fault) level from coder-decoder module 1A2A2.
1A2A1A8-22	Radar trigger fault lamp return: low to light (or high to extinguish) RADAR TRIG FAULT lamp 1A2DS1.
1A2A1A8-23	Coder-decoder fault lamp return; low to light (or high to extinguish) CODER DECODER FAULT lamp 1A2DS3.
1A2A1A8-28	Interface fault lamp return: low to light (or high to extinguish) INTERFACE FAULT lamp 1A2DS4.
1A2A1A8-29	Timing fault lamp return; low to light (or high to extinguish) TIMING FAULT lamp 1A2DS2.

Section II. FAULT INDICATION CIRCUIT TROUBLESHOOTING PROCEDURE

17–4. General

The fault indication circuits operate continuously, lighting the FAULT lamps in response to the four fault inputs, for as long as the synchronizer is turned ON. For troubleshooting or testing of the fault indication circuits, therefore, the only synchronizer inputs required from the hot mockup are 28-volt dc power and simulated radar triggers.

17–5. Test Equipment Required

a. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facility set are not required. The items required are the following:

(1) Multimeter.

(2) Radar test set (only to supply "0" TRIGGER output to 1J1).

(3) 28-volt dc power supply.

(4) Test facilities set (only for cables W32, W41, W42, and W47).

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

17–6. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c* below.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply.

17–7. Troubleshooting Procedure

a. With the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 17–6*b*, remove buffer circuit 1 card 1A2A1A8 from interface module 1A2A1, and install an extender card in its place. Do not insert the buffer circuit 1 card into the extender card until so directed in step *f* below.

b. Set the POWER circuit breakers on the synchronizer and interrogator group case to ON.

c. At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

The troubleshooting steps below may be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

d. Observe the four FAULT lamps on the synchronizer front panel. All four should be extinguished. If any are lighted, the corresponding lampholders are defective.

e. Momentarily press-to-test each of the four FAULT lamps. If any of the FAULT lamps fail to light when depressed, the corresponding lamp bulbs or lampholders are defective.

f. Set the synchronizer POWER circuit breaker to OFF, insert buffer circuit 1 card 1A2A1A8 into the extender card. The SYN SELF TEST lamp on the control box should light. If it does not light buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

g. Set the synchronizer POWER circuit breaker to ON and observe the SYN SELF TEST lamp on the control box and the four synchronizer FAULT lamps, disregarding the momentary indications, if any, immediately after setting the POWER circuit breaker to ON.

(1) If the SYN SELF TEST is extinguished, but one or more of the four FAULT lamps are lighted, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

(2) If the SYN SELF TEST lamp and the four FAULT lamps are all not lighted, disregard the remainder of this step and proceed with step *h*.

(3) If the SYN SELF TEST lamp is lighted, but all four of the FAULT lamps are not lighted, check the four fault levels at 1A2A1A8–14, –16, –18, and –20, using the multimeter.

(*a*) If all four fault levels are low, the synchronizer fault relay drive circuit on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

(*b*) If the radar trigger fault level at 1A2A1A8–16 is high, disregard steps *h* through *o* and proceed with step *p*.

(*c*) If the timing fault level at 1A2A1A8–18 is high, disregard steps *h* through *p* and proceed with step *q*.

(*d*) If the coder-decoder fault level at 1A2A1A8–20 is high, disregard steps *h* through *q* and proceed with step *r*.

(*e*) If the interface fault level at 1A2A1A8–14 is high, disregard steps *h* through *r* and proceed with step *s*.

h. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control fully counterclockwise to force a high (fault) radar trigger fault level. The SYN SELF TEST lamp on the control box and the RADAR TRIG FAULT lamp on the synchronizer should both be lighted.

(1) If the SYN SELF TEST lamp is not lighted, buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

(2) If the SYN SELF TEST lamp is lighted but the RADAR TRIG FAULT lamp is not lighted, disregard steps *i* through *o* and proceed with step *p*, leaving the PRF control on the XTAL MARK & SYNC panel fully counterclockwise.

i. Set the synchronizer POWER circuit breaker to OFF, remove the 10-mc clock and counter A card 1A2A4A1 from timing module 1A2A4, and then set the POWER circuit breaker to ON. This forces a

high (fault) timing fault level, but the TIMING FAULT lamp should not light because the radar trigger fault level is also high. If the TIMING FAULT lamp lights, the timing lamp drive circuit on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

j. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control clockwise until the RADAR TRIG FAULT lamp on the synchronizer goes out. The TIMING FAULT lamp should then light; if not, disregard steps *k* through *p* and proceed with step *q*, leaving the 10-mc clock and counter A card out of the timing module.

k. Set the synchronizer POWER circuit breaker to OFF, and reinstall the 10-mc clock and counter A card in the timing module. Then remove either correct code 1 card 1A2A2A2 or correct code 2 card 1A2A2A3 from coder-decoder module 1A2A2, and set the POWER circuit breaker to ON. This forces a high (fault) coder-decoder fault level, and the CODER DECODER FAULT lamp should light because the radar trigger fault level is low (no-fault). If the CODER DECODER FAULT lamp does not light, disregard steps *l* through *q* and proceed with step *r*, leaving the correct code 1 or correct code 2 card out of the coder-decoder module.

l. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control fully counterclockwise to force a high (fault) radar trigger fault level. The CODER DECODER FAULT lamp should go out; if not, the coder-decoder lamp drive circuit on buffer circuit 1 card 1A1A2A8 is defective; refer to chapter 20, section IX.

m. Set the synchronizer POWER circuit breaker to OFF, and reinstall the correct code 1 card or correct code 2 card in the coder-decoder module. Then remove interface self-test card 1A2A1A1 from interface module 1A2A1, and set the POWER circuit breaker to ON. This will force a high (fault) interface fault level during the next step.

n. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST, and observe the synchronizer INTERFACE FAULT lamp. With interface self-test card 1A2A1A1 removed, the interface fault level is forced high (fault), but the INTERFACE FAULT lamp should not light because the radar trigger fault level is also high. If the INTERFACE FAULT lamp lights, the interface lamp drive circuit on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX.

o. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control clockwise until the RADAR TRIG FAULT lamp on the synchronizer goes out. If the INTERFACE FAULT lamp then lights, the synchronizer fault relay drive circuit on buffer circuit 1 card 1A2A1A8 is defective; refer to chapter 20, section IX. If the INTERFACE FAULT lamp does not light, disregard steps *p* through *r* and proceed with step *s*, leaving the IFF set in the test target mode and interface self-test card 1A2A1A1 out of the interface module.

p. If the RADAR TRIG FAULT lamp does not light when the radar trigger fault level at 1A2A1A8–16 is high, measure the radar trigger fault lamp return level at 1A2A1A8–22, using the multimeter. If lower than +1.0 volt, lampholder 1A2XDS1 is defective. If higher than +1.0 volt, the radar trigger lamp drive circuit on the buffer circuit 1 card is defective; refer to chapter 20, section IX.

q. If the TIMING FAULT lamp does not light when the timing fault level at 1A2A1A8–18 is high and the radar trigger fault level at 1A2A1A8–16 is low, measure the timing fault lamp return level at 1A2A1A8–29, using the multimeter. If lower than +1.0 volt, lampholder 1A2XDS2 is defective. If higher than +1.0 volt, the timing lamp drive circuit on the buffer circuit 1 card is defective; refer to chapter 20, section IX.

r. If the CODER DECODER FAULT lamp does not light when the coder-decoder fault level at 1A2A1A8–20 is high and the radar trigger fault level at 1A2A1A8–16 is low, measure the coder-decoder fault lamp return level at 1A2A1A8–23, using the multimeter. If lower than +1.0 volt, lampholder 1A2XDS3 is defective. If higher than +1.0 volt, the coder-decoder lamp drive circuit on the buffer circuit 1 card is defective; refer to chapter 20, section IX.

s. If the INTERFACE FAULT lamp does not light when the interface fault level at 1A2A1A8–14 is high and the radar trigger fault level at 1A2A1A8–16 is low, measure the interface fault lamp return level at 1A2A1A8–28, using the multimeter. If lower than +1.0 volt, lampholder 1A2XDS4 is defective. If higher than +1.0 volt, the interface lamp drive circuit on the buffer circuit 1 card is defective; refer to chapter 20, section IX.

Section III. FAULT INDICATION CIRCUIT TESTING

17–8. Test Equipment and Preparation

The test procedure for the fault indication circuits is identical, except for the lack of trouble localization steps, to the troubleshooting procedure given in section II of this chapter. Therefore, the test equipment required is the same as that referenced in paragraph 17–5, and the preparation for testing is the same as the preparation for troubleshooting given in paragraph 17–6.

17–9. Test Procedure

a. With the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 17–6*b*, set the synchronizer POWER circuit breaker to ON.

b. At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

The testing steps below may be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup has ended.

c. Observe the SYN SELF TEST lamp on the control box and the four synchronizer FAULT lamps, disregarding the momentary indications, if any, immediately after applying power. All five lamps should be extinguished.

d. At the synchronizer, momentarily press-to-test each of the four FAULT lamps. Each should light for as long as it is depressed.

e. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control fully counterclockwise to simulate an unacceptably low radar trigger prf. The SYN SELF TEST lamp on the control box and the RADAR TRIG FAULT lamp on the synchronizer should both light.

f. Set the synchronizer POWER switch to OFF, remove 10-mc clock and counter A card 1A2A4A1 from timing module 1A2A4, and then set the POWER circuit breaker to ON. The TIMING FAULT lamp should not light.

g. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control clockwise until the RADAR TRIG FAULT lamp on the synchronizer goes out. The TIMING FAULT lamp should then light.

h. At the synchronizer set the POWER circuit breaker to OFF, and reinstall the 10-mc clock and counter A card in the timing module. Then remove either correct code 1 card 1A2A2A2 or correct code 2 card 1A2A2A3 from coder-decoder module 1A2A2, and set the POWER circuit breaker to ON. The CODER DECODER FAULT lamp should light.

i. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control fully counterclockwise to simulate an unacceptably low radar trigger prf. The CODER DECODER FAULT lamp on the synchronizer should then go out.

j. At the synchronizer, set the POWER circuit breaker to OFF, and reinstall the correct code 1 card or correct code 2 card in the coder-decoder module. Then remove interface self-test card 1A2A1A1 from interface module 1A2A1, and set the POWER circuit breaker to ON. The INTERFACE FAULT lamp should not light.

k. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST. The INTERFACE FAULT lamp on the synchronizer should not light.

l. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control clockwise until the RADAR TRIG FAULT lamp on the synchronizer goes out. The INTERFACE FAULT lamp should light.

CHAPTER 18

POWER SUPPLY AND POWER DISTRIBUTION CIRCUIT TROUBLESHOOTING AND REPAIR

Section I. POWER SUPPLY AND POWER DISTRIBUTION CIRCUIT TROUBLESHOOTING INFORMATION

18–1. General

a. This chapter presents troubleshooting, adjustment, and test procedures for the power supply and power distribution circuits. The power supply circuits consist of power supply module 1A2A3 and the front panel metering circuit composed of meter 1A2M1, voltage selector 1A2S1 (OUT, +5, +12, −12), and the parts on component board 1A2A7. The power distribution circuit is composed of sealed filter 1A2A6, POWER circuit breaker 1A2CB1, POWER lamp 1A2DS5, and filter capacitors 1A2C1 and 1A2A3C1. The troubleshooting procedure is based on the assumptions listed in paragraph 12–2 and the further assumption that the trouble is definitely known to lie in the power supply and power distribution circuits. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12.

b. This section indexes the power supply and power distribution circuit data located in other parts of this manual, and provides a list of the normal power supply and power distribution circuit test indications. Section II provides the power supply and power distribution circuit troubleshooting procedure, section III provides the power supply and power distribution circuit adjustment procedures, and section IV provides the power supply and power distribution circuit test procedure.

18–2. Reference Data

The data listed in the following chart will be helpful when troubleshooting the power supply and power distribution circuits:

Reference	*Data*
Chapter 9	Power supply and power distribution circuit functioning.
Fig. 20–15	+12-volt regulator card 1A2A2A1 waveforms.
Fig. 20–16	+5-volt regulator card 1A2A3A2 waveforms.
Fig. 20–17	−12-volt inverter card 1A2A3A3 waveforms.
Fig. 24–17	Synchronizer 1A2 schematic diagram.
Fig. 24–35	Power supply module 1A2A3 schematic diagram.
Fig. 24–36	+12-volt regulator card 1A2A3A1 schematic diagram.
Fig. 24–37	+5-volt regulator card 1A2A3A2 schematic diagram.
Fig. 24–38	−12-volt inverter card 1A2A3A3 schematic diagram.

18–3. Controls and Adjustments

a. Controls. The power supply and power distribution circuits contain two front panel controls: POWER circuit breaker 1A2CB1, and voltage selector 1A2S1 (OUT, +5, +12, −12).

(1) The POWER circuit breaker provides overcurrent protection and is used as a local synnchronizer ON–OFF switch to turn off the synchronizer independently of the other parts of the IFF set.

(2) The voltage selector is used in conjunction with 1A2M1 for checking the three power supply voltages on a go/no–go basis. At OUT, the voltage selector disconnects and short circuits 1A2M1 and potentiometer 1A2A7R3. At +5, +12, and −12, it connects 1A2M1 for go/no–go readings of the corresponding power supply voltages.

b. Adjustments. The power supply circuits contain three potentiometers: +12-volt adjustment

potentiometer 1A2A3A1R27, +5-volt adjustment potentiometer 1A2A3A2R23, and meter calibration potentiometer 1A2A7R3. The adjustment procedures for these potentiometers are given in paragraphs 18–11, 18–12, and 18–13, respectively.

(1) The total load on the +5-volt power supply voltage is also a load on the +12-volt power supply voltage, because the +5-volt regulator circuit receives the +12-volt power supply voltage as its input. Therefore, if either of the two voltages is in error by more than approximately ±0.5 volt when adjustment is started, then it may be necessary to adjust both voltages and the corresponding adjustment procedures take this possibility into account by specifying that both voltages be measured.

(2) The +12-volt adjustment potentiometer is adjusted for an output of +12 volts from +12-volt regulator card 1A2A3A1. Then the output of +5-volt regulator card 1A2A3A2 is measured to determine whether a +5-volt adjustment is also required. The output of the −12-volt inverter card is also measured, because it is affected by the +12-volt adjustment, but the measurement is merely to verify that the −12-volt power supply voltage is within its relatively broad tolerance (−12 ±1 volt).

(3) The +5-volt adjustment potentiometer is adjusted for an output of +5 volts from +5-volt regulator card 1A2A3A2. Then the output of the +12-volt regulator card is measured to determine whether it has been affected enough to require another +12-volt adjustment.

(4) The meter calibration adjustment potentiometer is adjusted so that the readings on 1A2M1 are as near as possible, on average, to the center of the solid green band when the voltage selector is switched to +5, +12, and −12 in any order.

18–4. Normal Test Indications

The following chart lists the normal indications and signals which are of significance in troubleshooting the power supply and power distribution circuits:

Point of observation	*Normal indication*
POWER lamp 1A2DS5	(1) Not lighted when POWER circuit breaker 1A2CB1 is at OFF.
	(2) Lights when depressed with POWER circuit breaker at OFF and with +28 volts available.
	(3) Lights when POWER circuit breaker is at ON with +28 volts available.
POWER circuit breaker 1A2CB1	Does not trip to OFF when set to ON with +28 volts available.
Green-Band Voltmeter 1A2M1	Gives readings within green (go) band when voltage selector 1A2S1 is set to +5, +12, and −12 and the corresponding voltages are within tolerance.
1A2A6–1	+28 volts (dc input from interrogator group case; actual voltage depends on external +28-volt dc power supply).
1A2A6–2	+28 volt return.
1A2A6–3	+28 volts (filtered).
1A2A6–4	+28 volt (filtered).
1A2E2	+28 volts when POWER circuit breaker 1A2CB1 is at ON; zero volts when 1A2CB1 is at OFF.
1A2A3A1E10	+12 volts (power supply voltage; normal value is +12 ± 0.25 volts, with ripple not exceeding ± 0.25 volt peak-to-peak).
1A2A3A1E11	+28 volts when POWER circuit breaker 1A2CB1 is at ON.
1A2A3A2E6	+5 volts (power supply voltage; normal value is +5 volts, with ripple not exceeding ± 0.50 volt peak-to-peak).

Point of observation	*Normal indication*
1A2A3A2E8	+28 volts (same as at 1A2A3A1E10).
1A2A3A3J1	10-kc triggers (A, fig. 20–17).
1A2A3A3J2	Current limited +12 volts (nominally equal to the +12 volts at 1A2A3A1E10 or 1A2A3A2E8).
1A2A3A3J3	−12 volts (power supply voltage; normal value −12 ± 1 volts, with ripple not exceeding ± 0.15 volt, peak-to-peak).
1A2A3A3J4	Crowbar trigger generator emitter voltage (normally +0.5 to +2.0 volts when measured with an oscilloscope).

Section II. POWER SUPPLY AND POWER DISTRIBUTION CIRCUIT TROUBLESHOOTING CHART

18–5. General

The only synchronizer input required from the hot mockup for troubleshooting or testing the power supply and power distribution circuits is +28-volt dc power.

18–6. Test Equipment Required

a. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the radar test set, the mode 4 word generator, and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Oscilloscope.

(2) Multimeter.

(3) 28-volt dc power supply.

(4) Test Facilities set (only for cables W32, W41, and W42).

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

18–7. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer and the 28-volt dc power supply to the interrogator group case as shown in figure 24–16. It is not necessary to connect the oscilloscope to receive an external SYNC IN signal, because all power supply and power distribution circuit waveforms are taken with the oscilloscope sweep internally synchronized.

c. At the control box, set the POWER circuit breaker to OFF. (The other control box switch settings are immaterial.)

d. Set the controls on the oscilloscope as directed in paragraph 12–5*f*.

e. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

f. Turn ON the 28-volt dc power supply.

18–8. Troubleshooting Chart

a. Preliminary Procedure. With the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 18–7*b*, set the POWER circuit breaker on the control box to ON and observe the visual indications or signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the corrective measures column. Note that the synchronizer POWER circuit breaker is to be left at OFF for step 1, and is then to be set to ON for all remaining steps.

NOTE

The troubleshooting steps can be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

b. Power Supply and Power Distribution Circuit Troubleshooting Chart.

Step	Test point	Test equipment	Normal indication	Corrective measures
1	POWER lamp 1A2DS5.	None	Lights when depressed with POWER circuit breaker 1A2CB1 at OFF and +28 volts available.	If abnormal, proceed with step 2. If normal, proceed with step 3.
2	1A2A6-3	Multimeter	+28 volts	If normal, lampholder 1A2XDS5 is defective. If abnormal, 1A2A6 is defective.
3	POWER circuit breaker 1A2CB1.	None	Remains at ON when set to ON.	If 1A2CB1 remains at ON, leave it at ON and proceed with step 9. If 1A2CB1 trips to OFF, remove interface, coder-decoder, power supply, and timing modules 1A2A1, 1A2A2, 1A2A3, and 1A2A4. Then proceed with step 4.
4	1A2CB1	None	Remains at ON when set to ON with 1A2A3 removed.	If 1A2CB1 trips to OFF, 1A2C1 is defective. If 1A2CB1 remains at ON, set it to OFF, reinstall power supply module 1A2A3, and proceed with step 5, leaving 1A2A1, 1A2A2, and 1A2A4 removed.
5	1A2CB1	None	Remains at ON when set to ON with 1A2A3 installed but 1A2A1 removed.	If 1A2CB1 remains at ON, a short circuit exists in the metering circuit composed of 1A2S1, 1A2M1, and component board 1A2A7. If 1A2CB1 trips to OFF, remove +5-volt regulator card 1A2A3A2, and proceed with step 6.
6	1A2CB1	None	Remains at ON when set to ON with 1A2A3A2 removed.	If 1A2CB1 remains at ON, 1A2A3A2 is defective; refer to chapter 20, section XVIII. If 1A2CB1 trips to OFF, remove —12-volt inverter card 1A2A3A3, and proceed with step 7.
7	1A2CB1	None	Remains at ON when set to ON with 1A2A3A3 removed.	If 1A2CB1 remains at ON, 1A2A3A3 is defective; refer to chapter 20, section XIX. If 1A2CB1 trips to OFF, remove +12-volt regulator card 1A2A3A1, and proceed with step 8.
8	1A2CB1	None	Remains at ON when set to ON with 1A2A3A1 removed.	If 1A2CB1 remains at ON, 1A2A3A1 is defective; refer to chapter 20, section XVII. If 1A2CB1 trips to OFF, 1A2A3C1 is defective.

Step	Test point	Test equipment	Normal indication	Corrective measures
9	POWER lamp 1A2DS5.	None	Lighted as long as 1A2CB1 is at ON.	If 1A2DS5 does not light, or lights dimly, measure voltage at 1A2E2, using multimeter. If 1A2E2 is at +28 volts, lampholder 1A2XDS5 is defective. If 1A2E2 is at less than +28 volts, 1A2CB1 is defective.
10	1A2A3A1E10	Multimeter	+12 ±0.25 volts	If normal, proceed with step 15. If abnormal, adjust 1A2A3A1R27 as directed in paragraph 18–11. If adjustment fails, proceed with step 11 if voltage is too low, or with step 13 if voltage is too high.
11	1A2A3A1E11	Multimeter	+28 volts	If normal, proceed with step 14. If abnormal, proceed with step 12.
12	1A2A6–3	Multimeter	+28 volts	If normal, a wiring defect exists. If abnormal, filter 1A2A6 is defective.
13	1A2A3A3J2	Multimeter	+12 volts (nominal)	If normal, +12-volt regulator card 1A2A3A1 is defective; refer to Chapter 20, section XVII. If abnormal, proceed with step 14.
14	1A2A3A3J1	Oscilloscope	10-kc triggers (A, fig. 20–17).	If normal, +12-volt regulator card 1A2A3A1 is defective; refer to chapter 20, section XVII. If abnormal, —12-volt inverter card 1A2A3A3 is defective; refer to chapter 20, section XIX.
15	1A2A3A1E10	Oscilloscope	Ripple on +12-volt output does not exceed 0.25 volt peak-to-peak (A, fig. 20–15).	If ripple exceeds 0.25 volt peak-to-peak, +12-volt regulator card 1A2A3A1 is defective; refer to chapter 20, section XVII.
16	1A2A3A3J3	Multimeter	—12 ±0.35 volts	If abnormal, proceed with step 17. If normal, proceed with step 19.
17	1A2A3A3J2	Multimeter	+12 volts (nominal)	If normal, —12-volt inverter card 1A2A3A3 is defective, refer to chapter 20, section XIX. If abnormal, continue with step 18.
18	1A2A3A3J4	Oscilloscope	+0.5 to +2.0 volts	If normal, +12-volt regulator card 1A2A3A1 is defective; refer to chapter 20, section XVII. If abnormal, —12-volt inverter card 1A2A3A3 is defective; refer to chapter 20, section XIX.

Step	Test point	Test equipment	Normal indication	Corrective measures
19	1A2A3A3J3	Oscilloscope	Ripple on −12 volt output does not exceed 0.2 volt peak-to-peak (B, fig. 20–17).	If ripple exceeds 0.2 volt peak-to-peak, −12-volt inverter card 1A2A3A3 is defective; refer to chapter 20, section XIX.
20	1A2A3A2E6	Multimeter	+5 volts	If abnormal, +5-volt regulator card 1A2A3A2 is defective; refer to chapter 20, section XVIII. If abnormal, proceed with step 21.
21	1A2A3A2E6	Oscilloscope	Ripple on +5-volt output does not exceed 0.2 volt peak-to-peak (A, fig. 20–16).	If ripple exceeds 0.2 volt peak-to-peak, +5-volt regulator card 1A2A3A2 is defective; refer to chapter 20, section XVIII.
22	Meter 1A2M1 (front panel).	None	Meter reading is within the green crosshatched area when voltage selector 1A2S1 (front panel) is set to +12.	If reading is within the green crosshatched area, proceed with step 28. If reading is zero or otherwise entirely outside green area, proceed with step 24.
23	Meter 1A2M1	None	Meter reading is within the green crosshatched area when 1A2S1 is set to −12.	If reading is zero or otherwise entirely outside the green crosshatched green band, voltage selector 1A2S1 is defective. If reading is within the area green band, proceed with step 24.
24	Meter 1A2M1	None	Meter reading is centered within solid green band when 1A2S1 is set to +5.	If reading is zero or otherwise entirely outside solid green band, perform step 27. If reading is within green band, adjust 1A2A7R3 as directed in paragraph 18–13. If adjustment fails, check 1A2A7R2, 1A2A7R3, and 1A2M1. Replace the defective part.
25	Meter 1A2M1	None	Meter reading is within the green crosshatched area when 1A2S1 is set to −12.	If reading is normal, or nearly normal (well within green crosshatched area), voltage selector 1A2S1 is defective.
26	Meter 1A2M1	None	Meter reading is centered within solid green band when 1A2S1 is set to +5.	If reading is normal or nearly normal (well within solid green band), resistor 1A2A7R4 is defective.
27	1A2A7–5, 1A2A7–2	Multimeter (measure voltage between test points. If necessary, remove 1A2A5 for access).	Voltage across 1A2A7R2 is 0.25 volt when 1A2S1 is set to +5.	If normal, check 1A2A7R3 and 1A2M1. If abnormal, check 1A2A7R2. Replace the defective part.

Step	Test point	Test equipment	Normal indication	Corrective measures
28	Meter 1A2M1 ------	None ----------	Meter reading is within green crosshatched area when 1A2S1 is set to −12.	If reading is zero or otherwise entirely outside green area, 1A2S1 is defective. If reading is normal or nearly normal (well within the crosshatched green area), check 1A2A7R1 and 1A2S1. Replace the defective part.

Section III. ADJUSTMENT OF POWER SUPPLY CIRCUITS

18–9. General

The power supply circuit adjustments are the +12 and +5 volt adjustments made by means of the corresponding potentiometers in power supply module 1A2A3 (fig. 19–5) and the meter calibration adjustment made by means of potentiometer 1A2A7R3 (fig. 12–1) behind the synchronizer front panel. These adjustments are made with the synchronizer turned ON and with a +28-volt dc input.

18–10. Test Equipment and Preparation

Like the troubleshooting procedure given in section II of this chapter, the adjustment procedures are based on operation of the synchronizer as part of a hot mockup: either the complete hot mockup shown in figure 24–16, or enough of that hot mockup to provide the synchronizer with a 28-volt dc power input. The test equipment required is therefore the same as described in paragraph 18–6, and the preparation procedure is the same as given in paragraph 18–7.

18–11. +12-Volt Adjustment

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

c. At the control box, set the POWER circuit breaker to ON.

NOTE

The adjustment steps below can be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

d. Measure the +12-volt power supply voltage at 1A2A3A1E10, using the multimeter. If the voltage at 1A2A3A1E10 is not +12 volts, adjust 1A2A3A1R27 (fig. 19–5) to correct the voltage to +12 volts.

e. Measure the +5-volt power supply voltage at 1A2A3A2E6, using the multimeter. If the voltage at 1A2A3A2E6 is not +5 volts, adjust 1A2A3A3R23 (fig. 19–5) to correct the voltage to +5 volts.

f. Repeat steps *d* and *e* above, until both voltages are accurately adjusted.

18–12. +5-Volt Adjustment

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

c. At the control box, set the POWER circuit breaker to ON.

NOTE

The adjustment steps below can be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

d. Measure the +5-volt power supply voltage at 1A2A3A2E6, using the multimeter. If the voltage at 1A2A3A2E6 is not +5 volts, adjust 1A2A3A2R23 (fig. 19–5) to correct the voltage to +5 volts.

e. Measure the +12-volt power supply voltage at 1A2A3A1E10, using the multimeter. If the voltage at 1A2A3A1E10 is not +12 volts, adjust

1A2A3A1R27 (fig. 19-5) to correct the voltage to +12 volts.

f. Repeat steps *d* and *e* above, until both voltages are accurately adjusted.

18-13. Meter Calibration Adjustment

a. After all preparations have been made, set the synchronizer POWER circuit breaker to ON.

b. On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

c. At the control box, set the POWER circuit breaker to ON.

NOTE

The adjustment steps below can be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

d. At the front panel of the synchronizer, note the readings of voltmeter 1A2M1 when voltage selector 1A2S1 is switched to its +5 position and then to its +12 position. If the average of the two readings is not at the center of the solid green band, adjust 1A2A7R3 (fig. 12-1) to correct the average reading to the center of the solid green band.

Section IV. POWER SUPPLY AND POWER DISTRIBUTION CIRCUIT TESTING

18-14. Test Equipment and Preparation

The power supply and power distribution circuits are tested under the same conditions as for troubleshooting or adjustment. The test equipment required is therefore the same as described in paragraph 18-16, and the preparation procedure is the same as given in paragraph 18-7.

18-15. Testing Procedure

a. After all preparations have been made, set the POWER circuit breakers on the interrogator group case (power control panel) and the control box to ON.

NOTE

The test steps below can be undertaken immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

b. At the synchronizer front panel, with the synchronizer POWER circuit breaker at OFF, POWER lamp 1A2DS5 should not be lighted.

c. Momentarily depress POWER lamp 1A2DS5. The POWER lamp should light for as long as it is held depressed.

d. Set POWER circuit breaker 1A2CB1 to ON. The POWER lamp should light, and the POWER circuit breaker should remain ON (not trip to OFF).

e. Measure the voltage 1A2A3A1E10, using the multimeter. The voltage should be +12 ± 0.25 volts.

f. Observe the +12-volt ripple waveform at 1A2A3A1E10 (A, fig. 20-15), using the oscilloscope. The +12-volt ripple should not exceed 0.25 volt peak-to-peak.

g. Measure the voltage at 1A2A3A2E6, using the multimeter. The voltage should be +5 ± 0.1 volts.

h. Observe the +5-volt ripple waveform at 1A2A3A2E6 (A, fig. 20-16), using the osciloscope. The +5-volt ripple should not exceed 0.2 volt peak-to-peak.

i. Measure the voltage at 1A2A3A3J3, using the multimeter. The voltage should be −12 ± 1.0 volts.

j. Observe the −12-volt ripple waveform at 1A2A3A3J3 (B, fig. 20-17), using the oscilloscope. The −12-volt ripple should not exceed 0.2 volt peak-to-peak.

k. Set voltage selector 1A2S1 successively to +5, +12, and −12, allowing the indication on voltmeter 1A2M1 to settle at each position. The meter indication at each position should be well within the solid green band.

CHAPTER 19

SYNCHRONIZER MODULE TROUBLESHOOTING AND REPAIR

Section I. SYNCHRONIZER MODULE TROUBLESHOOTING INFORMATION

19–1. General

This chapter outlines the troubleshooting and repair sequence to be followed when a defective synchronizer module is returned from the using activity, and provides module connector resistance measurements and part location photographs for each of the five synchronizer modules.

19–2. Module Troubleshooting and Repair Sequence

a. The complete sequence of troubleshooting and repair activities listed in *b*, below, applies to interface module 1A2A1 and coder-decoder module 1A2A2, each of which contains parts of more than one major functional circuit group. For power supply module 1A2A3 and timing module 1A2A4, the sequence is the same except that the sectionalization step (overall synchronizer troubleshooting) is not necessary: if the power supply module is known to be defective, the trouble is already sectionalized to the power supply and power distribution; or if the timing module is known to be defective, the trouble is already sectionalized to the timing circuits. In the sequence for delay line module 1A2A5, given in *c* below, the first step (short circuit check) is the same as for the other modules. However, the only additional troubleshooting step applicable to the delay line module is a continuity check (isolation), because the delay line module contains only two electrical parts other than wires: sealed (nonrepairable) delay line 1A2A5DL1, and module connector 1A2A5P1.

b. When a defective synchronizer module other than delay line module 1A2A5 is returned from the using activity, the following is the required sequence of troubleshooting and repair activities:

(1) Check the defective module for short circuits by comparing resistance measurements at its module connector pins with the values given in the corresponding paragraph of this chapter: paragraph 19–4 for interface module 1A2A1; paragraph 19–7 for coder-decoder module 1A2A2; paragraph 19–10 for power supply module 1A2A3; or paragraph 19–13 for timing module 1A2A4.

(2) Install the defective module in an otherwise satisfactory synchronizer for hot mockup troubleshooting.

(3) If the defective module is interface module 1A2A1 or coder-decoder module 1A2A2, perform overall synchronizer troubleshooting as directed in chapter 12. This will sectionalize the trouble to a major functional circuit group and may, in some cases, localize the trouble to a printed wiring card. If the defective module is power supply module 1A2A3 or timing module 1A2A4, the trouble may be considered to be sectionalized either to the power supply and power distribution circuits or to the timing circuits, respectively.

(4) When the trouble has been sectionalized to one of the major functional circuit groups, perform circuit troubleshooting as directed in the corresponding circuit troubleshooting and repair chapter. This will localize the trouble to a printed wiring card and may, in some cases, isolate the trouble to a stage or integrated circuit.

(5) When the trouble has been localized to one of the printed wiring cards, perform card troubleshooting as directed in the corresponding section of chapter 20. This will isolate the trouble to a stage or integrated circuit.

(6) If the trouble has been isolated to a stage containing discrete parts, test the parts to determine which part is defective. If isolated to an integrated circuit, the integrated circuit is the defective part.

(7) Replace the defective part in accordance with the information and instructions referenced in paragraph 11–3*l*. This repairs the card.

(8) After the card has been repaired, check it for short circuits which might have been introduced during the repair by comparing resistance measurements at its pins with the values given in the corresponding section of chapter 20.

(9) Test the repaired card by installing it in an otherwise satisfactory (hot mockup) synchronizer and performing the card test in the corresponding section of chapter 20.

c. When delay line module 1A2A5 is returned from the using activity, the following is the required sequence of troubleshooting and repair activities:

(1) Check the defective delay line module for short circuits by comparing resistance measurements at its module connector with the values given in paragraph 19–16. If any short circuits are found, trace them either to the wiring between 1A2A5P1 and 1A2A5DL1 or to 1A2A5DL1 itself. Then replace the short circuited wires or the line, and test the repaired delay line module by proceeding with steps (3) through (6) below.

(2) If no short circuits are found, check the wiring continuity between 1A2A5P1 and 1A2A5DL1 to verify that the wiring agrees with the delay line module schematic included in the overall synchronizer schematic diagram (fig. 24–17). Replace any wires not showing continuity, or replace 1A2A5DL1 if all wires show continuity. Then test the repaired delay line module by proceeding with steps (3) through (6) below.

(3) Install the repaired delay line module in an otherwise satisfactory (hot mockup) synchronizer and prepare for overall synchronizer troubleshooting as directed in paragraphs 12–4 and 12–5.

(4) Turn on the hot mockup, including the synchronizer, as directed in paragraph 12–6*a*, but do not continue with the overall synchronizer troubleshooting chart based on single fault lamp indication. Instead, observe the CODER DECODER FAULT lamp on the synchronizer front panel.

(5) If the CODER DECODER FAULT lamp is lighted, the repaired delay line module is still defective. Set the POWER circuit breakers on the synchronizer and on the control box to OFF, remove the defective delay line module from the synchronizer, and repeat the troubleshooting and repair sequence from step (1) above.

(6) If the CODER DECODER FAULT lamp is not lighted, perform the challenge encoding circuit test procedure given in paragraphs 14–14 and 14–15. If any unsatisfactory results are obtained, the repaired delay line module is still defective. Set the POWER circuit breakers on the synchronizer and on the control box to OFF, remove the defective delay line module from the synchronizer, and repeat the troubleshooting and repair sequence from step (1) above.

Section II. INTERFACE MODULE 1A2A1 TROUBLESHOOTING AND REPAIR

19–3. General

The interface module contains parts of the timing, challenge encoding, and reply decoding circuits, all of the display video interface circuits and all of the fault indication circuits except the four front panel FAULT lamps. To isolate and correct a trouble in the interface module, therefore, the entire sequence of paragraph 19–2*b* must be carried out.

19–4. Interface Module Connector Resistance Measurements

a. Conditions of Measurement. The following

chart gives the resistance values measured at the connector pins of a properly operating interface module. These values were measured with the module removed from the synchronizer, but with all eight printed wiring cards installed. The measurements were taken with respect to five pins which normally serve as ground and signal return pins when the interface module is installed in a synchronizer: 1A2A1P1–22, –26, and –50; and 1A2A1P2–1 and –17. These pins were interconnected by means of jumpers to provide a single common connection for the multimeter (operated as an ohmmeter). For the forward resistance measurements, the negative ohmmeter probe was connected to the jumpered group of pins, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive ohmmeter probe was connected to the jumpered group of pins, and the negative probe was touched to each of the listed pins.

b. Interface Module 1A2A1 Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A1P1–2	R X 100	3800	R X 100	2800
1A2A1P1–3	R X 100	2600	R X 100	700
1A2A1P1–4	R X 100	2500	R X 100	700
1A2A1P1–5	R X 100	2500	R X 100	700
1A2A1P1–6	R X 10,000	5 Mego	R X 100	800
1A2A1P1–7	R X 100	2500	R X 100	700
1A2A1P1–8	R X 100	2500	R X 100	700
1A2A1P1–9	R X 10,000	650K	R X 100	1300
1A2A1P1–10	R X 10,000	5 Mego	R X 100	1200
1A2A1P1–11	R X 10,000	5 Mego	R X 100	1200
1A2A1P1–12	R X 10,000	5 Mego	R X 100	1300
1A2A1P1–13	R X 10,000	5 Mego	R X 100	1150
1A2A1P1–14	R X 10,000	800K	R X 100	1600
1A2A1P1–15	R X 100	5000	R X 100	9500
1A2A1P1–16	R X 1	0.0	R X 1	0.0
1A2A1P1–18	R X 100	600	R X 100	480
1A2A1P1–19	R X 10,000	520K	R X 100	850
1A2A1P1–20	R X 10,000	750K	R X 100	780
1A2A1P1–21	R X 100	700	R X 1	7.2
1A2A1P1–22	R X 1	0.0	R X 1	0.0
1A2A1P1–24	R X 1	70	R X 1	15
1A2A1P1–25	R X 1	0.0	R X 1	0.0
1A2A1P1–26	R X 1	0.0	R X 1	0.0
1A2A1P1–27	R X 100	4500	R X 100	9500
1A2A1P1–28	R X 1	0.0	R X 1	0.0
1A2A1P1–30	R X 100	4800	R X 100	9500
1A2A1P1–31	R X 1	0.0	R X 1	0.0
1A2A1P1–33	R X 100	2800	R X 100	920
1A2A1P1–34	R X 100	4600	R X 100	9500
1A2A1P1–35	R X 1	0.0	R X 1	0.0
1A2A1P1–37	R X 1	100	R X 1	100
1A2A1P1–38	R X 1	0.0	R X 1	0.0
1A2A1P1–40	R X 100	5000	R X 100	9500
1A2A1P1–41	R X 1	0.0	R X 1	0.0
1A2A1P1–42	R X 1	85	R X 1	15
1A2A1P1–43	R X 100	4800	R X 100	9500
1A2A1P1–44	R X 1	0.0	R X 1	0.0
1A2A1P1–46	R X 100	4800	R X 100	9500
1A2A1P1–47	R X 1	0.0	R X 1	0.0
1A2A1P1–49	R X 1	85	R X 1	14
1A2A1P1–50	R X 1	0.0	R X 1	0.0

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A1P2-1	R X 1	0.0	R X 1	0.0
1A2A1P2-3	R X 100	3500	R X 100	2950
1A2A1P2-4	R X 100	3800	R X 100	2900
1A2A1P2-4	R X 100	3800	R X 100	2900
1A2A1P2-7	R X 10,000	1.3 Mego	R X 100	850
1A2A1P2-8	R X 10,000	5 Mego	R X 100	900
1A2A1P2-9	R X 10,000	5 Mego	R X 100	850
1A2A1P2-10	R X 10,000	650K	R X 100	1700
1A2A1P2-11	R X 10,000	750K	R X 100	1650
1A2A1P2-12	R X 10,000	900K	R X 100	1700
1A2A1P2-13	R X 10,000	750K	R X 100	1700
1A2A1P2-14	R X 10,000	900K	R X 100	1700
1A2A1P2-15	R X 100	850	R X 10,000	5 Mego
1A2A1P2-16	R X 100	850	R X 10,000	5 Mego
1A2A1P2-17	R X 1	0.0	R X 1	0.0
1A2A1P2-18	R X 100	600	R X 100	480
1A2A1P2-20	R X 10,000	850K	R X 100	1700
1A2A1P2-21	R X 10,000	900K	R X 100	1700
1A2A1P2-22	R X 100	5800	R X 100	5000
1A2A1P2-23	R X 100	6000	R X 100	5000
1A2A1P2-24	R X 100	6000	R X 100	5000
1A2A1P2-25	R X 100	6000	R X 100	5000
1A2A1P2-26	R X 100	6000	R X 100	5000
1A2A1P2-27	R X 100	6000	R X 100	5000
1A2A1P2-28	R X 100	6000	R X 100	5000
1A2A1P2-29	R X 100	6000	R X 100	5000
1A2A1P2-30	R X 100	6000	R X 100	5000
1A2A1P2-31	R X 10,000	850K	R X 100	800
1A2A1P2-32	R X 10,000	5 Mego	R X 100	850
1A2A1P2-33	R X 100	2700	R X 100	900
1A2A1P2-34	R X 100	750	R X 1	7.2
1A2A1P2-35	R X 1	0.0	R X 1	0.0
1A2A1P2-36	R X 10,000	750K	R X 100	1300
1A2A1P2-37	R X 10,000	680K	R X 100	900
1A2A1P2-38	R X 100	3800	R X 100	2900
1A2A1P2-39	R X 10,000	900K	R X 100	1600
1A2A1P2-40	R X 10,000	560K	R X 100	800
1A2A1P2-41	R X 10,000	550K	R X 100	750
1A2A1P2-42	R X 10,000	480K	R X 100	700
1A2A1P2-43	R X 10,000	850K	R X 100	1650
1A2A1P2-44	R X 10,000	520K	R X 100	1750
1A2A1P2-45	R X 10,000	850K	R X 100	1700
1A2A1P2-46	R X 10,000	550K	R X 100	1300
1A2A1P2-47	R X 10,000	550K	R X 100	1500
1A2A1P2-48	R X 10,000	550K	R X 100	1200
1A2A1P2-49	R X 10,000	5 Mego	R X 100	800
1A2A1P2-50	R X 100	750	R X 1	7.5

19-5. Interface Module Part Locations
(figs. 19-1 and 19-2)

Figure 19-1 shows a top view of the interface module with its eight printed wiring cards installed, and identifies the test jacks and adjustment potentiometers on those cards. Figure 19-2 is a bottom view which identifies module connectors 1A2A1P1 and 1A2A1P2 and the eight printed wiring card receptacles.

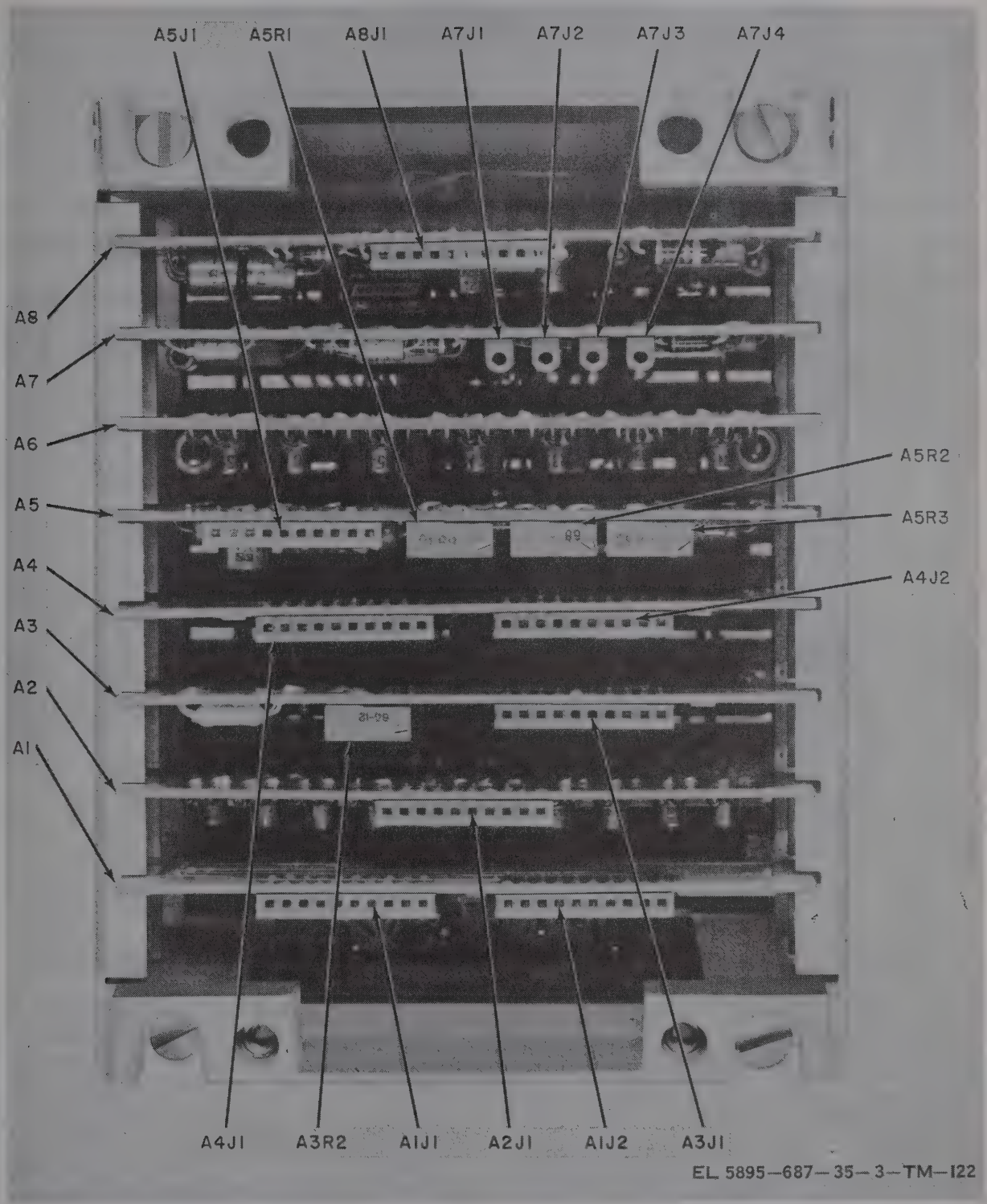


Figure 19-1. Interface module 1A2A1, top view.

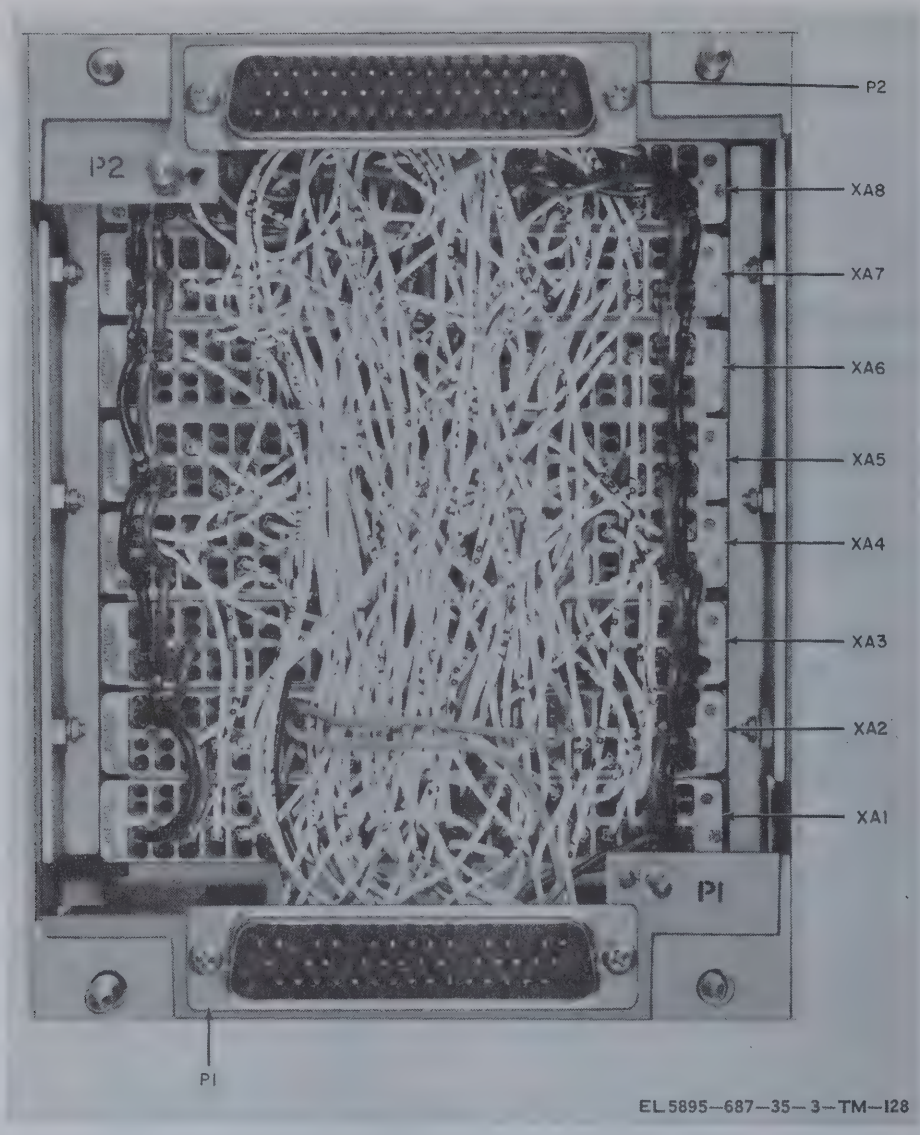


Figure 19-2. Interface module 1A2A1, bottom view.

Section III. CODER-DECODER MODULE 1A2A2 TROUBLESHOOTING AND REPAIR

19-6. General

The coder-decoder module contains most of the parts of the challenge encoding circuits and most of the parts of the reply decoding circuits. The remaining parts of those circuits are physically located within interface module 1A2A1. To isolate and correct a trouble in the coder-decoder module, therefore, the entire sequence of paragraph 19-2*b* must be carried out.

19-7. Coder-Decoder Module Connector Resistance Measurements

a. Conditions of Measurement. The following chart gives the resistance values measured at the connector pins of a properly operating coder-decoder module. These values were measured with the module removed from the synchronizer, but with all eight printed wiring cards installed. The measurements were taken with respect to the three pins which normally serve as ground and signal return pins when the coder-decoder module is installed in a synchronizer: 1A2A2P1-10; and 1A2A2P2-1 and -17. These pins were interconnected by means of jumpers to provide a single common connection for the multimeter (operated as an ohmmeter). For the forward resistance measurements, the negative ohmmeter probe was connected to the jumpered group

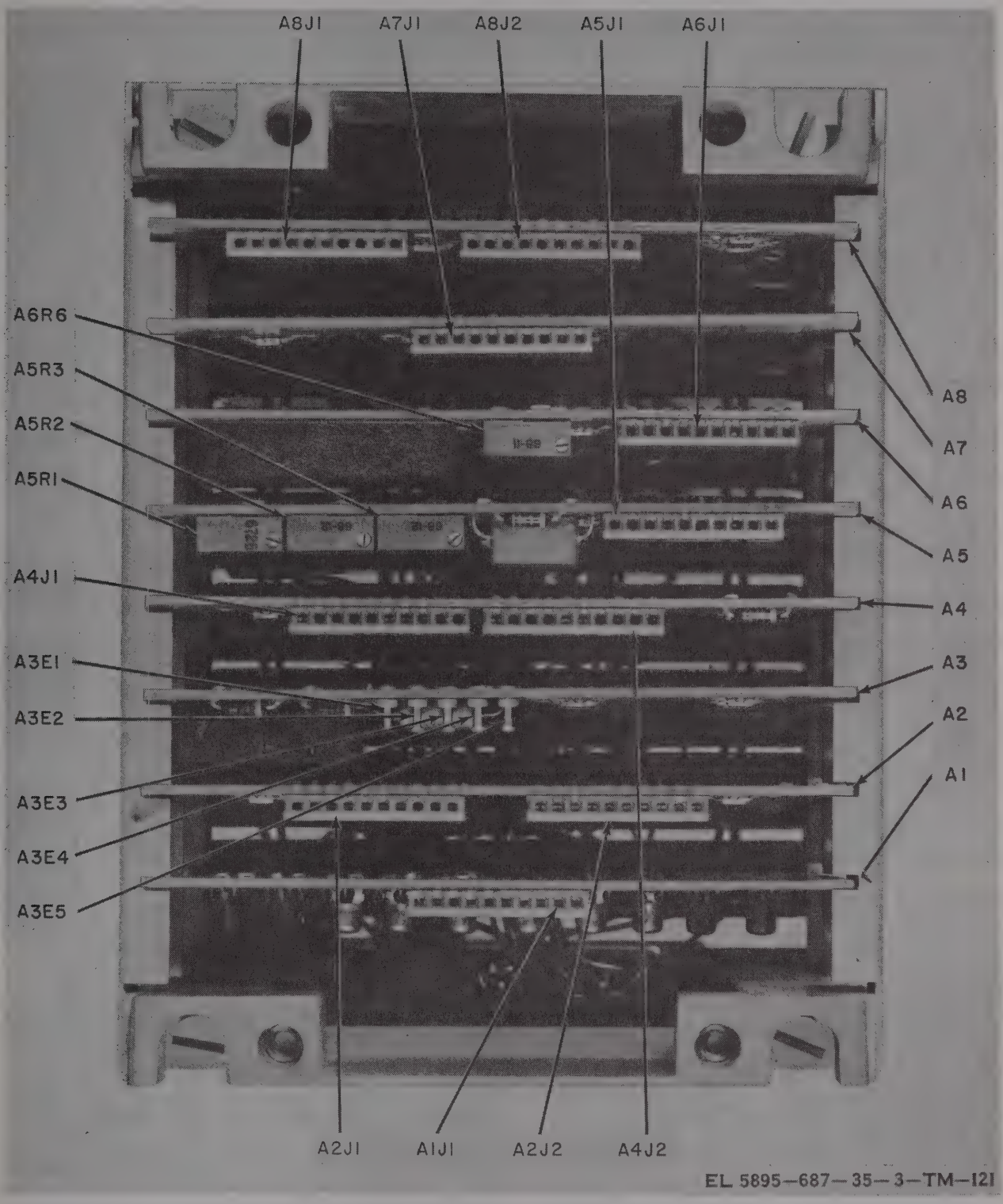


Figure 19-3. Coder-decoder module 1A2A2, top view.

of pins, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to the jumpered group of pins, and the negative probe was touched to each of the listed pins.

b. Coder-Decoder Module 1A2A2 Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A2P1-1	R X 100	8000	R X 100	5000
1A2A2P1-2	R X 100	8000	R X 100	5000
1A2A2P1-3	R X 10,000	350K	R X 100	1400
1A2A2P1-4	R X 10,000	350K	R X 100	1400
1A2A2P1-5	R X 100	8000	R X 100	5000
1A2A2P1-6	R X 100	8000	R X 100	5000
1A2A2P1-7	R X 100	4400	R X 100	800
1A2A2P1-8	R X 10,000	5 Mego	R X 100	900
1A2A2P1-9	R X 10,000	550K	R X 100	800
1A2A2P1-10	R X 1	0.0	R X 1	0.0
1A2A2P1-12	R X 10,000	900K	R X 100	5500
1A2A2P1-13	R X 1	0.0	R X 1	0.0
1A2A2P1-14	R X 10,000	480K	R X 100	4000
1A2A2P1-15	R X 10,000	500K	R X 100	10K
1A2A2P1-16	R X 10,000	530K	R X 100	10K
1A2A2P1-17	R X 100	1100	R X 1	200
1A2A2P1-18	R X 10,000	1 Mego	R X 100	1400
1A2A2P1-19	R X 100	8000	R X 100	4700
1A2A2P1-20	R X 100	8000	R X 100	4700
1A2A2P1-21	R X 100	8000	R X 100	4700
1A2A2P1-22	R X 100	8000	R X 100	4700
1A2A2P1-23	R X 10,000	520K	R X 100	850
1A2A2P1-24	R X 10,000	380K	R X 100	1850
1A2A2P1-27	R X 10,000	1.1 Mego	R X 100	4500
1A2A2P1-28	R X 10,000	1.1 Mego	R X 100	5500
1A2A2P1-29	R X 10,000	1.1 Mego	R X 100	6500
1A2A2P1-30	R X 100	1100	R X 100	380
1A2A2P1-31	R X 10,000	500K	R X 100	10K
1A2A2P1-32	R X 10,000	520K	R X 100	10K
1A2A2P1-33	R X 10,000	800K	R X 100	10K
1A2A2P1-34	R X 10,000	600K	R X 100	850
1A2A2P1-35	R X 10,000	400K	R X 100	1350
1A2A2P1-36	R X 100	8000	R X 100	4800
1A2A2P1-37	R X 100	8000	R X 100	4800
1A2A2P1-38	R X 10,000	350K	R X 100	1400
1A2A2P1-39	R X 10,000	5 Mego	R X 100	850
1A2A2P1-40	R X 10,000	460K	R X 100	650
1A2A2P1-45	R X 10,000	800K	R X 100	4500
1A2A2P1-46	R X 10,000	1 Mego	R X 100	7000
1A2A2P1-47	R X 10,000	1.1 Mego	R X 100	7000
1A2A2P1-48	R X 10,000	800K	R X 100	8000
1A2A2P1-49	R X 10,000	360K	R X 100	11K
1A2A2P1-50	R X 10,000	1 Mego	R X 100	9000
1A2A2P2-1	R X 1	0.0	R X 1	0.0
1A2A2P2-3	R X 10,000	420K	R X 100	1300
1A2A2P2-5	R X 1	75	R X 1	75
1A2A2P2-6	R X 1	0.0	R X 1	0.0
1A2A2P2-7	R X 10,000	5 Mego	R X 100	800
1A2A2P2-8	R X 10,000	120K	R X 100	700
1A2A2P2-9	R X 100	2300	R X 100	1200
1A2A2P2-10	R X 10,000	450K	R X 100	850
1A2A2P2-11	R X 10,000	360K	R X 100	850
1A2A2P2-13	R X 10,000	650K	R X 100	750
1A2A2P2-14	R X 10,000	5 Mego	R X 100	750

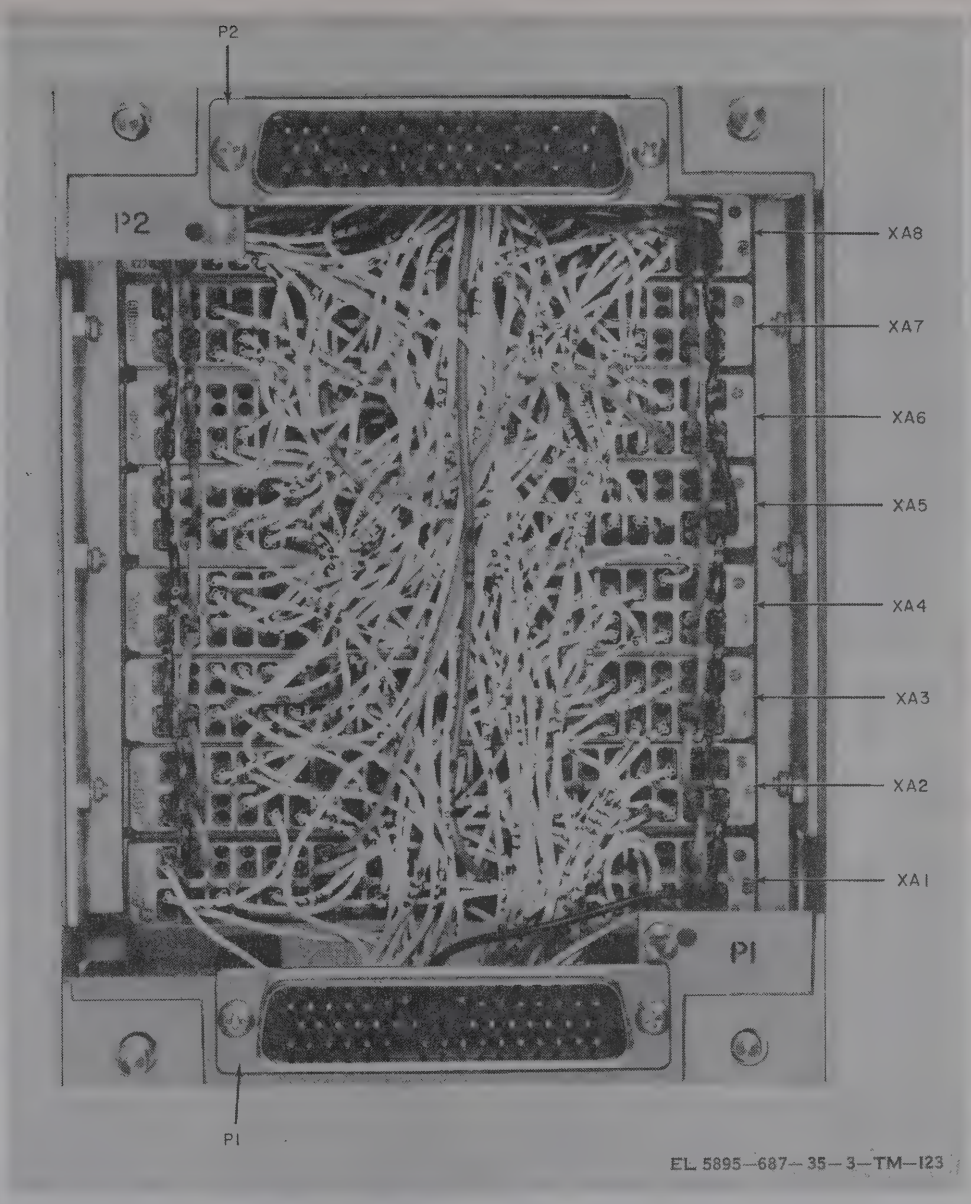


Figure 19-4. Coder-decoder module 1A2A2, bottom view.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A2P2-15	R X 10,000	650K	R X 100	3800
1A2A2P2-17	R X 1	0.0	R X 1	0.0
1A2A2P2-18	R X 100	1300	R X 100	650
1A2A2P2-20	R X 10,000	550K	R X 100	10K
1A2A2P2-22	R X 100	460	R X 100	450

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A2P2-24	R X 10,000	5 Mego	R X 100	750
1A2A2P2-25	R X 10,000	520K	R X 100	1700
1A2A2P2-26	R X 10,000	520K	R X 100	700
1A2A2P2-28	R X 10,000	520K	R X 100	1650
1A2A2P2-32	R X 10,000	650K	R X 100	1300

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A2P2–33	R X 100	4500	R X 100	2600
1A2A2P2–34	R X 100	800	R X 1	6.5
1A2A2P2–36	R X 10,000	48K	R X 1	28
1A2A2P2–38	R X 10,000	5 Mego	R X 1	46
1A2A2P2–40	R X 10,000	5 Mego	R X 100	800
1A2A2P2–41	R X 10,000	550K	R X 100	1750
1A2A2P2–42	R X 100	2300	R X 100	1250
1A2A2P2–44	R X 10,000	450K	R X 100	850
1A2A2P2–46	R X 10,000	520K	R X 100	800
1A2A2P2–48	R X 10,000	440K	R X 100	750
1A2A2P2–49	R X 10,000	5 Mego	R X 100	800
1A2A2P2–50	R X 100	800	R X 1	6.5

19–8. Coder-Decoder Module Part Locations (figs. 19–3 and 19–4)

Figure 19–3 shows a top view of the coder-decoder module with its eight printed wiring cards installed, and identifies the test jacks, test points, and adjustment potentiometers on those cards. Figure 19–4 is a bottom view which identifies module connectors 1A2A2P1 and 1A2A2P2 and the eight printed wiring card receptacles.

Section IV. POWER SUPPLY MODULE 1A2A3 TROUBLESHOOTING AND REPAIR

19–9. General

The power supply module contains all parts of the power supply circuits except voltage selector 1A2S1 and voltmeter 1A2M1 on the front panel and components board 1A2A7 just behind the front panel. To isolate and correct a trouble in the power supply module, therefore, the sequence of activities that must be carried out is the same as given in paragraph 19–2*b*, except that overall synchronizer troubleshooting can be omitted.

19–10. Power Supply Module Connector Resistance Measurements

a. Conditions of Measurement. The following chart gives the resistance values measured at the connector pins of a properly operating power supply module. These values were measured with the module removed from the synchronizer, but with all three printed wiring cards installed. The measurements were taken with respect to the eight pins which normally serve as voltage returns (grounds) when the power supply module is installed in a synchronizer: 1A2A3P1–14, –15, –17, –18, –20, –21, –23, and –24. These pins were interconnected by means of jumpers to provide a single common connection for the multimeter (operated as an ohmmeter). For the forward resistance measurements, the negative ohmmeter probe was connected to the jumpered group of pins, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to the jumpered group of pins, and the negative probe was touched to each of the listed pins.

b. Power Supply Module 1A2A3 Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A3P1–1	R X 100	800	R X 100	920
1A2A3P1–2	R X 100	800	R X 100	920
1A2A3P1–4	R X 100	550	R X 100	350
1A2A3P1–5	R X 100	550	R X 100	350
1A2A3P1–7	R X 100	1200	R X 100	380
1A2A3P1–8	R X 100	1200	R X 100	380
1A2A3P1–10	R X 100	550	R X 10,000	15K
1A2A3P1–11	R X 100	550	R X 10,000	15K
1A2A3P1–14	R X 1	0.0	R X 1	0.0
1A2A3P1–15	R X 1	0.0	R X 1	0.0
1A2A3P1–17	R X 1	0.0	R X 1	0.0
1A2A3P1–18	R X 1	0.0	R X 1	0.0
1A2A3P1–20	R X 1	0.0	R X 1	0.0
1A2A3P1–21	R X 1	0.0	R X 1	0.0
1A2A3P1–23	R X 1	0.0	R X 1	0.0
1A2A3P1–24	R X 1	0.0	R X 1	0.0

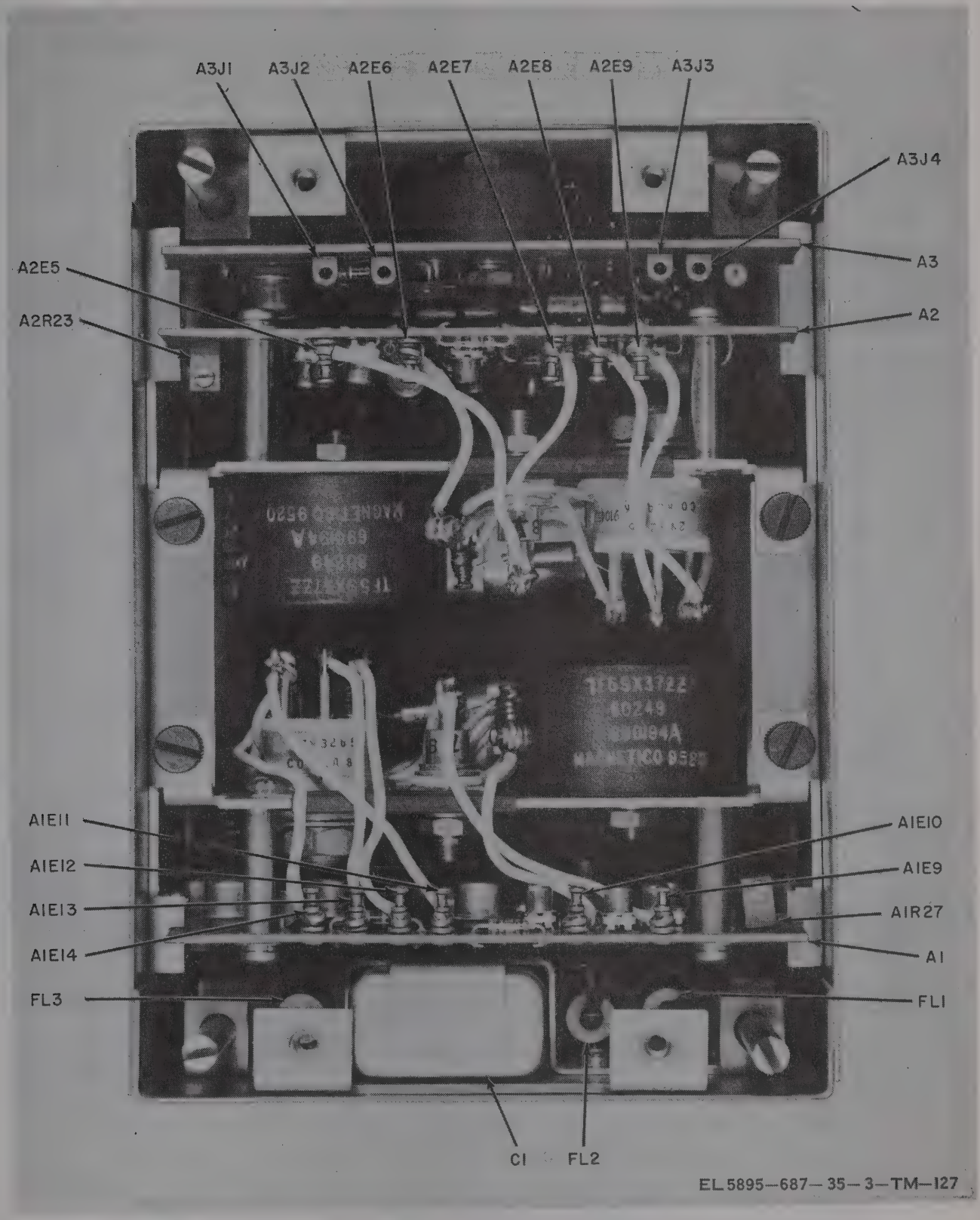


Figure 19-5. Power supply module 1A2A3, top view.

19-11. Power Supply Module Part Locations
(figs. 19-5 through 19-8)

Figure 19-5 shows a top view of the power supply module with its three printed wiring cards installed, and identifies the test jacks, test points, and adjustment potentiometers on those cards. Figures 19-6 and 19-7 show top interior views with +12-volt regulator card 1A2A3A1 and +5-volt regulator card 1A2A3A2 removed to expose the printed wiring card receptacles and the power supply module filter parts. Figure 19-8 is a bottom view which identifies module connector 1A2A3P1.

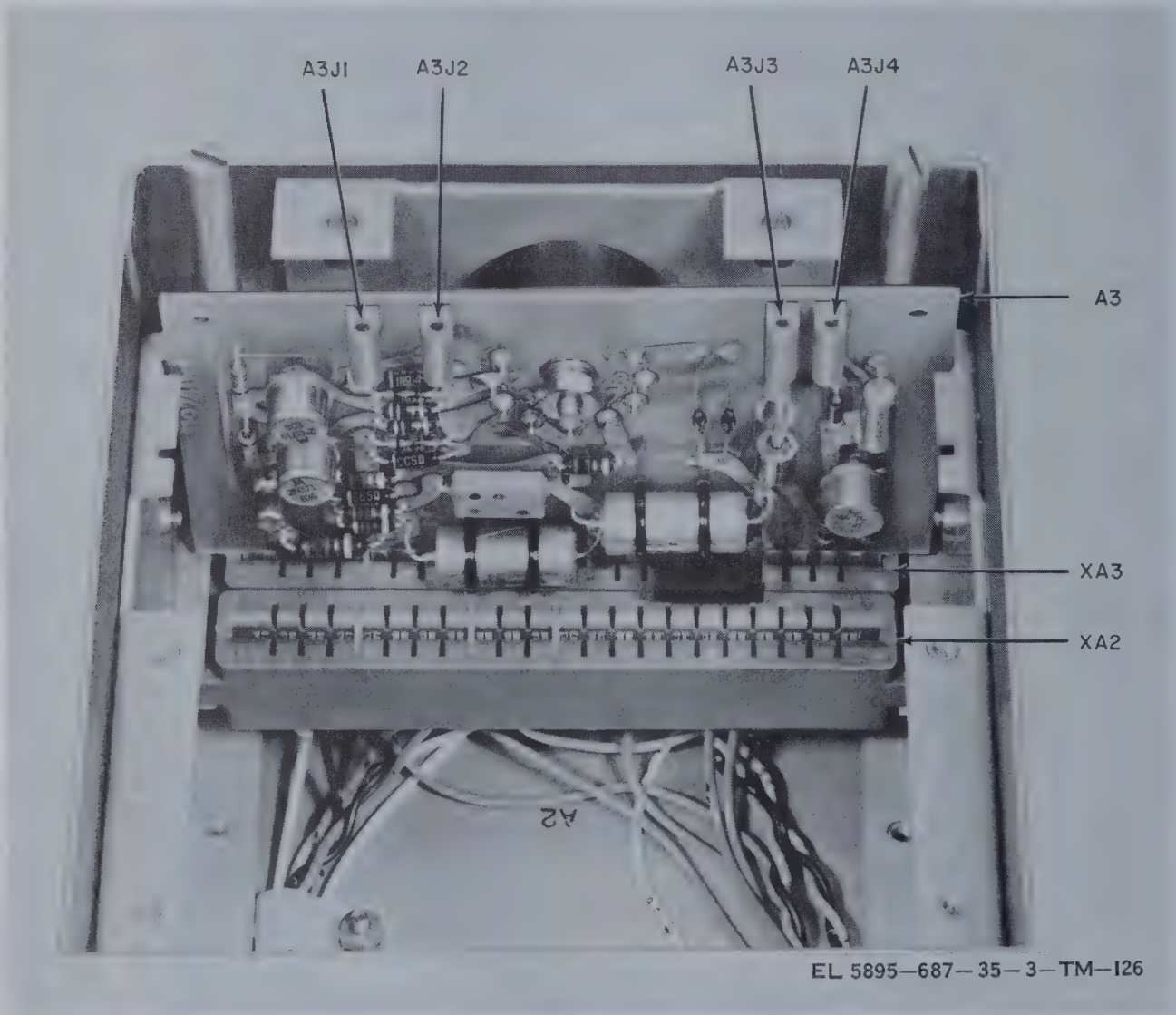


Figure 19-6. Power supply module 1A2A3, interior rear view with +12-volt reegulator card and +5-volt regulator card removed.

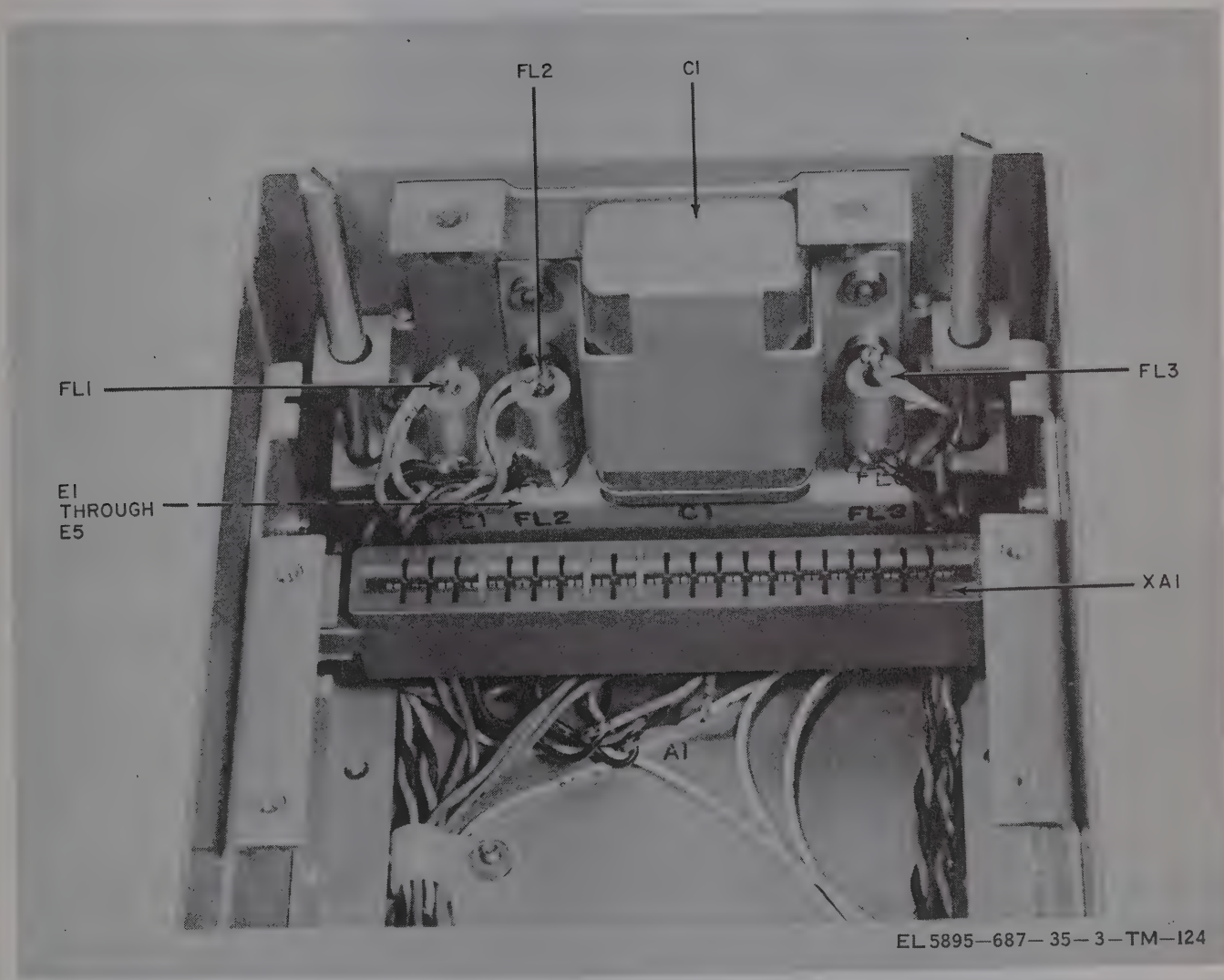


Figure 19-7. Power supply module 1A2A3, interior front view with +12-volt regulator card and +5-volt regulator card removed.

Figure 19-8. Power supply module 1A2A3, bottom view.

Section V. TIMING MODULE 1A2A4 TROUBLESHOOTING AND REPAIR

19-12. General

The timing module contains most of the parts of the timing circuits. The remaining parts of those circuits are physically located within interface module 1A2A1. To isolate and correct a trouble in the timing module, therefore, the sequence of activities that must be carried out is the same as given in paragraph 19-2*b*, except that overall synchronizer troubleshooting can be omitted.

19-13. Timing Module Connector Resistance Measurements

a. Conditions of Measurement. The following chart gives the resistance values measured at the connector pins of a properly operating timing module. These values were measured with the module removed from the synchronizer, but with all three printed wiring cards installed, and with program connector 1A2A4A2P1 inserted into 1A2A4A2J1. The measurements were taken with respect to the two pins which normally serve as ground and signal returns when the timing module is installed in a synchronizer: 1A2A4P1-1, and -17. These pins were interconnected by means of a jumper to provide a single common connection for the multimeter (operated as an ohmmeter). For the forward resistance measurements, the negative ohmmeter probe was connected to the jumpered group of pins, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to the jumpered group of pins, and the negative probe was touched to each of the listed pins.

b. Timing Module 1A2A4 Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A4P1-1	R X 1	0.0	R X 1	0.0
1A2A4P1-2	R X 10,000	5 Mego	R X 100	850
1A2A4P1-4	R X 100	3800	R X 100	720
1A2A4P1-10	R X 10,000	700K	R X 100	800
1A2A4P1-12	R X 10,000	700K	R X 100	850
1A2A4P1-13	R X 100	3800	R X 100	650
1A2A4P1-14	R X 100	3000	R X 100	650
1A2A4P1-15	R X 100	3500	R X 100	750
1A2A4P1-16	R X 10,000	200K	R X 100	1000
1A2A4P1-17	R X 1	0.0	R X 1	0.0
1A2A4P1-28	R X 10,000	650K	R X 100	350
1A2A4P1-34	R X 100	920	R X 1	10
1A2A4P1-50	R X 100	950	R X 1	10

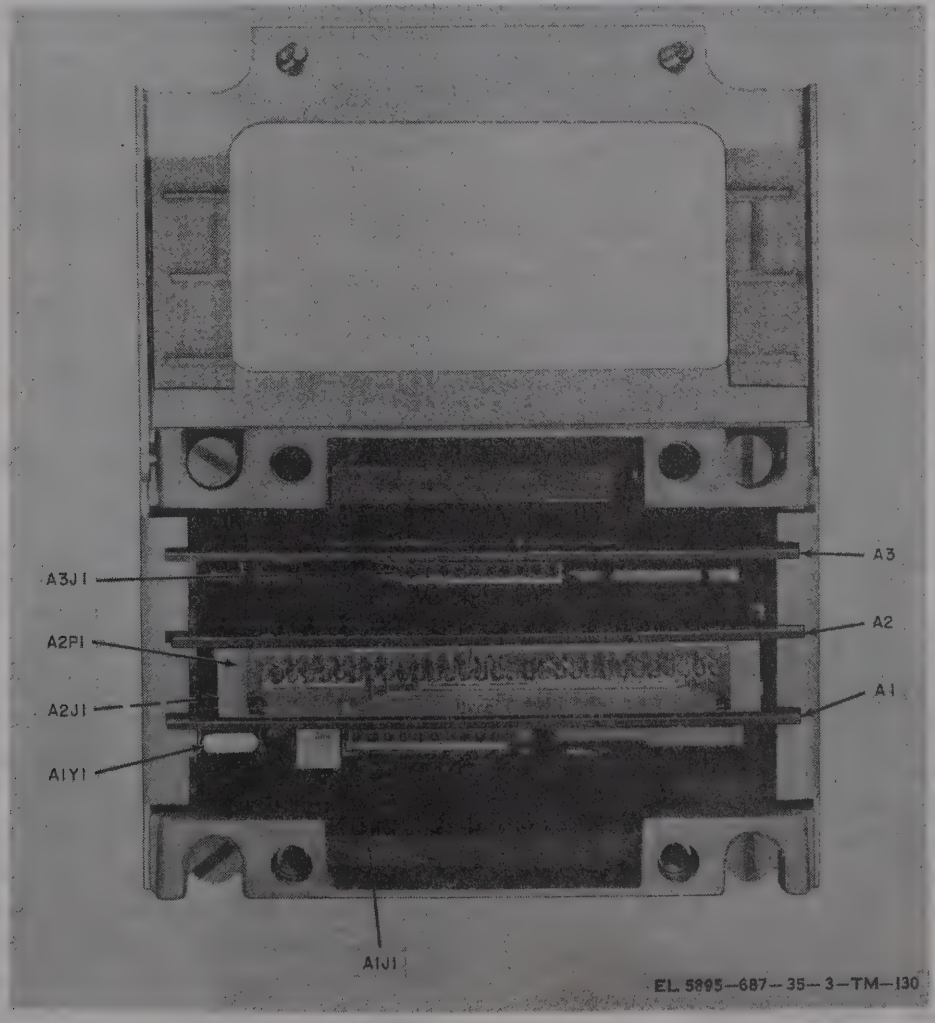


Figure 19-9. Timing module 1A2A4, top view.

19–14. Timing Module Part Locations
(figs. 19–9 and 19–10)

Figure 19–9 shows a top view of the timing module with its three printed wiring cards installed, and with program connector 1A2A4A2P1 inserted into 1A2A4A2J1. Figure 19–10 is a bottom view which identifies module connector 1A2A4P1 and the three printed wiring card receptacles.

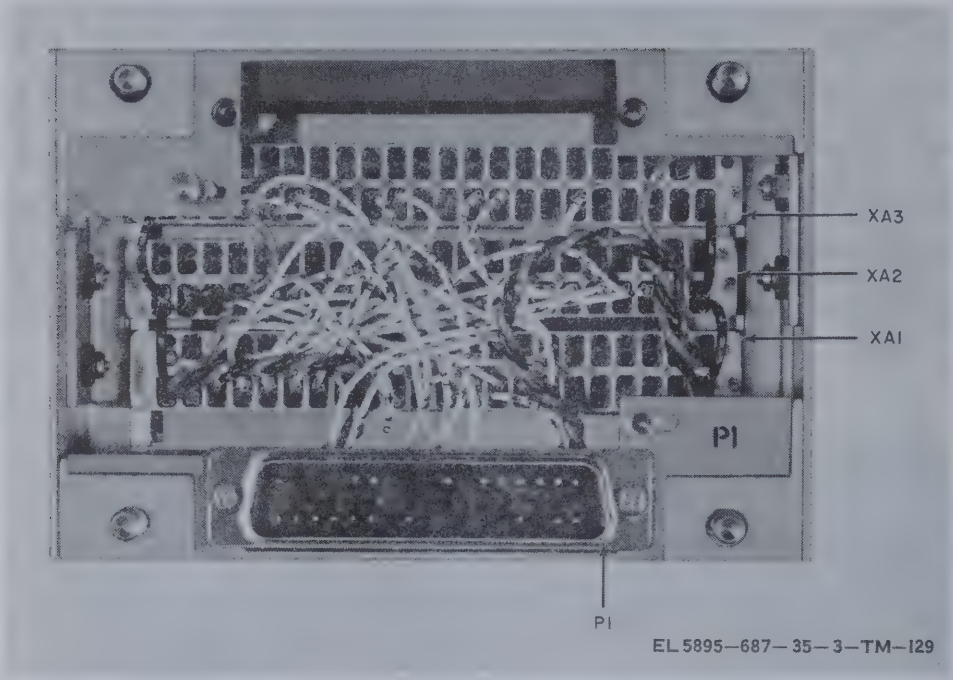


Figure 19–10. Timing module 1A2A4, bottom view.

Section VI. DELAY LINE MODULE 1A2A5 TROUBLESHOOTING AND REPAIR

19–15. General

The delay line module is time shared between the challenge encoding circuits and the reply decoding circuits, but is electrically composed only of sealed (nonrepairable) delay line 1A2A5DL1, module connector 1A2A5P1, and the wiring between them. To isolate and correct a trouble in the delay line module, therefore, the sequence of activities that must be carried out is as given in paragraph 19–2*c*.

19–16. Delay Line Module Connector Resistance Measurements

a. Conditions of Measurement. The following chart gives the resistance values measured at the connector pins of a properly operating delay line module. These values were measured with the module removed from the synchronizer. The measurements were taken with respect to pin 1A2A5P1–20, which normally serves as the delay line common pin when the delay line module is installed in a synchronizer. For the forward resistance measurements, the negative probe of the multimeter (operated as an ohmmeter) was connected to 1A2A5P1–20, and the positive probe was touched to each of the listed pins. For the reverse resistance readings, the positive probe of the multimeter (as an ohmmeter) was connected to 1A2A5P1–20 and the negative probe was touched to each of the listed pins.

b. Delay Line Module 1A2A5 Connector Resistance Measurements.

Connector pin	Resistance in ohms			
	Meter range	Forward	Meter range	Reverse
1A2A4P1–7	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–8	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–9	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–10	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–11	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–12	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–13	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–14	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–15	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–16	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–17	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–18	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–19	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–20	R X 1	0.0		
1A2A5P1–21	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–22	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–23	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–24	R X 10,000	5 Mego	R X 10,000	5 Mego
1A2A5P1–25	R X 10,000	5 Mego	R X 10,000	5 Mego

19–17. Delay Line Module Part Locations (fig. 19–11)

Figure 19–11 shows a bottom view of the delay line module which identifies delay line 1A2A5DL1 and module connector 1A2A5P1.

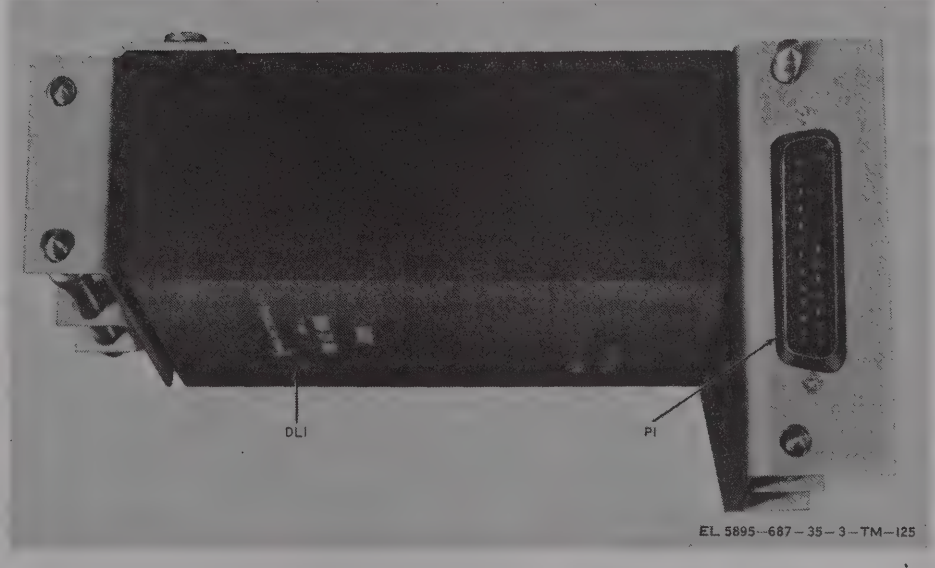


Figure 19–11. Delay line module 1A2A5.

CHAPTER 20

PRINTED WIRING CARD TROUBLESHOOTING AND REPAIR

Section I. INTRODUCTION

20-1. General

a. This chapter presents troubleshooting and testing information for the 22 printed wiring cards in the synchronizer. The information is presented in 21 separate sections, one section for each printed wiring card in reference designation order except for the two identical and interchangeable level shifter cards. Those two cards, 1A2A1A2 and 1A2A2A1, are covered in a single section (section III) which is applicable to either of the two cards.

b. The troubleshooting procedure given for each card is based on the assumptions listed in paragraph 12-2 and the further assumption that the card is definitely known to be defective, either because it was returned as defective by the using activity, or because the trouble has been localized to the card by means of other troubleshooting procedures. If there is any doubt, perform overall synchronizer troubleshooting as directed in chapter 12 to sectionalize the trouble to one of the major functional circuit groups, and then perform circuit troubleshooting as directed in the corresponding circuit troubleshooting and repair chapter to localize the trouble to the printed wiring card.

c. The troubleshooting and testing procedures, voltage measurements, and waveforms given for each card are based on operation of the card in the synchronizer of the hot mockup shown in figure 24-16. For some cards, however, one or more of the items of test equipment shown in figure 24-16 are not used and may be omitted. In those cases, the test equipment and preparation actually required are covered in the corresponding "Test Equipment Required" and "Preparation for Troubleshooting" paragraphs.

20-2. Printed Wiring Card Troubleshooting and Repair Sequence

a. The complete troubleshooting and repair sequence given in *b* below, applies to any synchronizer printed wiring card that has been returned individually from the using activity. When trouble has been localized to a printed wiring card by means of overall synchronizer troubleshooting and/or circuit troubleshooting, the first step (short circuit check) may be bypassed, and with the card already installed in the hot mockup synchronizer the sequence can begin with *b*(3) below.

b. When a defective printed wiring card is returned from the using activity, the required troubleshooting and repair sequence is as follows:

(1) Check the card for short circuits by comparing resistance measurements at its etched connector pins (card pins) with the values given in the corresponding section of this chapter. If any short circuits are detected by these measurements, remove the short circuits before continuing with this sequence.

(2) Install the card in an otherwise satisfactory synchronizer for hot mockup troubleshooting.

(3) Perform the card troubleshooting procedure given in the corresponding section of this chapter. This will isolate the trouble to a stage or integrated circuit.

(4) If the trouble is isolated to a stage containing discrete parts, test the parts to determine which part is defective. If isolated to an integrated circuit, the integrated circuit is the defective part.

(5) Replace the defective part in accordance with the information and instructions referenced in paragraph 11-3*l*. This repairs the card.

(6) After the card has been repaired, check it for short circuits which might have been introduced during the repair by comparing resistance measurements at its pins with the values given in the corresponding section of this chapter, as in (1) above.

(7) Test the repaired card by installing it in an otherwise satisfactory (hot mockup) synchronizer and performing the card test procedure given in the corresponding section of this chapter.

Section II. INTERFACE SELF-TEST CARD 1A2A1A1 TROUBLESHOOTING AND REPAIR

20-3. General

This section presents specific troubleshooting and testing information for interface self-test card 1A2A1A1. For troubleshooting, paragraph 20-4 lists helpful data located in other parts of this manual, and paragraphs 20-5 and 20-6 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20-7 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-8 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-1 shows the card waveforms which are of significance in troubleshooting and testing.

20-4. Reference Data

The data listed in the following chart will be helpful when troubleshooting the interface self-test card:

Reference	*Data*
Para 7-15	Decoded reply and delayed video self-test circuit functioning.
Para 7-16	Target present self-test circuit functioning.
Para 7-17	Friend self-test circuit functioning.
Para 7-18	Fault accumulator circuit functioning.
Fig. 24-19	Interface self-test card 1A2A1A1, schematic diagram.

20-5. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the interface self-test card are the same as for overall synchronizer troubleshooting (paras 12-4 and 12-5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24-16, and proceed as directed in paragraphs 12-5*c* through *i*.

20-6. Troubleshooting Chart

a. Preliminary Procedure. With the interface self-test card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24-16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1-3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column.

b. Interface Self-Test Card 1A2A1A1 Troubleshooting Chart.

Step	Test point	Test equipment	Normal indication	Corrective measures
1	J1-7	Oscilloscope	$\overline{\text{Decoded reply fault}}$ (E, fig. 20-1).	If normal, proceed with step 7. If abnormal, perform steps 2 through 6.
2	A11-5	Oscilloscope	Sif correct code video (same as A, fig. 20-1, except inverted).	If abnormal, inverter A11B is defective.

Step	Test point	Test equipment	Normal indication	Corrective measures
3	J1-3	Oscilloscope	$\overline{\text{Self-test decoded reply}}$ (A, fig. 20-1).	If abnormal, A7 is defective. If normal, temporarily hold control box CHALLENGE switch at TEST, and perform step 4.
4	J1-3	Oscilloscope	$\overline{\text{Self-test decoded reply}}$ (same as F, fig. 20-2).	If abnormal, AND A11A is defective. If normal, return CHALLENGE switch to ON, and continue with step 5.
5	J1-2	Oscilloscope	$\overline{\text{Decoded reply}}$ (same as K, fig. 20-3).	If normal, flip-flop A1A is defective. If abnormal, OR A11C or inverter A7C is defective; proceed with step 6.
6	A11-8	Oscilloscope	Decoded reply (same as K, fig. 20-3, except inverted).	If normal, inverter A-7C is defective. If abnormal, OR A11C is defective.
7	J1-4	Oscilloscope	$\overline{\text{Video fault}}$ (B, fig. 20-1)	If normal, proceed with step 9. If abnormal, observe $\overline{\text{delayed target}}$ video at J1-1 (same as J, fig. 20-3, except inverted). If normal at J1-1, flip-flop A1B is defective. If abnormal at J1-1, OR A11D or inverter A8B is defective; proceed with step 8.
8	A11-14	Oscilloscope	Delayed target video (same as J, fig. 20-3).	If normal, inverter A8B is defective. If abnormal, OR A11D is defective.
9	J1-9	Oscilloscope	Self-test strobed target (F, fig. 20-1).	If abnormal, A13 is defective.
10	J2-6	Oscilloscope	$\overline{\text{Target present fault}}$ (high)	If normal, proceed with step 18. If abnormal, perform steps 11 through 17.
11	J2-5	Oscilloscope	$\overline{\text{Self-test end of target}}$ (K, fig. 20-1).	If abnormal, AND A13C is defective.
12	J1-6	Oscilloscope	Self-test stored target (D, fig. 20-1).	If abnormal, A6 is defective.
13	J2-1	Oscilloscope	$\overline{\text{Self-test target present}}$ (H, fig. 20-1).	If abnormal, A4 or AND A5C is defective; proceed with step 14. If normal, place control box PROCESSOR switch at BYPASS, and proceed with step 15.
14	A5-13	Oscilloscope	$\overline{\text{Self-test target present}}$ (same as H, fig. 20-1).	If normal, A4 is defective. If abnormal, AND A5C is defective.

Step	Test point	Test equipment	Normal indication	Corrective measures
15	J2-1	Oscilloscope	$\overline{\text{Delayed target video}}$ (same as J, fig. 20-3, except inverted).	If normal, place control box PROCESSOR switch at IN, and proceed with step 16. If abnormal, check level at A12-5. If A12-5 is high, AND A4C is defective. If A12-5 is abnormal (low), inverter A12B is defective. Place control box PROCESSOR switch at IN.
16	J1-8	Oscilloscope	$\overline{\text{Target present trigger}}$ (same as K, fig. 20-4, except inverted).	If normal, flip-flop A3A is defective. If abnormal, inverter A12D or A8 is defective; proceed with step 17.
17	A12-14	Oscilloscope	$\overline{\text{Target present trigger}}$ (same as K, fig. 20-4, except inverted).	If normal, A8 is defective. If abnormal, inverter A12 is defective.
			STEPS 18 THROUGH 26 ARE TO BE CARRIED OUT IN TEST TARGET MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
18	J1-10	Oscilloscope	$\overline{\text{Friend fault}}$ (high)	If normal, proceed to step 27. If abnormal, perform step 19.
19	J2-2	Oscilloscope	$\overline{\text{Self-test friend present}}$ (J, fig. 20-1).	If normal, proceed with step 25. If abnormal, proceed with step 20.
20	A5-3	Oscilloscope	$\overline{\text{Self-test eyelash trigger}}$ (M, fig. 20-1).	If abnormal, AND A5A is defective. If normal, proceed with step 21.
21	A13-5	Oscilloscope	$\overline{\text{Strobe friend reset}}$ (P, fig. 20-1).	If abnormal, AND A13B is defective. If normal, proceed with step 22.
22	J1-5	Oscilloscope	Self-test friend stored (C, fig. 20-1).	If abnormal, OR flip-flop A4D, A12A is defective. If normal, proceed with step 23.
23	A12-8	Oscilloscope	Self-test friend present (same as J, fig. 20-1, except inverted).	If normal, AND A8D is defective. If abnormal, proceed with step 24.
24	A6-5	Oscilloscope	$\overline{\text{Self-test eyelash trigger}}$ (N, fig. 20-1).	If normal, OR A12C is defective. If abnormal, AND A6B is defective.
25	J2-3	Oscilloscope	$\overline{\text{Friend stored}}$ (same as L, fig. 20-4, except inverted).	If normal, flip-flop A3B is defective. If abnormal, OR A5B or inverter A6A is defective; proceed with step 26.

Step	Test point	Test equipment	Normal indication	Corrective measures
26	A5-5	Oscilloscope	Friend stored (same as L, fig. 20-4).	If normal, inverter A6A is defective. If abnormal, OR A5B is defective.
			STEPS 27 AND 28 ARE TO BE CARRIED OUT UNDER THE SAME CONDITIONS AS STEPS 1 THROUGH 17 (CHALLENGING IN MODE 3/A AND RECEIVING A CORRECTLY CODED REPLY). AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON."	
27	J2-9	Oscilloscope	Combined faults (L, fig. 20-1).	If abnormal, OR A2A is defective.
28	J2-8	Oscilloscope	Low	If normal, A9 is defective. If abnormal, flip-flop A10 is defective.

20-7. Test Procedure

a. The test procedure for the interface self-test card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the interface self-test card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-8. Then prepare a hot mockup as for troubleshooting (para 20-5), and perform the preliminary procedures given in paragraph 20-6*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A1J1-3, $\overline{\text{self-test decoded reply}}$ (A, fig. 20-1).

(2) 1A2A2A1J1-4, $\overline{\text{video fault}}$ (B, fig. 20-1).

(3) 1A2A2A1J1-6, self-test strobed target (D, fig. 20-1).

(4) 1A2A2A1J1-7, $\overline{\text{decoded reply fault}}$ (E, fig. 20-1).

(5) 1A2A2A1J1-9, $\overline{\text{self test strobed target}}$ (F, fig. 20-1).

(6) 1A2A2A1J2-1, $\overline{\text{self-test target present}}$ (H, fig. 20-1).

(7) 1A2A2A1J2-5, $\overline{\text{target clear}}$ (K, fig. 20-1).

(8) 1A2A2A1J2-6, $\overline{\text{target present fault}}$ (should be high).

(9) 1A2A2A1J2-9, combined faults (L, fig. 20-1).

c. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

d. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A1J1-5, self-test friend stored (C, fig. 20-1).

(2) 1A2A2A1J1-9, self-test strobed target (G, fig. 20-1).

(3) 1A2A2A1J1-10, $\overline{\text{friend fault}}$ (should be high).

(4) 1A2A2A1J2-2, $\overline{\text{self-test friend trigger}}$ (J, fig. 20-1).

(5) 1A2A2A1J2-8, previous fault reading (should be low).

(6) 1A2A2A1J2-10, fault reading-before-last (should be low).

20-8. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating interface self-test card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20-5). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-6*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Interface Self-Test Card 1A2A1A1 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1610	RX100	295
4	5.0	RX100	1610	RX100	295
5	3.6	RX10,000	700K	RX100	1100
6	3.8	RX10,000	680K	RX100	1100
7	0.1	RX10,000	740K	RX100	1080
8	0.12	RX10,000	740K	RX100	1050
9	0.1	RX10,000	840K	RX100	1100
10	3.9	RX10,000	670K	RX100	1100
11	3.9	RX10,000	720K	RX100	1080
12	0.15	RX10,000	20,000	RX100	1000
13	3.8	RX10,000	590,000	RX100	1000
14	5.6	RX10,000	760,000	RX100	1100

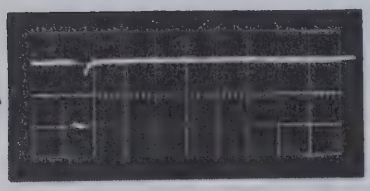
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
15	0.2	RX10,000	640,000	RX100	1150
16	0.1	RX10,000	650,000	RX100	1150
17	NOT USED				
18	5.0	RX10,000	800,000	RX100	1120
19	NOT USED				
20	5.0	RX10,000	850,000	RX100	1120
21	4.3	RX10,000	660,000	RX100	1680
22	0.13	RX10,000	700,000	RX100	1050
23	0.1	RX10,000	460K	RX100	1010
24	4.4	RX10,000	650K	RX100	1150
25	NOT USED				
26	5.0	RX10,000	780K	RX100	1120
27	NOT USED				
28	0.35	RX10,000	650K	RX100	1000
29	NOT USED				
30	3.9	RX10,000	650K	RX100	1100
31	NOT USED				
32	0.14	RX100	6500	RX100	1510
33	NOT USED				
34	5.0	RX10,000	770K		1000
35	0.1	RX100	7000		740
36	0.08	RX10,000	680K		1050
37	NOT USED				
38	3.8	RX10,000	750K		1040
39	NOT USED				
40	0.2	RX10,000	900K		1100
41	5.0	RX100	1610	RX100	295
42	5.0	RX100	1610	RX100	295
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20-9. Waveforms

(fig. 20-1)

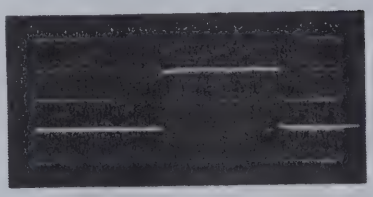
Figure 20-1 shows the interface self-test card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-5 and 20-6*a*).

A



J1-3 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

D



J1-6 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

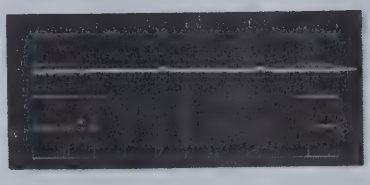
H

J2-1 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

B

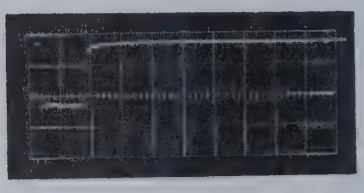
J1-4 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

E



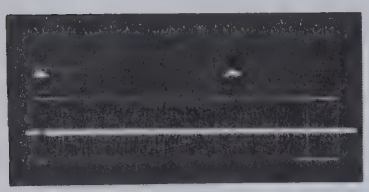
J1-7 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

J



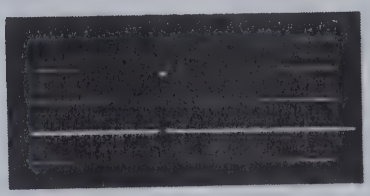
J2-2 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT-

C



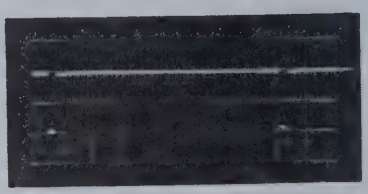
J1-5 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 10
SYNC: INT-

F



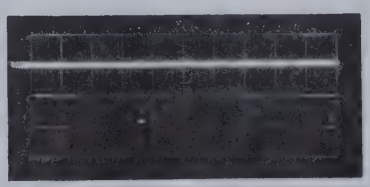
J1-9 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 10
SYNC: INT-

K



J2-5 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT DC + (1J1)

G



J1-9 (NOTE 3) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

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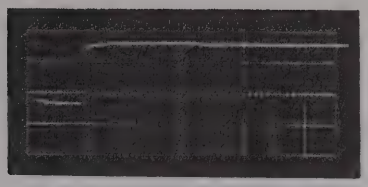
Figure 20-1①. Interface self-test card 1A2A1A1 waveforms (sheet 1 of 2).

L

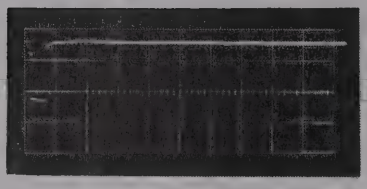
J2-9 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

N



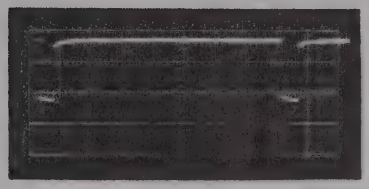
A6-5 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT-

M



A5-3 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT-

P



A13-5 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT-

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, ENABLE TEST TARGET MODE BY HOLDING CHALLENGE SWITCH AT TEST.

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Figure 20–1②. Interface self-test card 1A2A1A1 waveforms (sheet 2 of 2).

Section III. LEVEL SHIFTER CARD 1A2A1A2 OR 1A2A2A1 TROUBLESHOOTING AND REPAIR

20–10. General

This section presents specific troubleshooting and testing information for level shifter card 1A2A1A2 or 1A2A2A1. For troubleshooting, paragraph 20–11 lists helpful data located in other parts of this manual, and paragraphs 20–12, 20–13, and 20–14 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–15 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–16 provides a list of typical voltage and resistance measurements at the etched connector pins.

20–11. Reference Data

The data listed in the following chart will be helpful when troubleshooting the level shifter card:

Reference	*Data*
Para 10-3 ----	Level shifter card 1A2A1A2 or 1A2A2A1 functioning.
Fig. 24-20 ----	Level shifter card 1A2A1A2 or 1A2A2A1 schematic diagram.

20-12. Test Equipment Required

a. If the level shifter card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24-16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Radar test set (only to supply "0" TRIGGER output to 1J1).

(3) Test facilities set (only for cables W32, W41, W42, and W47).

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

20-13. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the XTAL MARK & SYNC panel of the radar test set, and the 28-volt dc power supply to the interrogator group case as shown in figure 24-16.

c. Set the switches on the control box as directed in paragraph 12-5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12-5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output of 28 volts.

20-14. Troubleshooting Chart

a. Preliminary Procedure. With an otherwise satisfactory synchronizer connected into either the complete hot mockup shown in figure 24-16 or the partial hot mockup established in paragraph 20-13*b*, proceed as follows:

(1) The troubleshooting chart applies only to level shifter card 1A2A2A1. If the defective level shifter card is already installed as 1A2A2A1, proceed directly with (2), below. If not, check that the synchronizer POWER circuit breaker is at OFF, remove the known-good level shifter card from 1A2A2XA1, and install the defective level shifter card as 1A2A2A1. Then proceed with (2) below.

(2) At the synchronizer, set the POWER circuit breaker to ON.

(3) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(4) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(5) Check the dc levels at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Level Shifter Card 1A2A1A2 or 1A2A2A1 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	J1–1	Oscilloscope	High	Q1 circuit defective
2	J1–2	Oscilloscope	High	Q2 circuit defective
3	J1–3	Oscilloscope	High	Q3 circuit defective
4	J1–4	Oscilloscope	High	Q4 circuit defective
5	J1–5	Oscilloscope	High	Q5 circuit defective
6	J1–6	Oscilloscope	High	Q8 circuit defective
7	J1–7	Oscilloscope	High	Q6 circuit defective
8	J1–8	Oscilloscope	High	Q7 circuit defective
9	J1–9	Oscilloscope	High	Q9 circuit defective
10	J1–10	Oscilloscope	High	Q10 circuit defective
			FOR STEPS 11 THROUGH 20, RELEASE "CHALLENGE" SWITCH ON CONTROL BOX TO "OFF."	
11	J1–1	Oscilloscope	Low	Q1 shorted
12	J1–2	Oscilloscope	Low	Q2 shorted
13	J1–3	Oscilloscope	Low	Q3 shorted
14	J1–4	Oscilloscope	Low	Q4 shorted
15	J1–5	Oscilloscope	Low	Q5 shorted
16	J1–6	Oscilloscope	Low	Q8 shorted
17	J1–7	Oscilloscope	Low	Q6 shorted
18	J1–8	Oscilloscope	Low	Q7 shorted
19	J1–9	Oscilloscope	Low	Q9 shorted
20	J1–10	Oscilloscope	Low	Q10 shorted

20–15. Test Procedure

a. The test procedure for the level shifter card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the level shifter card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–16. Then prepare a hot mockup as for troubleshooting (paras 20–12 and 20–13) and perform the preliminary procedure given in paragraph 20–14*a*, but do not continue

with the troubleshooting chart. Instead, proceed as follows:

(1) Check the dc levels at each contact of 1A2A2A1J1. All ten levels should be high when challenging in mode 3/A, code 7777.

(2) At the control box, release the CHALLENGE switch (to OFF).

(3) Again check the dc levels at each contact of 1A2A2A1J1. In this case (not challenging), all ten levels should be low.

20–16. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The charts below list the values of dc voltage and resistance that were measured at the etched connector pins of two properly operating level shifter cards.

(1) The dc voltages were measured with respect to chassis ground while the cards were extended (installed on extender cards) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20–12 and 20–13). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–14*a*), except that the two cards were extended from their respective sockets, and at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with each card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Level Shifter Card 1A2A1A2 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX10,000	3 Mego	RX100	7000
4	NOT USED				
5	NOT USED				
6	6.0	RX10,000	4 Mego	RX100	8000
7	NOT USED				
8	−0.6	RX10,000	5 Mego	RX100	700
9	NOT USED				
10	6.0	RX10,000	4 Mego	RX100	8500
11	−12.0	RX10,000	4 Mego	RX100	1250

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
12	—0.6	RX10,000	4 Mego	RX100	700
13	NOT USED				
14	6.0	RX10,000	3 Mego	RX100	8500
15	NOT USED				
16	—0.6	RX10,000	5 Mego	RX100	700
17	NOT USED				
18	5.9	RX10,000	3 Mego	RX100	7500
19	12.5	RX10,000	3 Mego	RX100	4200
20	—0.65	RX10,000	4 Mego	RX100	700
21	0.0	RX1	0.0	RX1	0.0
22	5.6	RX10,000	3 Mego	RX100	8000
23	NOT USED				
24	—0.6	RX10,000	5 Mego	RX100	700
25	NOT USED				
26	5.6	RX10,000	2 Mego	RX100	8000
27	NOT USED				
28	—0.6	RX10,000	3 Mego	RX100	700
29	NOT USED				
30	5.6	RX10,000	3 Mego	RX100	8000
31	—12.0	RX10,000	5 Mego	RX100	1250
32	—0.6	RX10,000	5 Mego	RX100	650
33	NOT USED				
34	5.6	RX10,000	4 Mego	RX100	8000
35	NOT USED				
36	—0.65	RX10,000	5 Mego	RX100	700
37	NOT USED				
38	5.6	RX10,000	4 Mego	RX100	8000
39	NOT USED				
40	—0.6	RX10,000	3 Mego	RX100	700

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
41	5.0	RX10,000	3.5 Mego	RX100	7000
42	5.6	RX10,000	3.5 Mego	RX100	8000
43	0.0	RX1	0.0	RX1	0.0
44	−0.65	RX10,000	5 Mego	RX100	700

c. Level Shifter Card 1A2A2A1 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX10,000	3 Mego	RX100	7000
4	NOT USED				
5	NOT USED				
6	5.6	RX10,000	4 Mego	RX100	8000
7	NOT USED				
8	−0.6	RX10,000	5 Mego	RX100	7000
9	NOT USED				
10	5.5	RX10,000	4 Mego	RX100	8500
11	−12.0	RX10,000	4 Mego	RX100	1250
12	−0.6	RX10,000	4 Mego	RX100	700
13	NOT USED				
14	5.5	RX10,000	3 Mego	RX100	8500
15	NOT USED				
16	−0.65	RX10,000	5 Mego	RX100	700
17	NOT USED				
18	5.5	RX10,000	3 Mego	RX100	7500

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
19	12.5	RX10,000	3 Mego	RX100	4200
20	—0.65	RX10,000	4 Mego	RX100	700
21	0.0	RX1	0.0	RX1	0.0
22	5.5	RX10,000	3 Mego	RX100	8000
23	NOT USED				
24	—0.65	RX10,000	5 Mego	RX100	700
25	NOT USED				
26	5.5	RX10,000	2 Mego	RX100	8000
27	NOT USED				
28	—0.65	RX10,000	3 Mego	RX100	700
29	NOT USED				
30	5.5	RX10,000	3 Mego	RX100	8000
31	—12.0	RX10,000	5 Mego	RX100	1250
32	—0.65	RX10,000	5 Mego	RX100	650
33	NOT USED				
34	5.5	RX10,000	4 Mego	RX100	8000
35	NOT USED				
36	—0.65	RX10,000	5 Mego	RX100	700
37	NOT USED				
38	5.5	RX10,000	4 Mego	RX100	8000
39	NOT USED				
40	—0.65	RX10,000	3 Mego	RX100	700
41	5.0	RX10,000	3.5 Mego	RX100	7000
42	5.5	RX10,000	3.5 Mego	RX100	8000
43	0.0	RX1	0.0	RX1	0.0
44	—0.6	RX10,000	5 Mego	RX100	700

Section IV. TEST TARGET GENERATOR CARD 1A2A1A3 TROUBLESHOOTING AND REPAIR

20–17. General

This section presents specific troubleshooting and testing information for test target generator card 1A2A1A3. For troubleshooting, paragraph 20–18 lists helpful data located in other parts of this manual, and paragraphs 20–19, 20–20, and 20–21 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20–23 references the applicable adjustment procedure, and paragraph 20–22 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–24 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–2 shows the card waveforms which are of significance in troubleshooting and testing.

20–18. Reference Data

The data listed in the following chart will be helpful when troubleshooting the test target generator card.

Reference	*Data*
Para 7–13	Test target generator circuit functioning.
Para 7–11	Display gate generation circuit functioning.
Fig. 24–21	Test target generator card 1A2A1A3 schematic diagram.

20–19. Test Equipment Required

a. If the test target generator card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Oscillscope.
(2) Radar test set (only to supply "0" TRIGGER output to 1J1).
(3) Test facilities set (only for cables W32, W41, W42, and W47).
(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–20. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn on the 28-volt dc power supply and adjust it for an output of 28 volts.

20–21. Troubleshooting Chart

a. Preliminary Procedure. With the test target generator card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–20*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Test Target Generator Card 1A2A1A3 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 12	Oscilloscope	$\overline{\text{Display gate}}$ (J, fig. 20–2)	If normal, proceed with step 6. If too wide or too narrow perform adjustment procedure for display gate width potentiometer R2 as described in paragraphs 16–10 and 16–11. If still abnormal, perform steps 2 through 5.
2	A9–5	Oscilloscope	Processor start pretrigger (same as J, fig. 20–18, except inverted).	If abnormal, inverter A9B is defective.
3	A12–3	Oscilloscope	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20–18).	If abnormal, inverter A12A is defective.
4	A5–9	Oscilloscope	Display generator (L, fig. 20–2).	If abnormal, single-shot A5 is defective.
5	A9–3	Oscilloscope	$\overline{\text{Processor self-test gate}}$ (same as D, fig. 20–7, except inverted).	If normal, AND A12C is defective. If abnormal, isolate either to inverter A9A or to flip-flop A8A.
6	J1–6	Oscilloscope	$\overline{\text{Test target video}}$ (F, fig. 20–2).	Proceed with step 7.
7	J1–1	Oscilloscope	Scale-of-64 gate (A, fig. 20–2).	If normal, proceed with step 12. If abnormal, proceed with steps 8 through 11.
8	A12–14	Oscilloscope	High	If abnormal, inverter A12D is defective.
9	A12–5	Oscilloscope	High	If abnormal, inverter A12B is defective.
10	A8–9	Oscilloscope	Scale-of-4 gate (M, fig. 20–2)	If abnormal, flip-flop A8 is defective.
11	A4–9	Oscilloscope	Scale-of-16 gate (K, fig. 20–2)	If normal, flip-flop A1 is defective. If abnormal, flip-flop A4 is defective.
12	J1–2	Oscilloscope	Test target range gate (B, fig. 20–2).	If normal, proceed with step 13.
13	A9–3	Oscilloscope	$\overline{\text{Processor self-test gate}}$ (same as D, fig. 20–7, except inverted).	If normal, flip-flop A13A is defective. If abnormal, inverter A9A is defective.
14	J1–7	Oscilloscope	Enabled strobe (G, fig. 20–2).	If abnormal, A9 is defective.
15	J1–5	Oscilloscope	2^1 bit comparison (E, fig. 20–2).	If normal, proceed with step 16. If abnormal, isolate to A14, A6, A3, or A10.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
16	J1-4	Oscilloscope	2^0 bit comparison (D, fig. 20-2).	If abnormal, isolate to A6 or A3.
17	J1-3	Oscilloscope	2^3 bit comparison (C, fig. 20-2).	If normal, proceed to step 18. If abnormal, isolate to A15, A7, A3, or A11.
18	J1-8	Oscilloscope	2^5 bit comparison (H, fig. 20-2).	If abnormal, isolate to A7 or A3. If normal, A2 is defective.

20-22. Adjustment

The single potentiometer on the test target generator card is display gate width adjustment potentiometer 1A2A1A3R2. This potentiometer is adjusted for a display gate width of 178 μsec (J, fig. 20-2), measured from the leading edge of the processor start pretrigger. The adjustment procedure is given in paragraphs 16-10 and 16-11.

20-23. Test Procedure

a. The test procedure for the test target generator card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the test target generator card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-24. Then prepare a hot mockup as for troubleshooting (paras 20-19 and 20-20) and perform the preliminary procedure given in para 20-21*a*), but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A3J1-1, scale-of-64 gate (A, fig. 20-2).

(2) 1A2A1A3J1-2, test target range gate (B, fig. 20-2).

(3) 1A2A1A3J1-3, 2^3 bit comparison (C, fig. 20-2).

(4) 1A2A1A3J1-4, 2^0 bit comparison (D, fig. 20-2).

(5) 1A2A1A3J1-5, 2^1 bit comparison (E, fig. 20-2).

(6) 1A2A1A3J1-6, $\overline{\text{test target video}}$ (F, fig. 20-2).

(7) 1A2A1A3J1-7, enabled strobe (G, fig. 20-2).

(8) 1A2A1A3J1-8, 2^2 bit comparison (H, fig. 20-2).

(9) 1A2A1A3-12, $\overline{\text{display gate}}$ (J, fig. 20-2).

20-24. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating test target generator card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-19 and 20-20). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-21*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchro-

nizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Test Target Generator Card 1A2A1A3 Etched Connector Pin Voltage and Resistance Measurements.

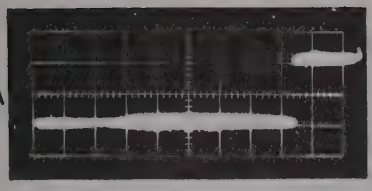
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX1	75	RX1	7
4	5.0	RX1	75	RX1	7
5	Not used				
6	Not used				
7	Not used				
8	Not used				
9	Not used				
10	Not used				
11	Not used				
12	3.9	RX100	55	RX100	7
13	Not used				
14	Not used				
15	Not used				
16	Not used				
17	Not used				
18	0.45	RX100	5000	RX100	1000
19	Not used				
20	−0.6	RX10,000	550K	RX100	1000
21	Not used				
22	5.0	RX10,000	650K	RX100	1000

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
23	Not used				
24	0.35	RX10,000	600K	RX100	1100
25	Not used				
26	4.4	RX100	5700	RX100	7500
27	Not used				
28	Not used				
29	Not used				
30	Not used				
31	Not used				
32	Not used				
33	Not used				
34	Not used				
35	Not used				
36	Not used				
37	Not used				
38	Not used				
39	Not used				
40	Not used				
41	5.0	RX1	75	RX1	7
42	5.0	RX1	75	RX1	7
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–25. Waveforms

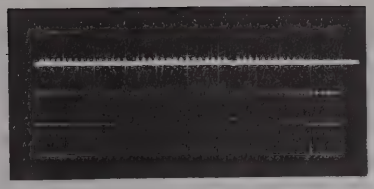
(fig. 20–2)

Figure 20–2 shows the test target generator card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–19, 20–20, and 20–21*a*).



A

J1-1 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 10
SYNC: INT +



F

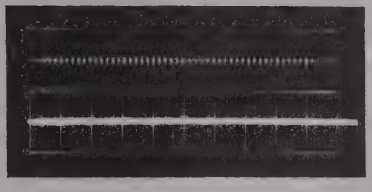
J1-6 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT –

L

A5-9 (NOTE 1) V/CM: 2
SWEEP DELAY: 443 USEC USEC/CM: 20
SYNC: EXT + (1J1)

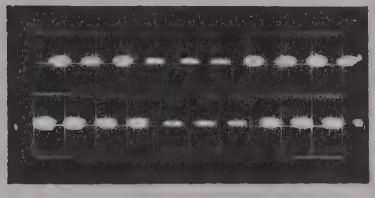
B

J1-2 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



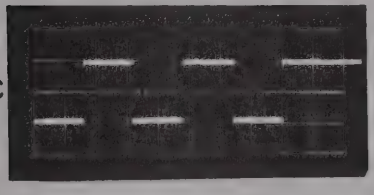
G

J1-7 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT –



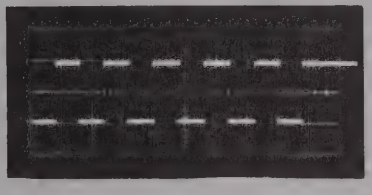
M

A8-9 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 10
SYNC: INT +



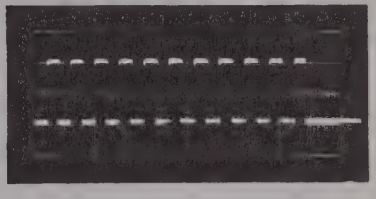
C

J1-3 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



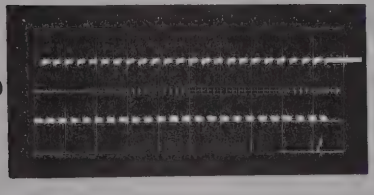
H

J1-8 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



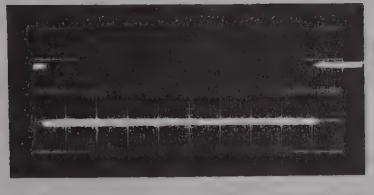
N

A14-12 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



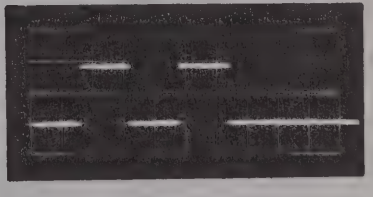
D

J1-4 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



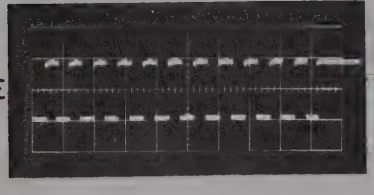
J

PIN 12 (NOTE 1) V/CM: 2
SWEEP DELAY: 443 USEC USEC/CM: 20
SYNC: EXT + (1J1)



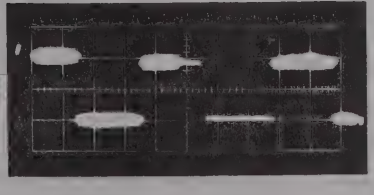
P

A15-12 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



E

J1-5 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: INT +



K

A4-9 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 10
SYNC: INT +

NOTE :

1. AT CONTROL BOX, ENABLE TEST TARGET MODE BY HOLDING CHALLENGE SWITCH AT TEST.

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Figure 20-2. Test target generator card 1A2A1A3 waveforms.

Section V. TARGET VIDEO CARD 1A2A1A4 TROUBLESHOOTING AND REPAIR

20-26. General

This section presents specific troubleshooting and testing information for target video card 1A2A1A4. For troubleshooting, paragraph 20-27 lists helpful data located in other parts of this manual, and paragraphs 20-28 and 29-29 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20-30 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-31 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-3 shows the card waveforms which are of significance in troubleshooting and testing.

20-27. Reference Data

The data listed in the following chart will be helpful when troubleshooting the target video card:

Reference	*Data*
Paras 7-7, 7-8	Target video selection and reshaping circuits functioning.
Para 7-9	Digital delay circuit functioning.
Para 7-10	Tail trigger generation circuit functioning.
Fig. 24-22	Target video card 1A2A1A4 schematic diagram.

20-28. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the target video card are the same as for overall synchronizer troubleshooting (paras 12-4 and 12-5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, install the card in an otherwise satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24-16, and proceed as directed in paragraph 12-5*c* through *i*.

20-29. Troubleshooting Chart

a. Preliminary Procedure. With the target video card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24-16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777. Make al sif replies acceptable by holding the SIF REPLIES switch at ALL.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1-3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column.

b. Target Video Card 1A2A1A4 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 35	Oscilloscope	Decoded reply video (K, fig. 20-3).	If normal, proceed with step 16. If abnormal, proceed with step 2.
2	Pin 13	Oscilloscope	Sif reply enable (same as K, fig. 20-11, except inverted).	If abnormal, inverter A14C is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
3	Pin 38	Oscilloscope	5-mc clock (same as Q, fig. 20–10).	If abnormal, inverter A12B is defective.
4	Pin 32	Oscilloscope	$\overline{\text{5-mc clock}}$ (same as Q, fig. 20–10).	If abnormal, inverter A12A is defective.
5	A7–14	Oscilloscope	High	If abnormal, inverter A7D is defective.
6	Pin 5	Oscilloscope	$\overline{\text{Sif bracket decoded video}}$ (same as Q, fig. 20–9).	If normal, proceed with step 7. If abnormal, isolate either to OR A5B or to flip-flop A1B.
7	J1–4	Oscilloscope	Final 0.2 μsec of $\overline{\text{decoded reply}}$ (A, fig. 20–3).	If abnormal, isolate to flip-flop A1 or AND A5A.
8	Pin 15	Oscilloscope	$\overline{\text{Target line input}}$ (same as Q, fig. 20–9).	If normal, proceed with step 14. If abnormal, proceed with step 9.
9	J1–1	Oscilloscope	$\overline{\text{Enabled sif correct code video}}$ (same as R, fig. 20–9).	If abnormal, A14 is defective.
10	J1–3	Oscilloscope	Target line input (same as Q, fig. 20–9, except inverted).	If normal, inverter A5D is defective. If abnormal, proceed with step 11.
11	J1–7	Oscilloscope	$\overline{\text{Enabled bracket decoded video}}$ (same as Q, fig. 20–9).	If normal, proceed with step 13. If abnormal, proceed with step 12.
12	A5–5	Oscilloscope	Sif bracket decoded video or sif correct code video (same as Q, fig. 20–9, except inverted).	If normal, AND A9A is defective. If abnormal, OR A5B is defective.
13	J1–2	Oscilloscope	$\overline{\text{Enabled mode 4 time decoded video/test target video}}$ (high).	If normal, OR A9C is defective. If abnormal, AND A13D is defective.
14	J1–9	Oscilloscope	Final 0.2 μsec of $\overline{\text{decoded reply}}$ (same as A, fig. 20–3).	If normal, proceed with step 15. If abnormal, isolate flip-flop A2 or AND A7A.
15	A6–10	Oscilloscope	Decoded reply video (same as K, fig. 20–3, except inverted).	If normal, inverter A5C is defective. If abnormal, OR A6B is defective.
16	Pin 30	Oscilloscope	Delayed target video (J, fig. 20–3).	If normal, proceed with step 26. If pulse is not present, proceed with step 17. If pulse is too short, proceed with step 21. If continuously high, proceed with step 23.
17	J2–4	Oscilloscope	Decoded reply delayed 1.6 μsec (E, fig. 20–3).	If abnormal, A3 is defective.
18	J2–6	Oscilloscope	Decoded reply delayed 3.2 μsec (G, fig. 20–3).	If abnormal, A4 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
19	J2-5	Oscilloscope	Decoded reply delayed 4.8 μsec (F, fig. 20-3).	If abnormal, A8 is defective.
20	A7-8	Oscilloscope	High	If high, A11 is defective. If not high, inverter A7C is defective.
21	J2-3	Oscilloscope	Final 0.6 μsec of delayed target video (D, fig. 20-3).	If continuously high, flip-flop A11B is defective.
22	J2-2	Oscilloscope	Friend reset enable (C, fig. 20-3).	If normal, flip-flop A10 is defective. If continuously high, flip-flop A15A is defective.
23	J1-10	Oscilloscope	Final 0.2 μsec of delayed target video (abnormal in this step).	If continuously low, proceed with step 24. If waveform goes high at any time, flip-flop A11A is defective.
24	J2-3	Oscilloscope	Final 0.6 μsec of delayed target video (abnormal in this step).	If not continuously high, flip-flop A11B is defective.
25	J2-2	Oscilloscope	Friend reset enable (C, fig. 20-3).	If abnormal, flip-flop A15A is defective. If normal, flip-flop A10 is defective.
26	Pin 22	Oscilloscope	$\overline{\text{Friend reset}}$ (H, fig. 20-3).	If abnormal, AND A7B is defective.
			STEPS 27 THROUGH 31 ARE TO BE CARRIED OUT IN TEST TARGET MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
27	Pin 40	Oscilloscope	$\overline{\text{Tail trigger}}$ (N, fig. 20-3)	If abnormal, A16 is defective.
28	Pin 7	Oscilloscope	Mode 4/test target enable (high).	If normal, proceed with step 30. If abnormal, A13 or inverter A9B is defective; proceed with step 29.
29	A9-5	Oscilloscope	$\overline{\text{Test target enable}}$ (low)	If not low, inverter A9B is defective. If low, OR A13C is defective.
30	J1-3	Oscilloscope	Test target video (same as F, fig. 20-2, except inverted).	If normal, proceed with step 32. If abnormal, proceed with step 31.
31	J1-2	Oscilloscope	$\overline{\text{Test target video}}$ (same as F, fig. 20-2).	If normal, OR A9C is defective. If abnormal, AND A13D is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
			STEP 32 IS TO BE CARRIED OUT WITH A LOW MODE 4 ENABLE INPUT FROM THE CONTROL BOX (AS FOR CHALLENGING IN MODE 4). HOWEVER, THE MODE 4 WORD GENERATOR IS NOT REQUIRED. AT CONTROL BOX, PLACE "MODE SELECT" SWITCH AT 4, AND HOLD "CHALLENGE" SWITCH AT "ON."	
32	Pin 3 ----------	Oscilloscope --------	Mode 4 enable (high) ------	If not high, A13 is defective.

20–30. Test Procedure

a. The test procedure for the target video card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the target video card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraphs 20–31. Then prepare a hot mockup as for troubleshooting (para 20–28) and perform the preliminary procedure given in para 20–29*a*), but do continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A4–3, mode 4 enable (should be low).

(2) 1A2A1A4–7, mode 4/test target enable (should be low).

(3) 1A2A1A4–8, $\overline{\text{mode 4 enable}}$ (should be high).

(4) 1A2A1A4–12, $\overline{\text{mode 4/test target enable}}$ (should be high).

(5) 1A2A1A4–22, $\overline{\text{friend reset}}$ (H, fig. 20–3).

(6) 1A2A1A4–30, delayed target video (J, fig. 20–3).

(7) 1A2A1A4–32, $\overline{\text{5-mc clock}}$ (same as Q, fig. 20–10).

(8) 1A2A1A4–35, $\overline{\text{decoded reply video}}$ (K, fig. 20–3).

c. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

d. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A1A4J1–3, test target video (same as F, fig. 20–2, except inverted).

(2) 1A2A1A4–12, $\overline{\text{mode 4/test target enable}}$ (should be low).

(3) 1A2A1A4–40, $\overline{\text{tail trigger}}$ (N, fig. 20–3).

e. At the control box, challenge in mode 4 by holding the CHALLENGE switch at ON with the MODE SELECT switch at 4.

f. At the synchronizer, check the dc level at 1A2A1A4–3. This is the mode 4 enable, which should be high.

20–31. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating target video card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20–28). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–29*a*), except that at the control box the CHALLENGE switch was left at OFF (released), and the SIF REPLIES switch was left at CODED (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Target Video Card 1A2A1A4 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	−0.65	RX10,000	400K	RX100	1850
2	0.0	RX1	0.0	RX1	0.0
3	0.14	RX10,000	450K	RX100	900
4	5.0	RX100	1500	RX100	300
5	3.6	RX10,000	500K	RX100	900
6	−0.65	RX10,000	500K	RX100	1700
7	0.12	RX10,000	400K	RX100	850
8	3.8	RX10,000	380K	RX100	850
9	0.1	RX10,000	380K	RX100	2100
10	−0.6	RX10,000	480K	RX100	1600
11	3.9	RX10,000	3 Mego	RX100	800
12	3.8	RX10,000	3 Mego	RX100	900
13	0.1	RX10,000	490K	RX100	850
14	Not used				
15	4.3	RX10,000	560K	RX100	720
16	Not used				
17	Not used				

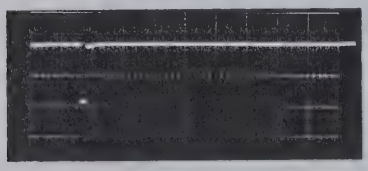
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
18	3.8	RX10,000	540K	RX100	2000
19	3.8	RX10,000	520K	RX100	1500
20	0.08	RX10,000	530K	RX100	900
21	Not used				
22	3.9	RX10,000	3 Mego	RX100	900
23	4.4	RX10,000	790K	RX100	1500
24	Not used				
25	Not used				
26	Not used				
27	Not used				
28	Not used				
29	Not used				
30	0.1	RX10,000	360K	RX100	700
31	3.9	RX10,000	540K	RX100	700
32	2.1	RX10,000	280K	RX100	600
33	2.2	RX10,000	520K	RX100	1500
34	0.2	RX10,000	410K	RX100	800
35	3.9	RX10,000	3 Mego	RX100	850
36	3.9	RX10,000	380K	RX100	1700
37	3.9	RX10,000	400K	RX100	1800
38	1.65	RX10,000	470K	RX100	800
39	3.8	RX10,000	410K	RX100	850
40	3.9	RX10,000	3 Mego	RX100	800
41	Not used				
42	5.0	RX100	1500	RX100	300
43	0.2	RX10,000	410K	RX100	850
44	0.0	RX1	0.0	RX1	0.0

20-32. Waveforms

(fig. 20-3)

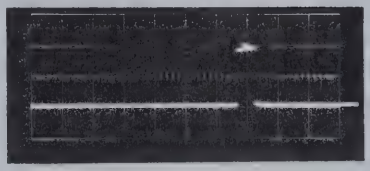
Figure 20-3 shows the Target Video card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-28 and 20-29*a*).

A



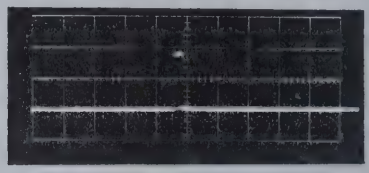
J1-4 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

D



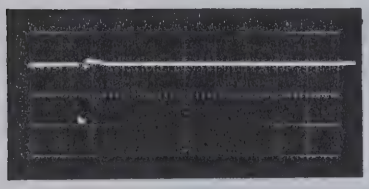
J2-3 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

G



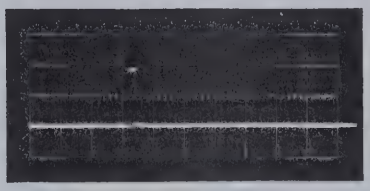
J2-6 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

B



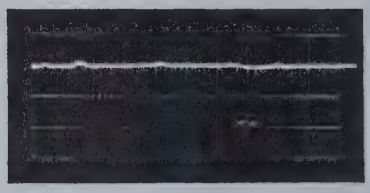
J1-5 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

E



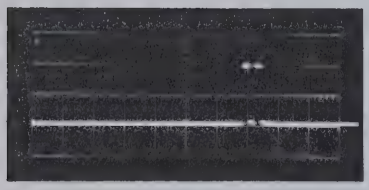
J2-4 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

H



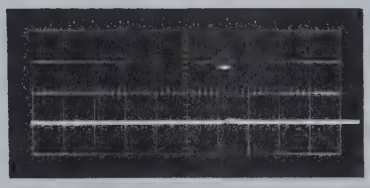
PIN 22 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

C



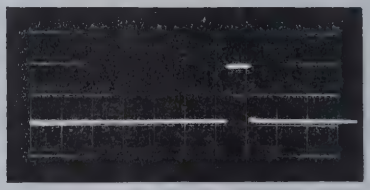
J2-2 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

F



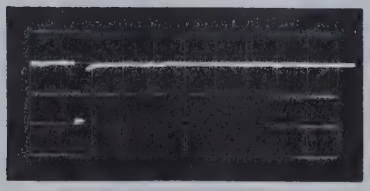
J2-5 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

J



PIN 30 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

K



PIN 35 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

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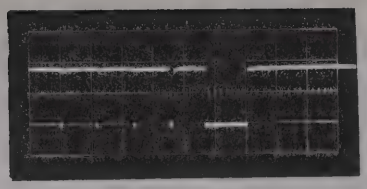
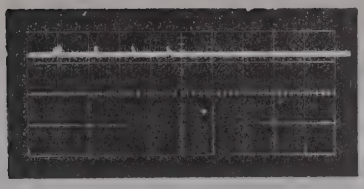
Figure 20-3①. Target video card 1A2A1A4 waveforms (sheet 1 of 2).

L



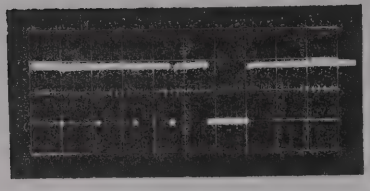
PIN 36 (NOTE 3) V/CM: 2
SWEEP DELAY: 400 USEC USEC/CM:50
SYNC: EXT + (1J1)

N



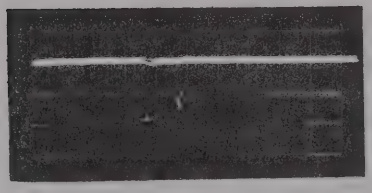
PIN 40 (NOTE 3) V/CM: 2
SWEEP DELAY: 400 USEC USEC/CM:50
SYNC: EXT + (1J1)

M



PIN 37 (NOTE 3) V/CM: 2
SWEEP DELAY: 400 USEC USEC/CM:50
SYNC: EXT + (1J1)

P



PIN 40 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, ENABLE TEST TARGET MODE BY HOLDING CHALLENGE SWITCH AT TEST.

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Figure 20-3(2). Target video card 1A2A1A4 waveforms (sheet 2 of 2).

Section VI. DISPLAY VIDEO CARD 1A2A1A5 TROUBLESHOOTING AND REPAIR

20-33. General

This section presents specific troubleshooting and testing information for display video card 1A2A1A5. For troubleshooting, paragraph 20-34 lists helpful data located in other parts of this manual, and paragraphs 20-35, 20-36, and 20-37 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20-38 references the applicable adjustment procedure, and paragraph 20-39 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-40 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-4 shows the card waveforms which are of significance in troubleshooting and testing.

20-34. Reference Data

The data listed in the following chart will be helpful when troubleshooting the display video card:

Reference	*Data*
Para 7-10	Target generation and processor bypass circuit functioning.
Para 7-11	Friend generation circuit functioning.
Para 7-12	Video reshaping circuit functioning.
Fig. 24-28	Display video card 1A2A1A5 schematic diagram.

20-35. Test Equipment Required

a. If the display video card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24-16, there is no need to change the hot mockup. However, the mode 4 word generator is not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set.

(3) Test facilities set.

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11-7.

20-36. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24-16, disregard step *b* and proceed with step *c*.

b. Interconnect the test equipment listed in paragraph 12-35*b* and the hot mockup IFF set as shown in figure 24-16, except disregard the mode 4 word generator connections shown. (The mode 4 word generator is not needed.)

c. Set the switches on the control box as directed in paragraph 12-5*c*.

d. At the interrogator group case, set the POWER circuit breaker to ON.

e. Set the controls on the radar test set as directed in paragraph 12-5*e*.

f. Set the controls on the oscilloscope as directed in paragraph 12-5*f*.

g. At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

h. Turn on the 28-volt dc power supply and adjust it for an output of 28 volts.

20-37. Troubleshooting Chart

a. Preliminary Procedure. With the display video card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24-16 or the partial hot mockup established in paragraph 20-36*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777. Make all sif replies acceptable by holding the SIF REPLIES switch to ALL.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1-3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Display Video Card 1A2A1A5 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 6 ----------	Oscilloscope --------	IFF display video (H, fig. 20-4).	If normal, proceed with step 9. If too long or too short, perform adjustment procedure for target present pulse width potentiometer R1 as described in paragraphs 16-10 and 16-12. If still abnormal, proceed with step 2.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
2	Pin 28	Oscilloscope	Target present trigger (K, fig. 20–4).	If abnormal, proceed with step 3. If normal, temporarily place control box PROCESSOR switch to BYPASS. If indication is still normal, return PROCESSOR switch to IN and proceed with step 7. If indication is now abnormal, A2 is defective.
3	J1–8	Oscilloscope	$\overline{\text{Strobed target}}$ (E, fig. 20–4)	If normal, proceed with step 4. If abnormal, check Pin 10 (same as E, fig. 20–7). If Pin 10 is abnormal, isolate to ANDs A1A, A2D, or A5A. If Pin 10 is normal, AND A1A is defective.
4	J1–7	Oscilloscope	$\overline{\text{Target reset}}$ (D, fig. 20–4)	If normal, proceed with step 5. If abnormal, AND A2D is defective.
5	J1–4	Oscilloscope	$\overline{\text{Target stored}}$ (A, fig. 20–4)	If abnormal, flip-flop A6B is defective.
6	A5–13	Oscilloscope	$\overline{\text{Target present trigger}}$ (same as K, fig. 20–4, except inverted).	If normal, OR A2A is defective. If abnormal, check Pin 39. If Pin 39 is normal (same as J, fig. 20–3), check Pin 27. If Pin 27 is normal (high), AND A5C is defective. If Pin 39 is abnormal, isolate to AND A2B, AND A5C, or single-shot A4. If Pin 27 is abnormal, isolate to AND A5C or AND A7A.
7	J1–10	Oscilloscope	Target present pulse (G, fig. 20–4).	If abnormal, single-shot stage A3 is defective.
8	A7–8	Oscilloscope	Same as step 7, except inverted.	If normal, display video amplifier stage Q1 is defective. If abnormal, inverter A7B is defective.
			STEP 9 IS TO BE CARRIED OUT IN TEST TARGET MODE. AT CONTROL BOX, HOLD ''CHALLENGE'' SWITCH AT "TEST."	
9	J1–9	Oscilloscope	Friend pulse (F, fig. 20–4)	If normal, proceed with step 14. If too long, or too short, perform adjustment procedure for friend pulse width potentiometer R3 as described in paragraphs 16–10 and 16–12. If still abnormal, proceed with step 10.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
			STEP 10 IS TO BE CARRIED OUT UNDER THE SAME CONDITIONS AS STEPS 1 THROUGH 8. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON."	
10	A2-8	Oscilloscope	Same as step 3, except inverted.	If abnormal, inverter A2C is defective. If normal, proceed with step 11.
			STEPS 11 THROUGH 15 ARE TO BE CARRIED OUT IN TEST TARGET MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
11	J1-6	Oscilloscope	$\overline{\text{Friend store}}$ (C, fig. 20-4)	If abnormal, A1 is defective.
12	J1-5	Oscilloscope	Friend clear (B, fig. 20-4)	If abnormal, A5 is defective.
13	Pin 34	Oscilloscope	Friend stored (L, fig. 20-4)	If normal, single-shot stage A4 is defective. If abnormal, flip-flop A6A is defective.
14	Pin 36	Oscilloscope	$\overline{\text{Friend stored}}$ (same as L, fig. 20-4, except inverted).	If abnormal, flip-flop A6A is defective.
15	Pin 6	Oscilloscope	IFF display video (J, fig. 20-4).	If pulse is abnormal, perform adjustment for friend pulse amplitude potentiometer R2 as described in paragraphs 16-10 and 16-12. If still abnormal, AND A7A is defective.

20-38. Adjustments

The three potentiometers on the display video card are IFF display video adjustment potentiometers. Potentiometer 1A2A1A5R1 is adjusted for a target present pulse width of 1.0 μsec. Potentiometer 1A2A1A5R2 is adjusted for a friend pulse amplitude of 5.0 volts. Potentiometer 1A2A1A5R3 is adjusted for a friend pulse width of 5.0 μsec. The adjustment procedure for all three potentiometers is given in paragraphs 16-10 and 16-12.

20-39. Test Procedure

a. The test procedure for the display video card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the display video card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-40. Then prepare a hot mockup as for troubleshooting (paras 20-35 and 20-36) and perform the preliminary procedure given in paragraph 20-37*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A5-6, IFF display video (H, fig. 20-4).

(2) 1A2A1A5-28, target present trigger (K, fig. 20-4).

c. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

d. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any order:

(1) 1A2A1A5J1-9, friend pulse (F, fig. 20-4).

(2) 1A2A1A5-6, IFF display video (J, fig. 20-4).

(3) 1A2A1A5-34, friend stored (L, fig. 20-4).

(4) 1A2A1A5-36, $\overline{\text{friend stored}}$ (same as L, fig. 20-4, except inverted).

20-40. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating display video card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-35 and 12-36). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-37*a*) except that at the control box the CHALLENGE switch was left at OFF (released), and the SIF REPLIES switch was left at CODED (released).

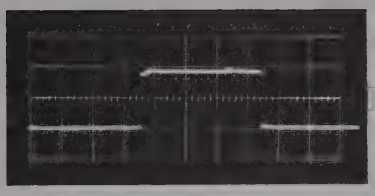
(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Display Video Card 1A2A1A5 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1200	RX100	340
4	5.0	RX100	1200	RX100	340
5	0.0	RX1	0.0	RX1	0.0
6	0.0	RX100	8000	RX100	8000
7	Not used				
8	12.5	RX10,000	3 Mego	RX100	2100
9	Not used				

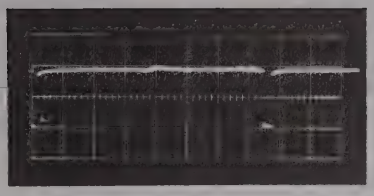
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
10	0.35	RX10,000	600K	RX100	1000
11	Not used				
12	3.9	RX10,000	590K	RX100	1100
13	Not used				
14	—0.6	RX10,000	660K	RX100	1100
15	Not used				
16	0.08	RX10,000	610K	RX100	1100
17	Not used				
18	0.2	RX10,000	580K	RX100	1100
19	Not used				
20	3.9	RX10,000	560K	RX100	1100
21	Not used				
22	5.0	RX10,000	600K	RX100	1100
23	Not used				
24	3.9	RX10,000	650K	RX100	1100
25	Not used				
26	0.1	RX10,000	580K	RX100	1030
27	3.8	RX10,000	580K	RX100	1100
28	0.13	RX100	5800	RX100	700
29	Not used				
30	3.9	RX10,000	220K	RX100	940
31	Not used				
32	Not used				
33	Not used				
34	0.13	RX100	5800	RX100	670
35	Not used				
36	4.4	RX100	5200	RX100	670
37	Not used				
38	0.12	RX10,000	800K	RX100	4800
39	0.1	RX10,000	290K	RX100	1000

A



J1-4 (NOTES 1,2) V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

D

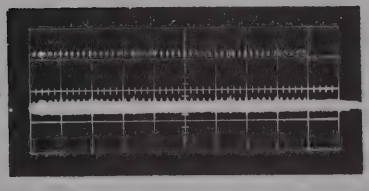


J1-7(NOTES 1,2) V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

G

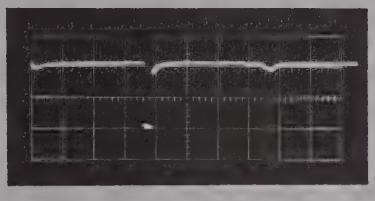
J1-10(NOTES 1,2) V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

B



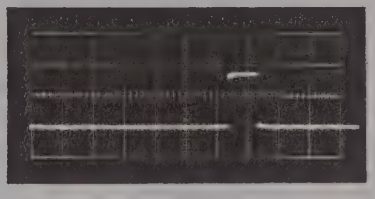
J1-5 (NOTE 3) V/CM:2
SWEEP DELAY:450 USEC USEC/CM:20
SYNC: EXT+(1J1)

E



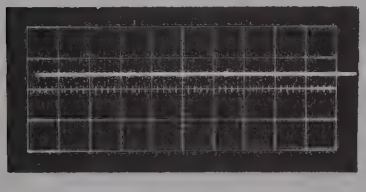
J1-8 (NOTES 1,2 V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

H



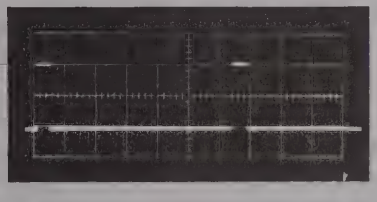
PIN 6 (NOTES 1,2) V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

C



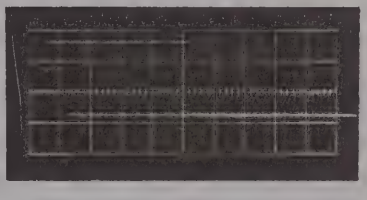
J1-6 (NOTE 3) V/CM:2
SWEEP DELAY:450USEC USEC/CM:20
SYNC: EXT+(1J1)

F



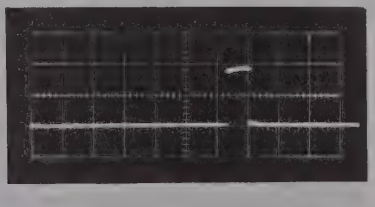
J1-9 (NOTE 3) V/CM:2
SWEEP DELAY: NONE USEC/CM:10
SYNC: INT+

J



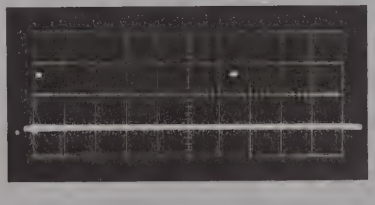
PIN 6 (NOTE 3) V/CM:2
SWEEP DELAY: NONE USEC/CM:1
SYNC: INT+

K



PIN 28 (NOTES 1,2) V/CM:2
SWEEP DELAY:520USEC USEC/CM:1
SYNC:EXT+(1J1)

L



PIN 34 (NOTE 3) V/CM:2
SWEEP DELAY: NONE USEC/CM:10
SYNC: INT+

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, ENABLE TEST TARGET MODE BY HOLDING CHALLENGE SWITCH AT TEST.

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Figure 20-4. Display video card 1A2A1A5 waveforms.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
40	Not used				
41	5.0	RX100	1200	RX100	340
42	5.0	RX100	1200	RX100	340
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–41. Waveforms

(fig. 20–4)

Figure 20–4 shows the display video card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–35, 20–36, and 20–37*a*).

Section VII. LOW LEVEL LINE DRIVER CARD 1A2A1A6 TROUBLESHOOTING AND REPAIR

20–42. General

This section presents specific troubleshooting and testing information for low level line driver card 1A2A1A6. For troubleshooting, paragraph 20–43 lists helpful data located in other parts of this manual, and paragraphs 20–44 and 20–45 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–46 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–47 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–5 shows the card waveforms which are of significance in troubleshooting and testing.

20–43. Reference Data

The data listed in the following chart will be helpful when troubleshooting the low level line driver card:

Reference	*Data*
Para 10–7 ----	Low level line driver card 1A2A1A6 functioning.
Fig. 24–24 ---	Low level line driver card 1A2A1A6 schematic diagram.

20–44. Test Equipment and Preparation

The test equipment and preparation required for troubeshooting the low level line driver card are the same as for overall synchronizer troubleshooting (paras 12–4 and 12–5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24–16, and if all initial control settings have been made as directed in paragraph 12–5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24–16, and proceed as directed in paragraph 12–5*c* through *i*.

20–45. Troubleshooting Chart

a. Preliminary Procedure. With the low level line driver card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24–16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column.

b. Low Level Line Driver Card 1A2A1A6 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 7	Oscilloscope	Buffered receiver video pulses (A, fig. 20–5).	If abnormal, line driver stage Q1 is defective.
2	Pin 13	Oscilloscope	Reshaped mode 4 pretrigger (B, fig. 20–5).	If abnormal, line driver stage Q2 is defective.
3	Pin 21	Oscilloscope	Gtc trigger (C, fig. 20–5)	If abnormal, line driver stage Q3 is defective.
4	Pin 27	Oscilloscope	Challenge video (D, fig. 20–5).	If abnormal, line driver stage Q4 is defective.
5	Pin 33	Oscilloscope	Isls gate (E, fig. 20–5)	If normal, line driver stage Q6 is defective. If abnormal, line driver stage Q5 is defective.

20–46. Test Procedure

a. The test procedure for the low level line driver card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the low level line driver card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–47. Then prepare a hot mockup as for troubleshooting (para 20–44) and perform the preliminary procedure given in paragraph 20–45*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A1A6–7, buffered receiver video (A, fig. 20–5).

(2) 1A2A1A6–13, reshaped mode 4 pretrigger (B, fig. 20–5).

(3) 1A2A1A6–21, gtc trigger (C, fig. 20–5).

(4) 1A2A1A6–27, challenge video (D, fig. 20–5).

(5) 1A2A1A6–33, isls gate (E, fig. 20–5).

c. At the control box, challenge in mode 4 by holding the CHALLENGE switch at ON with the MODE SELECT switch at 4.

d. Modify the hot mockup to simulate a mode 4 reply at a range such that the first reply pulse appears as a receiver video pulse at 1A2A2A6J1–3 within the synchronizer 470 μsec after the 0 TRIGGER (simulated radar trigger) applied to RADAR TRIG receptable 1J1 on the interrogator group case.

e. At the synchronizer, use the oscilloscope to observe the triple pulse decoded video waveform at 1A2A1A6–39 (F, fig. 20–5).

20–47. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating low level line driver card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20–44). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–45*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching of otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 1, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 1, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 1, and the negative probe was touched to each of the listed pins.

b. Low Level Line Driver Card 1A2A1A6 Etched Connector Pin Voltage and Resistance Measurements.

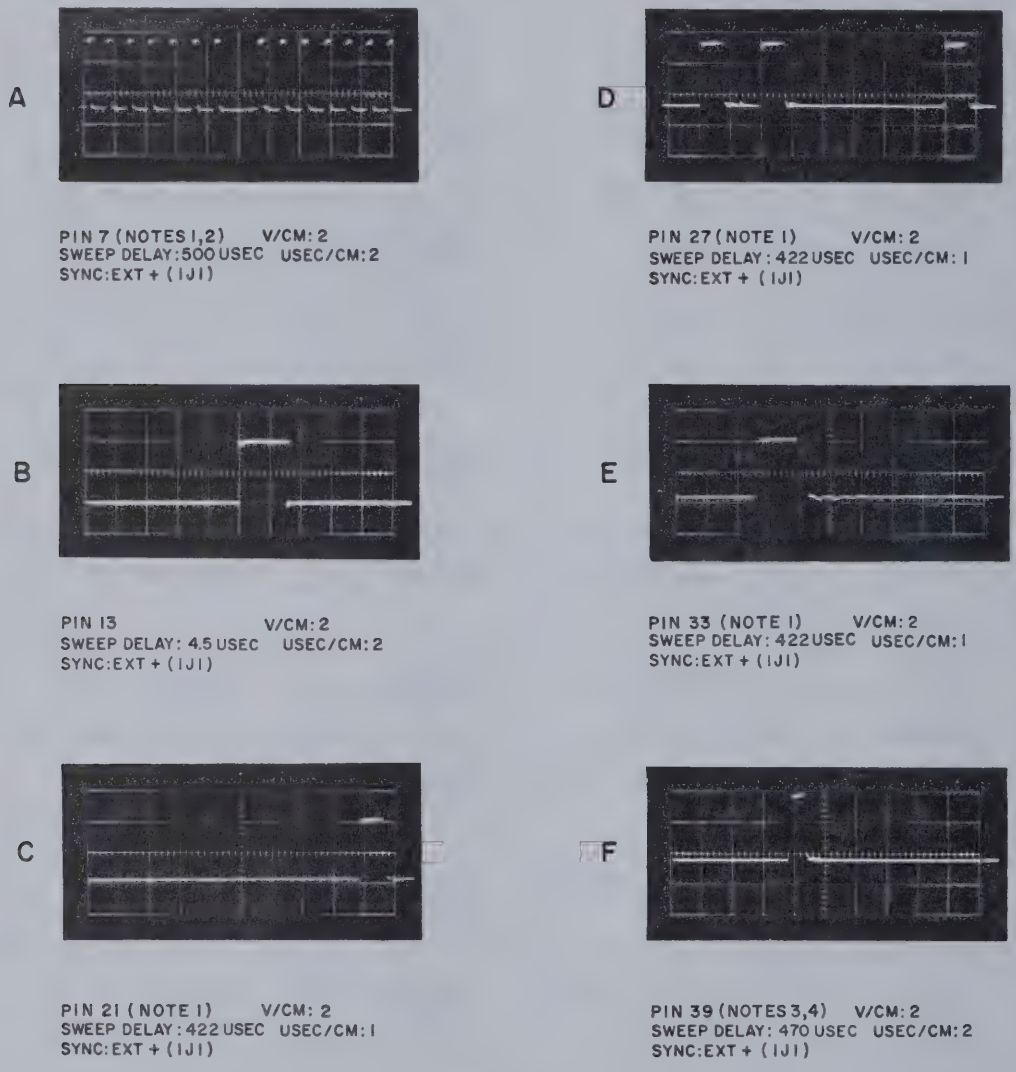
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	Not avail.				
3	5.0	RX10,000	3 Mego	RX100	9000
4	Not avail.				
5	5.2	RX10,000	4 Mego	RX100	7900
6	Not avail.				
7	0.0	RX100	7900	RX100	7500
8	Not avail.				
9	Not used				
10	Not avail.				
11	5.6	RX10,000	5 Mego	RX100	7500
12	Not avail.				
13	0.0	RX100	7900	RX100	7500
14	Not avail.				
15	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
16	Not avail.				
17	5.6	RX10,000	5 Mego	RX100	7500
18	Not avail.				
19	12.5	RX10,000	5 Mego	RX100	7000
20	Not avail.				
21	0.22	RX100	7900	RX100	7500
22	Not avail.				
23	Not used				
24	Not avail.				
25	5.7	RX10,000	5 Mego	RX100	12K
26	Not avail.				
27	0.23	RX10,000	5 Mego	RX10,000	2 Mego
28	Not avail.				
29	5.7	RX10,000	5 Mego	RX100	12K
30	Not avail.				
31	5.3	RX10,000	5 Mego	RX100	12K
32	Not avail.				
33	0.4	RX10,000	5 Mego	RX10,000	2 Mego
34	Not avail.				
35	0.0	RX10,000	5 Mego	RX10,000	2.5 Mego
36	Not avail.				
37	5.7	RX100	5 Mego	RX100	12K
38	Not avail.				
39	0.0	RX10,000	5 Mego	RX10,000	2.5 Mego
40	Not avail.				
41	5.0	RX10,000	5 Mego	RX100	13K
42	Not avail.				
43	0.0	RX10,000	5 Mego	RX10,000	5 Mego
44	Not avail.				

20-48. Waveforms

(fig. 20-5)

Figure 20-5 shows the low level line driver card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-44 and 20-45*a*).



NOTES :

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, CHALLENGE IN MODE 4 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 4.
4. MODIFY HOT MOCK-UP TO SIMULATE AN RF MODE 4 REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 517 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.

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Figure 20-5. Low level line driver card 1A2A1A6 waveforms.

Section VIII. BUFFER CIRCUIT 2 CARD 1A2A1A7 TROUBLESHOOTING AND REPAIR

20–49. General

This section presents specific troubleshooting and testing information for buffer circuit 2 card 1A2A1A7. For troubleshooting, paragraph 20–50 lists helpful data located in other parts of this manual, and paragraphs 20–51 and 20–52 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–53 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–54 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–6 shows the card waveforms which are of significance in troubleshooting and testing.

20–50. Reference Data

The data listed in the following chart will be helpful when troubleshooting the buffer circuit 2 card:

Reference	*Data*
Para 10–8 ----	Buffer circuit 2 card 1A2A1A7 functioning.
Fig. 24–25 ---	Buffer circuit 2 card 1A2A1A7 schematic diagram.

20–51. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the buffer circuit 2 card are the same as for overall synchronizer troubleshooting (paras 12–4 and 12–5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24–16, and if all initial control settings have been made as directed in paragraph 12–5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24–16, and proceed as directed in paragraph 12–5*c* through *i*.

20–52. Troubleshooting Chart

a. Preliminary Procedure. With the buffer circuit 2 card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24–16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the folowing chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Buffer Circuit 2 Card 1A2A1A7 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	J2 ----------	Oscilloscope --------	Reshaped radar trigger (B, fig. 20–6).	If normal, proceed with step 4. If abnormal, perform steps 2 and 3.
2	J1 ----------	Oscilloscope --------	Radar trigger (A, fig. 20–6) --	If abnormal, inverter A5B or amplitude limiter circuit (CR1, CR2) is defective.
3	A5–1 ----------	Oscilloscope --------	Reshaped radar trigger (same as B, fig. 20–6, except inverted).	If normal, inverter A5A is defective. If abnormal, single-shot stage A1 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
4	J3	Oscilloscope	$\overline{\text{Reshaped mode 4 pretrigger}}$ (C, fig. 20–6).	If normal, proceed to step 7. If abnormal, perform steps 5 and 6.
5	A5–14	Oscilloscope	$\overline{\text{Mode 4 pretrigger}}$ (same as K, fig. 20–18).	If abnormal, A5 or A3A is defective. Observe waveform at Pin 24 (same as K, fig. 20–18). If normal at Pin 24, A5 is defective. If abnormal at Pin 24, isolate to A5C or A3A.
6	A3–6	Oscilloscope	Reshaped mode 4 pretrigger (same as C, fig. 20–6, except inverted).	If normal, inverter A3B is defective. If abnormal, single-shot stage A2 is defective.
7	Pin 28	Oscilloscope	Mode 4 pretrigger (same as K, fig. 20–18, except inverted).	If abnormal, inverter A3A is defective.
8	Pin 8	Oscilloscope	$\overline{\text{Self test pretrigger}}$ (same as M, fig. 20–19).	If abnormal, A4 or resistor R5 is defective.
9	Pin 12	Oscilloscope	$\overline{\text{Processor start pretrigger}}$ (same as J, fig. 20–18).	If abnormal, A4 or resistor R6 is defective.
			STEPS 10 AND 11 ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 4. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON" WITH "MODE SELECT" SWITCH AT "4."	
10	Pin 40	Oscilloscope	Mode 4 challenge video (same as G, fig. 20–11).	If abnormal, amplitude limiter circuit CR5, CR6 is defective.
11	Pin 38	Oscilloscope	Mode 4 gtc trigger (same as N, fig. 20–11, except inverted).	If abnormal, amplitude limiter circuit CR3, CR4 is defective.

20–53. Test Procedure

a. The test procedure for the buffer circuit 2 card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the buffer circuit 2 card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–54. Then prepare a hot mockup as for troubleshooting (para 20–51) and perform the preliminary procedure given in paragraph 20–52*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A1A7J2, reshaped radar trigger (B, fig. 20–6).

(2) 1A2A1A7J3, $\overline{\text{reshaped mode 4 pretrigger}}$ (C, fig. 20–6).

(3) 1A2A1A7–8, self-test pretrigger (same as M, fig. 20–19).

(4) 1A2A1A7–12, processor start pretrigger (same as J, fig. 20–18).

(5) 1A2A1A7–28, mode 4 pretrigger (same as K, fig. 20–18, except inverted).

c. At the control box, challenge in mode 4 by holding the CHALLENGE switch at ON with the MODE SELECT switch at 4.

d. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A7–38, mode 4 gtc trigger (same as N, fig. 20–11, except inverted).

(2) 1A2A1A7–40, mode 4 challenge video (same as G, fig. 20–11).

20–54. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating buffer circuit 2 card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20–51). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–52*a*).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Buffer Circuit 2 Card 1A2A1A7 Etched Connector Pin Voltage and Resistance Measurements.

			Resistance in ohms		
Pin No.	Voltage (volts)	Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1850	RX100	450
4	5.0	RX100	1850	RX100	450
5	5.0	RX10,000	830K	RX100	1700
6	0.14	RX10,000	830K	RX100	800
7	Not used				
8	3.9	RX10,000	3 Mego	RX100	880
9	5.0	RX10,000	850K	RX100	1720
10	0.1	RX10,000	830K	RX100	780

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
11	Not used				
12	3.9	RX10,000	4 Mego		
13	0.0	RX1	0.0		
14	0.0	RX1	0.0		
15	0.0	RX1	0.0		
16	0.0	RX1	0.0		
17	0.0	RX1	0.0		
18	0.1	RX10,000	4 Mego		
19	0.0	RX1	0.0		
20	0.0	RX1	0.0		
21	Not used				
22	—12.0	RX100	570		
23	Not used				
24	5.0	RX10,000	750K	RX100	1410
25	Not used				
26	Not used				
27	Not used				
28	0.1	RX100	2060	RX100	680
29	Not used				
30	5.6	RX10,000	460K	RX100	780
31	0.0	RX1	0.0	RX1	0.0
32	—0.4	RX1	60	RX1	14
33	Not used				
34	—0.5	RX1	70	RX1	14
35	Not used				
36	—0.45	RX1	70	RX1	12.6
37	Not used				
38	0.15	RX100	840	RX10,000	3 Mego
39	Not used				
40	0.13	RX100	840	RX10,000	3 Mego

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
41	5.0	RX100	1850	RX100	450
42	5.0	RX100	1850	RX100	450
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20-55. Waveforms (fig. 20-6)

Figure 20-6 shows the buffer circuit 2 card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (para. 20-51 and 20-52 *a*).

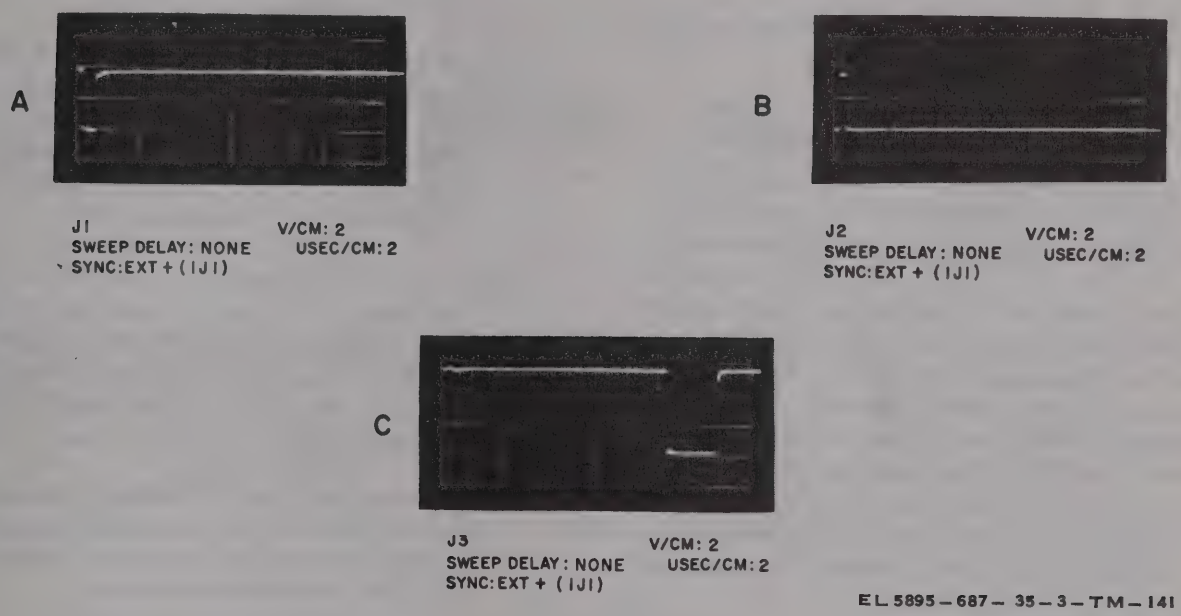


Figure 20-6. Buffer circuit 2 card 1A2A1A7 waveforms.

Section IX. BUFFER CIRCUIT 1 CARD 1A2A1A8 TROUBLESHOOTING AND REPAIR

20-56. General

This section presents specific troubleshooting and testing information for buffer circuit 1 card 1A2A1A8. For troubleshooting, paragraph 20-57 lists helpful data located in other parts of this manual, and paragraphs 20-58 and 20-59 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20-60 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-61 provides a list of typical voltage and resistance measurements at the etched

connector pins, and figure 20–7 shows the card waveforms which are of significance in troubleshooting and testing.

20–57. Reference Data

The data listed in the following chart will be helpful when troubleshooting the buffer circuit 1 card:

Reference	*Data*
Para 10–9 ----	Buffer circuit 1 card 1A2A1A8 functioning.
Fig. 24–26 ---	Buffer circuit 1 card 1A2A1A8 schematic diagram.

20–58. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the buffer circuit 1 card are the same as for overall synchronizer troubleshooting (paras 12–4 and 12–5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24–16, and if all initial control settings have been made as directed in paragraph 12–5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24–16, and proceed as directed in paragraphs 12–5*c* through *i*.

20–59. Troubleshooting Chart

a. Preliminary Procedure. With the buffer circuit 1 card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24–16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Buffer Circuit 1 Card 1A2A1A8 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 27 ----------	Oscilloscope -------	Target gated ----------	If abnormal, observe target pulse at J1–9 (B, fig. 20–7). If J1–9 is normal, A6 is defective. If J1–9 is abnormal, inverter A7B is defective.
2	Pin 40 ----------	Oscilloscope -------	Strobe (E, fig. 20–7) -------	If abnormal, inverter A7C is defective.
3	Pin 34 ----------	Oscilloscope -------	Processor bypass enable (high).	If abnormal, inverter A7A is defective. If normal, place control box PROCESSOR switch to BYPASS. Indication should now be a low reading. If not, inverter A7A is defective. Return PROCESSOR switch to IN.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
4	Pin 9	Oscilloscope	$\overline{\text{Tail/eyelash enable}}$ (high)	If abnormal, inverter A4C or capacitor C8 is shorted.
5	SYN SELF TEST lamp on control box.	None	Not Lighted	If normal, proceed to step 18. If abnormal, perform steps 6 through 17.
6	J1–5	Oscilloscope	High	If abnormal, inverter A5B is defective.
7	Pin 22	Oscilloscope	High	If abnormal, inverter A3A or lamp driver Q1 is defective.
8	J1–8	Oscilloscope	High	If abnormal, AND A5C is defective.
9	Pin 29	Oscilloscope	High	If abnormal, inverter A3C or lamp driver Q4 is defective.
10	J1–6	Oscilloscope	High	If abnormal, AND A5D is defective.
11	Pin 23	Oscilloscope	High	If abnormal, inverter A3B or lamp driver Q3 is defective.
12	J1–7	Oscilloscope	High	If abnormal, AND A5A is defective.
13	Pin 28	Oscilloscope	High	If abnormal, inverter A3D or lamp driver Q2 is defective.
14	J1–3	Oscilloscope	Low	If abnormal, OR A2B is defective.
15	A4–14	Oscilloscope	High	If abnormal, inverter A4D is defective.
16	J1–4	Oscilloscope	High	If abnormal, single-shot stage A1 is defective.
17	A2–6	Oscilloscope	Low	If normal, relay K1 is defective. If abnormal, OR A2A is defective.
			STEPS 18 THROUGH 21 ARE TO BE CARRIED OUT IN TEST TARGET MODE. AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
18	J1–2	Oscilloscope	$\overline{\text{Spoof counter video}}$ (A, fig. 20–7).	If abnormal, inverter A4A is defective.
19	J1–1	Oscilloscope	High	If abnormal, OR A4B is defective.
20	J1–10	Oscilloscope	High	If abnormal, video amplifier stage Q5 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
21	PIN 37 ----------	Oscilloscope -------	Test target video (same as F, fig. 20-2, except inverted).	If abnormal, inverter A7D is defective. If normal, problem must be mode 4 time decoded video, hence video amplifier stage Q5 is defective or A7D is defective. Isolate to Q5 or A7D.

20-60. Test Procedure

a. The test procedure for the buffer circuit 1 card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the buffer circuit 1 card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the valves listed in paragraph 20-61. Then prepare a hot mockup as for troubleshooting (para 20-58) and perform the preliminary procedure given in paragraph 20-59*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A8-8, $\overline{\text{error reset}}$ (should be high).

(2) 1A2A1A8-9, eyelash enable (should be high).

(3) 1A2A1A8-26, $\overline{\text{processor self-test gate}}$ (same as D, fig. 20-7, except inverted).

(4) 1A2A1A8-27, target gated (C, fig. 20-7).

(5) 1A2A1A8-34, processor bypass enable (should be high when PROCESSOR switch on control box is at IN; low when PROCESSOR switch is at BYPASS. Leave PROCESSOR switch at IN.

(6) 1A2A1A8-40, strobe (E, fig. 20-7).

c. Observe the four FAULT lamps on the synchronizer front panel and the SYN SELF TEST lamp on the control box. All five lamps should be out (not lighted).

d. At the control box, release the CHALLENGE switch to OFF.

e. At the synchronizer, observe the $\overline{\text{error reset}}$ level at 1A2A1A8-8. This level should be low whenever the CHALLENGE switch is at OFF.

f. At the control box, place the IFF set in the test target mode by holding the CHALLENGE switch at TEST.

g. At the synchronizer, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A1A8-8, $\overline{\text{error reset}}$ (should be high).

(2) 1A2A1A8-13, $\overline{\text{spoof counter video}}$ (same as A, fig. 20-7).

(3) 1A2A1A8-37, mode 4 time decoded video/test target video (same as F, fig. 20-2, except inverted).

h. At the control box, challenge in mode 4 by holding the CHALLENGE switch at ON with the MODE SELECT switch at 4.

i. Modify the hot mockup to simulate a mode 4 reply at a range such that the first reply pulse appears as a receiver video pulse at 1A2A2A6J1-3 within the synchronizer 470 μsec after the 0 TRIGGER (simulated radar trigger) applied to RADAR TRIG receptacle 1J1 on the interrogator group case.

j. At the synchronizer, use the oscilloscope to observe the mode 4 time decoded video/test target video at 1A2A1A8-37 (same as F, fig. 20-5).

k. At the XTAL MARK & SYNC panel of the radar test set, turn the PRF control first clockwise, then counterclockwise, observing the RADAR TRIG FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box. Both of these lamps should light when the simulated radar trigger prf exceeds approximately 625 pps, and also when the prf is less than approximately 200 pps. Leave the PRF control fully counterclockwise until step *n* below.

l. At the synchronizer, set the POWER circuit breaker to OFF, and remove the following printed wiring cards:

(1) Interface self-test card 1A2A1A1 from interface module 1A2A1.

(2) Correct code 1 card 1A2A2A2 (or correct code 2 card 1A2A2A3) from coder-decoder module 1A2A2.

(3) 10-mc clock and counter A card 1A2A4A1 from timing module 1A2A4.

m. Set the synchronizer POWER circuit breaker to ON. The RADAR TRIG FAULT lamp on the synchronizer front panel and the SYN SELF TEST lamp on the control box should both be lighted, but the other three FAULT lamps on the synchronizer front panel should be out (not lighted).

n. Turn the PRF control on the XTAL MARK & SYNC panel of the radar test set clockwise until the RADAR TRIG FAULT lamp on the synchronizer front panel goes out. At that setting, the TIMING, CODER DECODER, and INTERFACE FAULT lamps on the synchronizer front panel should all light.

20–61. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating buffer circuit 1 card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into the hot mockup and prepared in the same way as for troubleshooting (papa 20–58). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–59*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

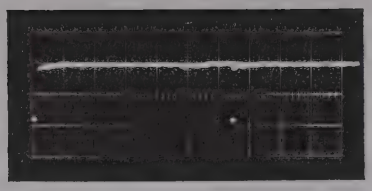
(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Buffer Circuit 1 Card 1A2A1A8 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	950	RX100	360
4	5.0	RX100	950	RX100	360
5	4.0	RX10,000	700K	RX100	1700
6	3.8	RX10,000	700K	RX100	1700
7	Not used				

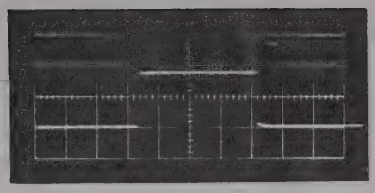
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
8	0.15	RX100	9000	RX100	850
9	0.1	RX10,000	5 Mego	RX100	790
10	0.1	RX10,000	610K	RX100	1600
11	24.8	RX1	0.2	RX1	0.2
12	5.0	RX10,000	700K	RX100	1650
13	3.8	RX10,000	5 Mego	RX100	950
14	0.1	RX10,000	700K	RX100	1850
15	3.8	RX10,000	570K	RX100	850
16	0.12	RX10,000	680K	RX100	1700
17	Not used				
18	0.12	RX10,000	680K	RX100	1900
19	Not used				
20	0.13	RX10,000	680K	RX100	1900
21	12.5	RX10,000	3 Mego	RX100	1300
22	26.0	RX10,000	3 Mego	RX100	1600
23	26.0	RX10,000	3 Mego	RX100	1500
24	3.9	RX10,000	640K	RX100	800
25	0.0	RX1	0.3	RX1	0.3
26	3.5	RX10,000	640K	RX100	800
27	0.08	RX10,000	3 Mego	RX100	800
28	26.0	RX10,000	3 Mego	RX100	1500
29	26.0	RX10,000	3 Mego	RX100	1500
30	3.5	RX10,000	630K	RX100	1600
31	0.45	RX10,000	100K	RX100	800
32	0.0	RX1	80	RX1	80
33	−0.6	RX10,000	630K	RX100	1800
34	3.8	RX10,000	3 Mego	RX100	850
35	−12.0	RX100	4100	RX100	1800
36	3.8	RX10,000	680K	RX100	1850

A



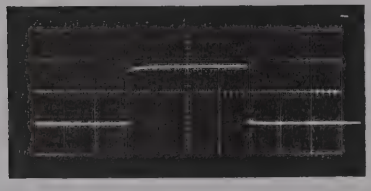
J1-2 (NOTE 3) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 10
SYNC: INT -

C



PIN 27 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

B

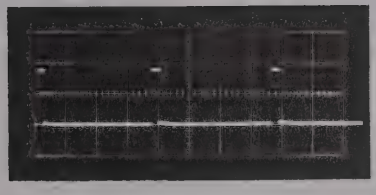


J1-9 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

D

PIN 31 (NOTE 1) V/CM: 2
SWEEP DELAY: 620 USEC USEC/CM: 50
SYNC: EXT + (1J1)

E



PIN 40 (NOTE 1) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 1
SYNC: EXT + (1J1)

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, ENABLE TEST TARGET MODE BY HOLDING CHALLENGE SWITCH AT TEST.

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Figure 20-7. Buffer circuit 1 card 1A2A1A8 waveforms.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
37	0.1	RX10,000	2 Mego	RX100	850
38	4.4	RX10,000	550K	RX100	2000
39	3.6	RX10,000	680K	RX100	2000
40	0.35	RX10,000	540K	RX100	800
41	5.0	RX100	950	RX100	3600
42	5.0	RX100	950	RX100	3600
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–62. Waveforms

(fig. 20–7)

Figure 20–7 shows the buffer circuit 1 card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–58 and 20–59*a*).

Section X. CORRECT CODE 1 CARD 1A2A2A2 TROUBLESHOOTING AND REPAIR

20–63. General

This section presents specific troubleshooting and testing information for correct code 1 card 1A2A2A2. For troubleshooting, paragraph 20–64 lists helpful data located in other parts of this manual, and paragraphs 20–65, 20–66 and 20–67 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–68 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–69 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–8 shows the card waveforms which are of significance in troubleshooting and testing.

20–64. Reference Data

The data listed in the following chart will be helpful when troubleshooting the correct code 1 card:

Reference	*Data*
Para 6–6 -----	Reply decoding circuits functioning.
Fig. 24–28 ---	Correct code 1 card 1A2A2A2 schematic diagram.

20–65. Test Equipment Required

a. If the correct code 1 card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set (only to supply "0" TRIGGER output to 1J1).

(3) Test facilities set (only for cables W32, W41, W42, and W47).

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–66. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output of 28 volts.

20–67. Troubleshooting Chart

a. Preliminary Procedure. With the correct code 1 card installed in an otherwise satisfactory synchronizer, and the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–66*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Correct Code 1 Card 1A2A2A2 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 21	Oscilloscope	Reshaped self-test $\overline{\text{pretrigger}}$ (same as S, fig. 20–14).	If abnormal, isolate to A9 or A12.
2	Pin 27	Oscilloscope	$\overline{\text{Code override}}$ (same as R, fig. 20–14).	If abnormal, isolate to A1B, A2B, A3B, A4B, A5B, A8B, A10B, or A11B.
3	Pin 23	Oscilloscope	C1 through D1 Kill (P, fig. 20–8).	If normal, proceed with step 20. If abnormal, proceed with step 4.
4	J1–2	Oscilloscope	$\overline{\text{B1 Kill}}$ (same as E, fig. 20–8, except inverted).	If normal, proceed with step 6. If abnormal, proceed with step 5.
5	Pin 30	Oscilloscope	Buffered 8.7 μsec (same as E, fig. 20–8).	If normal A11 is defective. If abnormal, OR A12B is defective.
6	J1–3	Oscilloscope	A2 Kill (same as C, fig. 20–8, except inverted).	If normal, proceed with step 8. If abnormal, proceed with step 7.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
7	Pin 13	Oscilloscope	Buffered 14.5 μsec (same as C, fig. 20-8).	If normal, A10 is defective. If abnormal, OR A9B is defective.
8	J1-4	Oscilloscope	$\overline{\text{C2 kill}}$ (same as A, fig. 20-8, except inverted).	If normal, proceed with step 10. If abnormal, proceed with step 9.
9	Pin 14	Oscilloscope	Buffered 15.95 μsec (same as A, fig. 20-8).	If normal, A1 is defective. If abnormal, OR A9C is defective.
10	J1-5	Oscilloscope	$\overline{\text{C1 kill}}$ (same as D, fig. 20-8, except inverted).	If normal, proceed with step 12. If abnormal, proceed with step 11.
11	Pin 10	Oscilloscope	Buffered 18.85 μsec (same as D, fig. 20-8).	If normal, A5 is defective. If abnormal, OR A9D is defective.
12	J1-6	Oscilloscope	$\overline{\text{A1 kill}}$ (same as B, fig. 20-8, except inverted).	If normal, proceed with step 14. If abnormal, proceed with step 13.
13	Pin 20	Oscilloscope	Buffered 17.4 μsec (same as B, fig. 20-8).	If normal, A2 is defective. If abnormal, OR A9A is defective.
14	J1-7	Oscilloscope	$\overline{\text{C4 kill}}$ (same as F, fig. 20-8, except inverted).	If normal, proceed with step 16. If abnormal, proceed with step 15.
15	Pin 38	Oscilloscope	Buffered 13.05 μsec (same as F, fig. 20-8).	If normal A8 is defective. If abnormal, OR A12D is defective.
16	J1-8	Oscilloscope	$\overline{\text{D1 kill}}$ (same as H, fig. 20-8, except inverted).	If normal, proceed with step 18. If abnormal, proceed with step 17.
17	Pin 40	Oscilloscope	Buffered 7.25 μsec (same as H, fig. 20-8).	If normal, A4 is defective. If abnormal, OR A12C is defective.
18	J1-9	Oscilloscope	$\overline{\text{A4 kill}}$ (same as G, fig. 20-8, except inverted).	If abnormal, proceed with step 19.
19	Pin 28	Oscilloscope	Buffered 11.6 μsec (same as G, fig. 20-8).	If normal, A3 is defective. If abnormal, OR A12A is defective.
			FOR STEPS 20 THROUGH 28 CHALLENGE IN MODE 3/A CODE 7777 BY HOLDING THE "CHALLENGE" SWITCH "ON" WITH THE "MODE SELECT" SWITCH AT "3/A" AND WITH THE "MODE 3/A CODE SELECT" SWITCHES AT "7777."	

Step No.	Test point	Test equipment	Normal indication	Corrective measures
20	Pin 22	Oscilloscope	C1 through D1 go (N, fig. 20–8).	If abnormal, proceed with step 21. If normal, proceed with step 29.
21	J1–1	Oscilloscope	C2 Go (A, fig. 20–8)	If abnormal, A1 is defective. If normal, proceed with step 22.
22	J1–10	Oscilloscope	A1 Go (B, fig. 20–8)	If abnormal, A2 is defective. If normal, proceed with step 23.
23	J2–1	Oscilloscope	A2 Go (C, fig. 20–8)	If abnormal, A10 is defective. If normal, proceed with step 24.
24	J2–2	Oscilloscope	C1 Go (D, fig. 20–8)	If abnormal, A5 is defective. If normal, proceed with step 25.
25	J2–3	Oscilloscope	B1 Go (E, fig. 20–8)	If abnormal, A11 is defective. If normal, proceed with step 26.
26	J2–4	Oscilloscope	C4 Go (F, fig. 20–8)	If abnormal, A8 is defective. If normal, proceed with step 27.
27	J2–5	Oscilloscope	B1 Go (G, fig. 20–8)	If abnormal, A3 is defective. If normal, proceed with step 28.
28	J2–6	Oscilloscope	D1 Go (H, fig. 20–8)	If abnormal, A4 is defective.
			FOR STEPS 29 THROUGH 36 RELEASE "CHALLENGE" SWITCH TO "OFF."	
29	J1–1	Oscilloscope	High	If abnormal, OR A1A is defective.
30	J1–10	Oscilloscope	High	If abnormal, OR A2C is defective.
31	J2–1	Oscilloscope	High	If abnormal, OR A10C is defective.
32	J2–2	Oscilloscope	High	If abnormal, OR A5A is defective.
33	J2–3	Oscilloscope	High	If abnormal, OR A11C is defective.
34	J2–4	Oscilloscope	High	If abnormal, OR A8A is defective.
35	J2–5	Oscilloscope	High	If abnormal, OR A3C is defective.
36	J2–6	Oscilloscope	High	If abnormal, OR A4A is defective.

20-68. Test Procedure

a. The test procedure for the correct code 1 card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the correct code 1 card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-69. Then prepare a hot mockup as for troubleshooting (paras 20-65 and 20-66) and perform the preliminary procedure given in paragraph 20-67*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A2A2-10, buffered 18.85 μsec (same as D, fig. 20-8).

(2) 1A2A2A2-13, buffered 14.5 μsec (same as C, fig. 20-8).

(3) 1A2A2A2-14, buffered 15.95 μsec (same as A, fig. 20-8).

(4) 1A2A2A2-20, buffered 17.4 μsec (same as B, fig. 20-8).

(5) 1A2A2A2-22, $\overline{\text{C1 through D1 go}}$ (N, fig. 20-8).

(6) 1A2A2A2-23, C1 through D1 kill (P, fig. 20-8).

(7) 1A2A2A2-28, buffered 11.6 μsec (same as G, fig. 20-8).

(8) 1A2A2A2-30, buffered 8.7 μsec (same as E, fig. 20-8).

(9) 1A2A2A2-38, buffered 13.05 μsec (same as F, fig. 20-8).

(10) 1A2A2A2-40, buffered 7.25 μsec (same as H, fig. 20-8).

20-69. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating correct code 1 card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-65 and 20-66). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-67*a*).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Correct Code 1 Card 1A2A2A2 Etched Connector Pin Voltage and Resistance Measurements.

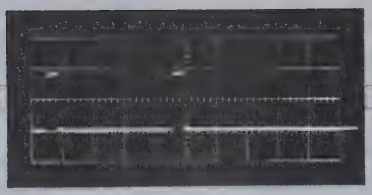
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
3	5.0	RX1	120	RX100	350
4	5.0	RX1	120	RX100	350
5	5.0	RX10,000	520K	RX100	4400
6	—0.65	RX10,000	620K	RX100	1450
7	5.0	RX10,000	480K	RX100	5500
8	—0.65	RX10,000	600K	RX100	1450
9	5.0	RX10,000	480K	RX100	5800
10	0.08	RX10,000	620K	RX100	850
11	Not used				
12	5.0	RX10,000	480K	RX100	4800
13	0.08	RX10,000	480K	RX100	860
14	0.08	RX10,000	600K	RX100	850
15	Not used				
16	—0.6	RX10,000	550K	RX100	1400
17	Not used				
18	—0.6	RX10,000	500K	RX100	1600
19	Not used				
20	0.08	RX10,000	550K	RX100	860
21	4.1	RX10,000	470K	RX100	1300
22	0.1	RX10,000	3 Mego	RX100	960
23	0.06	RX10,000	5 Mego	RX100	750
24	—0.65	RX10,000	580K	RX100	1350
25	Not used				
26	—0.65	RX10,000	570K	RX100	1400
27	4.3	RX10,000	520K	RX100	1300
28	0.1	RX10,000	560K	RX100	1000
29	Not used				
30	0.1	RX10,000	580K	RX100	1000
31	Not used				

A

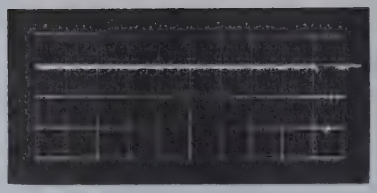
J1-1 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

E



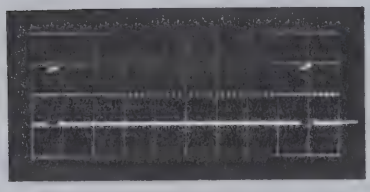
J2-3 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

J



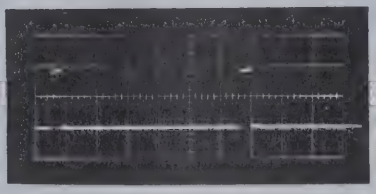
PIN 5 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

B



J1-10 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

F

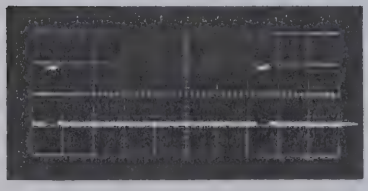


J2-4 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

K

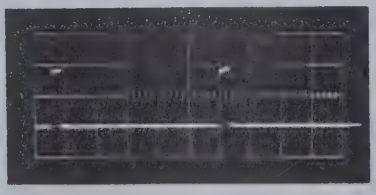
PIN 7 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

C



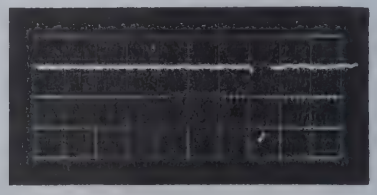
J2-1 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

G



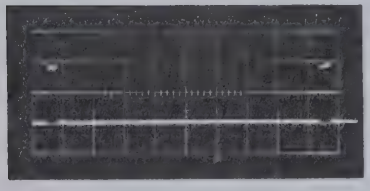
J2-5 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

L



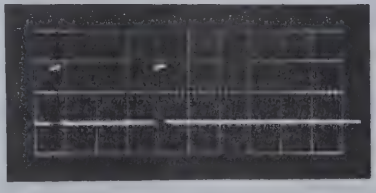
PIN 9 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

D



J2-2 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

H



J2-6 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

M

PIN 12 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

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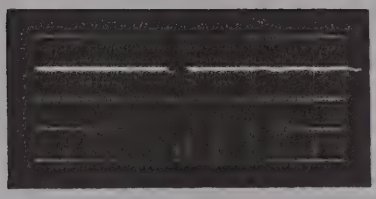
Figure 20-8①. Correct code 1 card 1A2A2A2 waveforms (sheet 1 of 2).

N

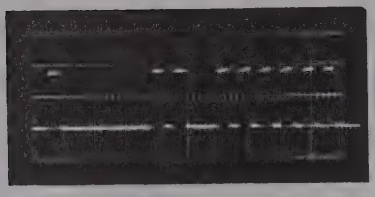
PIN 22 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

R



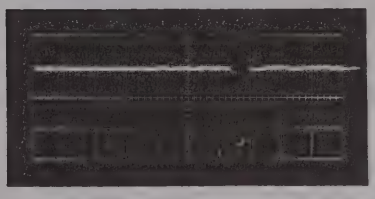
PIN 35 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

P



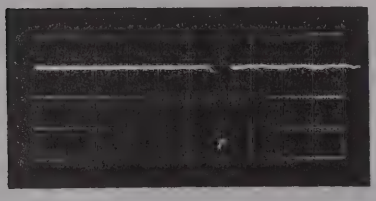
PIN 23 (NOTE 1) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

S



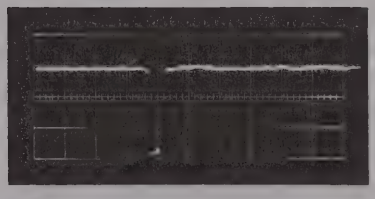
PIN 37 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

Q



PIN 32 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

T



PIN 39 V/CM: 5
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (IJI)

NOTES :

1. AT CONTROL BOX, RELEASE CHALLENGE SWITCH (TO OFF).
2. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.

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Figure 20-8②. Correct code 1 card 1A2A2A2 waveforms (sheet 2 of 2).

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
32	5.0	RX10,000	550K	RX100	7900
33	Not used				
34	−0.65	RX10,000	600K	RX100	1400
35	5.0	RX10,000	550K	RX100	7500
36	−0.6	RX10,000	500K	RX100	1500
37	5.0	RX10,000	550K	RX100	7500
38	0.1	RX10,000	600K	RX100	1000
39	5.0	RX10,000	550K	RX100	9000
40	0.1	RX10,000	500K	RX100	1000
41	5.0	RX1	120	RX100	350
42	5.0	RX1	120	RX100	350
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–70. Waveforms
(fig. 20–8)

Figure 20–8 shows the correct code 1 card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–65, 20–66, and 20–67*a*).

Section XI. CORRECT CODE 2 CARD 1A2A2A3 TROUBLESHOOTING AND REPAIR

20–71. General

This section presents specific troubleshooting and testing information for correct code 2 card 1A2A2A3. For troubleshooting, paragraph 20–72 lists helpful data located in other parts of this manual, and paragraphs 20–73, 20–74, and 20–75 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–76 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–77 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–9 shows the card waveforms which are of significance in troubleshooting and testing.

20–72. Reference Data

The data listed in the following chart will be helpful when troubleshooting the correct code 2 card:

Reference	*Data*
Par 6–6 -----	Reply decoding circuits functioning.
Para 6–9 -----	Bracket decoding circuit functioning.
Fig. 24–29 ---	Correct code 2 card 1A2A2A3 schematic diagram.

20–73. Test Equipment Required

a. If the correct code 2 card can be (or is already)

installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator is not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set.

(3) Test facilities set.

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–74. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. Interconnect the test equipment listed in paragraph 20–73 and the hot mockup IFF set as shown in figure 24–16, except disregard the mode 4 word generator connections shown. (The mode 4 word generator is not needed.)

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker to ON.

e. Set the controls on the radar test set as directed in paragraph 12–5*e*.

f. Set the controls on the oscilloscope in paragraph 12–5*f*.

g. At the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

h. Turn on the 28-volt dc power supply and adjust it for an output of 28 volts.

20–75. Troubleshooting Chart

a. Preliminary Procedure. With the correct code 2 card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–74*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge the mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column.

b. Correct Code 2 Card 1A2A2A3 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 38	Oscilloscope	$\overline{\text{Sif correct code video}}$ (R, fig. 20–9).	If normal, proceed to step 25. If abnormal, proceed with step 2.
2	E1	Oscilloscope	$\overline{\text{A11 go. No kill}}$ (A, fig. 20–9)	If normal, proceed with step 24. If abnormal, proceed with step 3.
3	E2	Oscilloscope	$\overline{\text{A11 go.}}$ (B, fig. 20–9)	If normal, proceed with step 16. If abnormal, proceed with step 4.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
4	A11-3	Oscilloscope	$\overline{\text{C1 through D1 go}}$ (same as N, fig. 20-8).	If abnormal, inverter A11A is defective.
5	Pin 16	Oscilloscope	$\overline{\text{Reshaped self-test pretrigger}}$ (same as 5, fig. 20-14).	If normal, proceed with step 6. If abnormal, isolate to A9B, A11C, A11D, or A12.
6	E3	Oscilloscope	B2 through D4 go (C, fig. 20-9).	If abnormal, proceed with step 7. If normal, observe undelayed bracket decoded video at Pin 17 (same as X, fig. 20-13 except inverted). If Pin 17 is normal, AND A5A is defective. If Pin 17 is abnormal, A9 is defective.
7	Pin 20	Oscilloscope	Buffered 1.45 μsec (same as V, fig. 20-9).	If normal, proceed with step 8. If abnormal, OR A12A is defective.
8	Pin 14	Oscilloscope	Buffered 2.9 μsec (same as Z, fig. 20-9).	If normal, proceed with step 9. If abnormal, OR A12C is defective.
9	Pin 18	Oscilloscope	Buffered 4.35 μsec (same as W, fig. 20-9).	If normal, proceed with step 10. If abnormal, OR A12D is defective.
10	Pin 19	Oscilloscope	Buffered 5.8 μsec (same as U, fig. 20-9).	If normal, proceed with step 11. If abnormal, OR A12B is defective.
11	A4-14	Oscilloscope	B2 go (U, fig. 20-9)	If abnormal, A4 is defective.
12	A7-14	Oscilloscope	D2 go (W, fig. 20-9)	If abnormal, A7 is defective.
13	A10-14	Oscilloscope	B4 go (Z, fig. 20-9)	If abnormal, A10 is defective.
14	A6-14	Oscilloscope	D4 go (V, fig. 20-9)	If abnormal, A6 is defective. If normal, proceed with step 15.
15	A8-2	Oscilloscope	$\overline{\text{B2 through D4 go}}$ (same as C, fig. 20-9, except inverted).	If normal, inverter A11B is defective. If abnormal, AND A8A is defective.
16	A13-8	Oscilloscope	10-mc clock (same as L, fig. 20-18).	If abnormal, inverter A13C is defective.
17	E4	Oscilloscope	Reshaped all go (D, fig. 20-9).	If normal, proceed with step 18. If too long or too short, flip-flop A1 or AND A5B is defective. If continuously low, flip-flop A2B or AND A5B is defective. If continuously high, observe waveform at E5 (E, fig. 20-9). If E5 is normal, flip-flop A2B or AND A5B is

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				defective. If E5 is abnormal, flip-flop is defective.
			FOR STEPS 18 THROUGH 23 RELEASE "CHALLENGE" SWITCH TO "OFF."	
18	Pin 22	Oscilloscope	$\overline{\text{C1 through D1 kill}}$ (L, fig. 20-9).	If abnormal, AND A11C is defective.
19	Pin 34	Oscilloscope	$\overline{\text{B2 through D4 kill}}$ (D, fig. 20-9).	If normal, AND A5C is defective. If abnormal, proceed with step 20.
20	A6-5	Oscilloscope	D4 kill (same as V, fig. 20-9, except inverted).	If abnormal, A6 is defective.
21	A10-5	Oscilloscope	$\overline{\text{B4 kill}}$ (same as Z, fig. 20-9, except inverted).	If abnormal, A10 is defective.
22	A7-5	Oscilloscope	$\overline{\text{D2 kill}}$ (same as W, fig. 20-9 except inverted).	If abnormal, A7 is defective.
23	A4-5	Oscilloscope	$\overline{\text{B2 kill}}$ (same as U, fig. 20-9 except inverted).	If abnormal, A4 is defective.
			PLACE "CHALLENGE" SWITCH TO "ON."	
24	Pin 39	Oscilloscope	$\overline{\text{Sif correct code pulses}}$ (same as R, fig. 20-9).	If normal, A13 is defective. If abnormal, A3 or delay line DL2 is defective.
25	Pin 17	Oscilloscope	Undelayed bracket decoded video (same as X, fig. 20-13, except inverted).	If abnormal A9 is defective.
26	Pin 35	Oscilloscope	$\overline{\text{Sif bracket decoded video}}$ (same as Q, fig. 20-9, except inverted).	If abnormal, isolate to either inverter A3A or delay line DL1.
27	Pin 36	Oscilloscope	Sif bracket decoded video (Q, fig. 20-9).	If abnormal, inverter A13D is defective.
			FOR STEPS 28 THROUGH 31, RELEASE "CHALLENGE" SWITCH TO "OFF."	
28	A4-14	Oscilloscope	B2 go (high)	If abnormal, OR A4D is defective.
29	A6-14	Oscilloscope	D4 go (high)	If abnormal, OR A6D is defective.
30	A7-14	Oscilloscope	D2 go (high)	If abnormal, OR A7D is defective.
31	A10-14	Oscilloscope	B4 go (high)	If abnormal, OR A10D is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
32	Pin 24 ----------	Oscilloscope --------	Buffered 20.3 μsec (H, fig. 20–9). STEP 33 IS TO BE CARRIED OUT WHILE CHALLENGING IN MODE 3/A AND RECEIVING A CORRECTLY CODED I/P REPLY: • AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "ON." • AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 I/P REPLY AT A RANGE SUCH THAT THE FIRST REPLY PULSE APPEARS AT 1A2A2A6J1–3 AS A RECEIVER VIDEO PULSE 500 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.	If abnormal, OR A9B is defective.
33	Pin 38 ----------	Oscilloscope --------	I/p video (S, fig. 20–9) ------	If abnormal, A13 is defective. If normal and no faults have been found, SIF correct code enable through A13B may be defective. Place an incorrect code in and Pin 38 should go high.

20–76. Test Procedure

a. The test procedure for the correct code 2 card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the correct code 2 card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–77. Then prepare a hot mockup as for troubleshooting (paras 20–73 and 20–74) and perform the preliminary procedure given in paragraph 20–75*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A3–17, undelayed bracket decoded video (same as X, fig. 20–13, except inverted).

(2) 1A2A2A3–23, sif correct code video (M, fig. 20–9).

(3) 1A2A2A3–36, $\overline{\text{sif}}$ bracket decoded video (Q, fig. 20–9).

(4) 1A2A2A3–38, $\overline{\text{sif}}$ correct code video (R, fig. 20–9).

c. At radar test set, simulate an I/p reply and observe the signal at 1A2A2A3–38, sif correct code video (S, fig. 20–9).

20-77. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the value of dc voltage and resistance that were measured at the etched connector pins of a properly operating correct code 2 card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-73 and 20-74). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-75*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

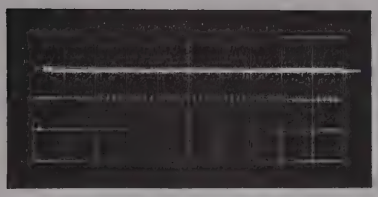
(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2 and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Correct Code 2 Card 1A2A2A3 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX1	80	RX1	12.5
4	5.0	RX1	80	RX1	12.5
5	0.1	RX100	460	RX100	460
6	5.0	RX10,000	450K	RX100	3800
7	5.0	RX10,000	450K	RX100	8000
8	5.0	RX10,000	450K	RX100	8500
9	5.0	RX10,000	450K	RX100	8500
10	5.0	RX10,000	450K	RX100	9000
11	5.0	RX10,000	450K	RX100	9500
12	4.1	RX10,000	380K	RX100	1300
13	0.12	RX10,000	360K	RX100	750
14	0.1	RX10,000	380K	RX100	750
15	0.1	RX10,000	450K	RX100	850

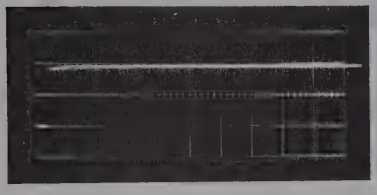
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
16	4.1	RX10,000	450K	RX100	1200
17	0.1	RX10,000	350K	RX100	800
18	—0.6	RX10,000	400K	RX100	1400
19	0.1	RX10,000	430K	RX100	800
20	0.1	RX10,000	400K	RX100	800
21	Not used				
22	3.9	RX10,000	320K	RX100	800
23	0.1	RX10,000	470K	RX100	800
24	0.13	RX10,000	450K	RX100	840
25	Not used				
26	0.06	RX10,000	520K	RX100	1700
27	Not used				
28	—0.65	RX10,000	440K	RX100	1300
29	Not used				
30	—0.6	RX10,000	400K	RX100	1700
31	Not used				
32	—0.65	RX10,000	370K	RX100	1800
33	1.37	RX100	440	RX100	440
34	3.9	RX10,000	350K	RX100	850
35	0.1	RX10,000	460K	RX100	800
36	3.6	RX100	3600	RX100	750
37	0.1	RX10,000	450K	RX100	1500
38	3.8	RX10,000	3 Mego	RX100	800
39	3.9	RX10,000	450K	RX100	750
40	3.8	RX10,000	450K	RX100	1500
41	5.0	RX1	80	RX1	12.5
42	5.0	RX1	80	RX1	12.5
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

A



E1 V/CM:2
SWEEP DELAY: 354USEC USEC/CM:2
SYNC:EXT + (IJI)

B

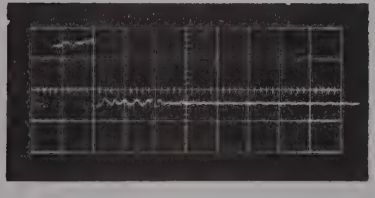


E2 V/CM:2
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

C

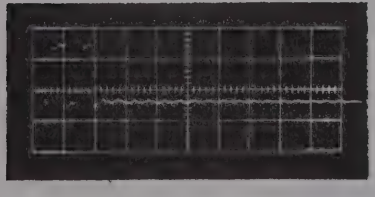
E3 (NOTE 2) V/CM:2
SWEEP DELAY: 354 USEC USEC/CM:2
SYNC:EXT + (IJI)

D



E4 V/CM:2
SWEEP DELAY:354USEC USEC/CM:0.2
SYNC:EXT + (IJI)

E

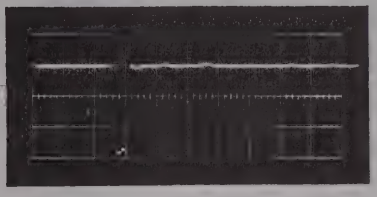


E5 V/CM:2
SWEEP DELAY:354 USEC USEC/CM:0.2
SYNC:EXT + (IJI)

F

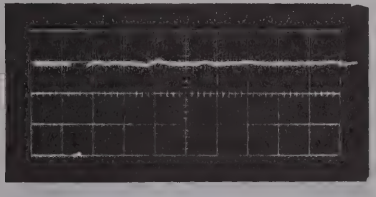
PIN 6 V/CM:5
SWEEP DELAY:356 USEC USEC/CM:2
SYNC:EXT + (IJI)

G



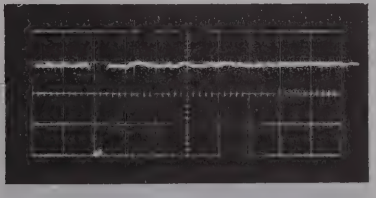
PIN 7 V/CM:5
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

H



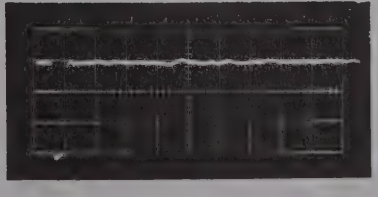
PIN 8 V/CM:5
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

J



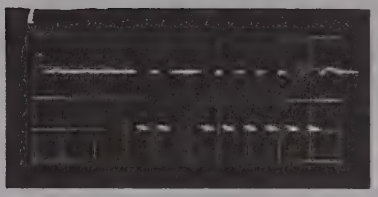
PIN 9 V/CM:5
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

K



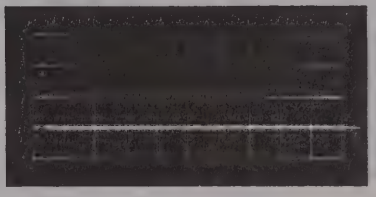
PIN 10 V/CM:5
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

L



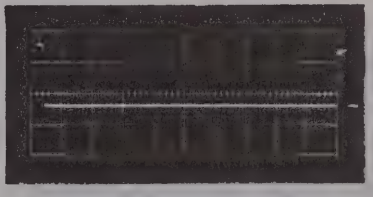
PIN 22 (NOTE 1) V/CM:2
SWEEP DELAY: 354 USEC USEC/CM:2
SYNC:EXT + (IJI)

M



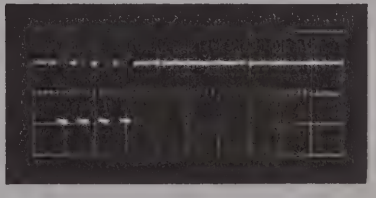
PIN 23 V/CM:2
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

N



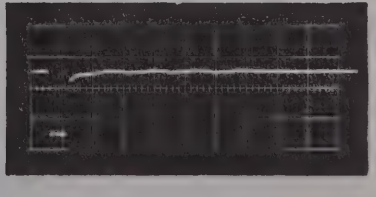
PIN 24 V/CM:2
SWEEP DELAY:354USEC USEC/CM:2
SYNC:EXT + (IJI

P



PIN 34 (NOTE 1) V/CM:2
SWEEP DELAY:354 USEC USEC/CM:2
SYNC:EXT + (IJI)

Q



PIN 36 V/CM:2
SWEEP DELAY:354 USEC USEC/CM:1
SYNC:EXT + (IJI)

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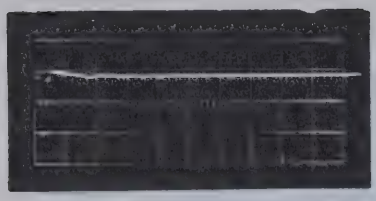
Figure 20-9①. Correct code 2 card 1A2A2A3 waveforms (sheet 1 of 2).

R



PIN 38 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

S

PIN 38 (NOTES 2,3) V/CM: 2
SWEEP DELAY: 518 USEC USEC/CM: 5
SYNC: EXT + (1J1)

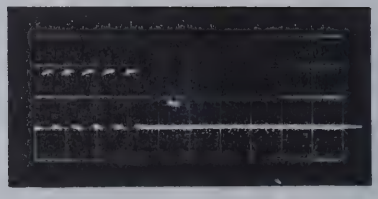
T

A1-9 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

V

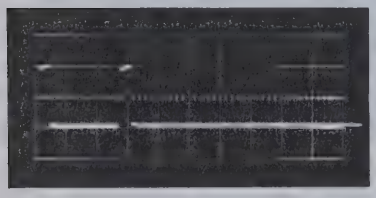
A6-14 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

X



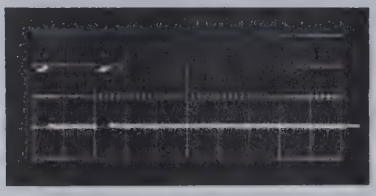
A8-10 (NOTE 1) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

U



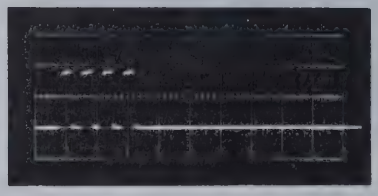
A4-14 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

W



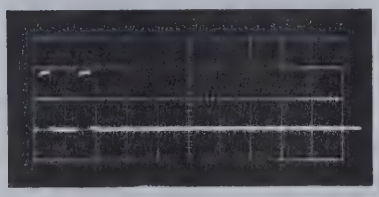
A7-14 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

Y



A8-10 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

Z



A10-14 (NOTE 2) V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 2
SYNC: EXT + (1J1)

NOTES :

1. AT CONTROL BOX, RELEASE CHALLENGE SWITCH (TO OFF).
2. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7700, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7700.
3. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 I/P REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.

EL 5895 – 687 – 35 – 3 – TM – 144 (2)

Figure 20-9(2). Correct code 2 card 1A2A2A3 waveforms (sheet 2 of 2).

20-78. Waveforms
(fig. 20-9)

Figure 20-9 shows the correct code 2 card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-74 and 20-75*a*).

Section XII. CODER CARD 1A2A2A4 TROUBLESHOOTING AND REPAIR

20-79. General

This section presents specific troubleshooting and testing information for coder card 1A2A2A4. For troubleshooting, paragraph 20-80 lists helpful data located in other parts of this manual, and paragraphs 20-81 and 20-82 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20-83 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-84 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-10 shows the card waveforms which are of significance in troubleshooting and testing.

20-80. Reference Data

The data listed in the following chart will be helpful when troubleshooting the coder card:

Reference	*Data*
Para 5-5 -----	Sif enabling circuit functioning.
Para 5-7 -----	Sif challenge/reply enabling circuits functioning.
Para 5-10 ----	Isls timing counter, isls pulse generation, isls gate generation, and 5-mc clock generation circuit functioning.
Fig. 24-30 ---	Coder card 1A2A2A4 schematic diagram.

20-81. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the coder card are the same as for overall synchronizer troubleshooting (paras 12-4 and 12-5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24-16, and proceed as directed in paragraph 12-5*c* through *i*.

20-82. Troubleshooting Chart

a. Preliminary Procedure. With the coder card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24-16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Coder Card 1A2A2A4 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 8	Oscilloscope	Mode 1 enable	With MODE SELECT switch in mode 3/A, Pin 8 should be low. If normal, switch to mode 1; Pin 8 should now be high. If either reading is abnormal, isolate to A9A or A13B.
2	Pin 7	Oscilloscope	Mode 2 enable	With MODE SELECT switch in mode 1, Pin 7 should be low. If normal, switch to mode 2; Pin 7 should now be high. If either reading is abnormal; isolate to A9B or A13A.
3	Pin 13	Oscilloscope	Mode 3/A enable	With MODE SELECT switch in mode 2; Pin 13 should be low. If normal, switch to mode 3/A; Pin 13 should now be high. If either reading is abnormal, isolate to A9C or A13C.
4	A5-5	Oscilloscope	(High)	If abnormal, AND A5B is defective.
5	Pin 12	Oscilloscope	(High) Connect code enable	If abnormal, flip-flop A4A is defective.
6	A1-10	Oscilloscope	Sif P1 trigger (mode 3/A) same as T, Fig. 20-10).	If normal, proceed with step 8. If abnormal, proceed with step 7.
7	A13-13	Oscilloscope	$\overline{\text{Mode 3 P1 trigger}}$ (same as T, fig. 20-10, except inverted).	If normal, OR A1B is defective. If abnormal, AND A13C is defective.
8	A1-10	Oscilloscope	Sif P1 trigger (mode 2) same as U, fig. 20-10).	Place MODE SELECT switch to mode 2. If normal, proceed with step 10. If abnormal, proceed with step 9.
9	A13-3	Oscilloscope	$\overline{\text{Mode 2 P1 trigger}}$ (same as U, fig. 20-10, except inverted).	If normal, OR A1B is defective. If abnormal, AND A13A is defective.
10	A1-10	Oscilloscope	Sif P1 trigger (mode 1) (same as V, fig. 20-10).	Place MODE SELECT switch to mode 1. If normal, place MODE SELECT switch to mode 3/A and proceed with step 13. If abnormal, proceed with step 11.
11	J2-8	Oscilloscope	Buffered 18.0 μsec (L, fig. 20-10).	If abnormal, inverter A12D or resistor R3 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
12	A13-5	Oscilloscope	$\overline{\text{Mode 1 P1 trigger}}$ (same as V, fig. 20-12, except inverted).	If normal, OR A1B is defective. If abnormal, AND A13B is defective.
13	J2-7	Oscilloscope	Buffered 21.0 μsec (K, fig. 20-10).	If abnormal, inverter A8A, resistor R1 or resistor R2 is defective.
14	Pin 14	Oscilloscope	Mode 2, 3/A enable	Place MODE SELECT switch to mode 1; Pin 14 should be low. Switch to mode 2 and 3/A in turn; Pin 14 should be high for modes 2 and 3/A. If abnormal, in any mode A9 is defective.
15	Pin 35	Oscilloscope	$\overline{\text{SIF enable}}$	Place MODE SELECT switch to mode 4; Pin 35 should be high. Switch to modes 1, 2, and 3/A in turn; Pin 35 should be low. If normal, proceed with step 18. If abnormal, proceed with step 16.
16	J1-2	Oscilloscope	SIF enable	Place MODE SELECT switch to mode 4; J1-2 should be low. Switch to modes 1, 2, and 3/A in turn J1-2 should be high. If normal, inverter A12A is defective. If abnormal, proceed with step 17.
17	A9-3	Oscilloscope	$\overline{\text{Mode 1 enable}}$	Place MODE SELECT switch to mode 1; A9-3 should be low. Return MODE SELECT switch to mode 3/A; A9-3 should be high. If normal, OR A5C is defective. If abnormal, inverter A9A is defective.
18	Pin 34	Oscilloscope	Isls gate (W, fig. 20-10)	MODE SELECT switch should be in mode 3/A. If normal, proceed with step 31. If abnormal, proceed with step 19.
19	Pin 32	Oscilloscope	$\overline{\text{Sif P1 trigger}}$ (same as T, fig. 20-10, except inverted).	If normal, proceed with step 21. If abnormal, proceed with step 20.
20	Pin 29	Oscilloscope	$\overline{\text{Reply enable 1}}$ (R, fig. 20-10)	If normal, AND A12B is defective. If continuously low, flip-flop A4B is defective. If continuously high, observe waveform at J2-10 (N, fig. 20-10). If J2-10 is normal, flip-flop A4B is defective. If J2-10 is abnormal, A8 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
21	J1-5	Oscilloscope	A15B-Q (A, fig. 20-10)	If normal, proceed with step 28. If abnormal, proceed with step 22.
22	J1-8	Oscilloscope	$\overline{\text{10-mc clock}}$ (same as L, fig. 20-18).	If abnormal, inverter A16C is defective.
23	A16-3	Oscilloscope	$\overline{\text{Sif P1 trigger}}$ (same as T, fig. 20-10, except inverted).	If abnormal, A16 is defective.
24	A15-13	Oscilloscope	$\overline{\text{Isls counter control}}$ (Z, fig. 20-10).	If leading edge is abnormal (it should be coincident with the leading edge of P1 trigger step 23), flip-flop A15A is defective. The trailing edge should be coincident with the trailing edge at J2-4. If A15-3 trailing edge is not coincident with the trailing edge at J2-4, A15A is defective. If there is no trailing edge at J2-4 and the leading edge of A15-13 is normal, proceed with step 25.
25	A1-2	Oscilloscope	Same as step 24	If abnormal, inverter A1A is defective.
26	J2-2	Oscilloscope	2^1 (F, fig. 20-10)	If abnormal, flip-flop A7 is defective.
27	J2-1	Oscilloscope	2^3 (E, fig. 20-10)	If normal, flip-flop A15B is defective. If abnormal, flip-flop A11 is defective.
28	J1-9	Oscilloscope	$\overline{\text{1.4 }\mu\text{sec decode}}$ (C, fig. 20-10)	If abnormal, AND A2 is defective.
29	J2-3	Oscilloscope	$\overline{\text{2.8 }\mu\text{sec decode}}$ (G, fig. 20-10)	If abnormal, AND A6 is defective.
30	J2-4	Oscilloscope	Isls gate (H, fig. 20-10)	If normal, AND A16B is defective. If abnormal, flip-flop A3A is defective.
31	Pin 5	Oscilloscope	Reply enable 1 (same as R, fig. 20-10, except inverted).	If abnormal, flip-flop A4B is defective.
32	A12-8	Oscilloscope	$\overline{\text{Isls pulse inhibit}}$ (high)	If abnormal, inverter A12 is defective.
33	J1-10	Oscilloscope	$\overline{\text{Sif P2 (isls) trigger}}$ (D, fig. 20-10).	If abnormal, AND A10 is defective. If normal, temporarily place control box MODE SELECT switch to 4 and observe $\overline{\text{mode 4 isls trigger}}$ at Pin 18 (P, fig. 20-10). If abnormal, AND A14 is defective. Return MODE SELECT switch to 3/A.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
34	A8–14	Oscilloscope	High	If abnormal, inverter A8D is defective.
35	Pin 24	Oscilloscope	5-mc clock (Q, fig. 20–10)	If abnormal, flip-flop A3B is defective.
36	Pin 26	Oscilloscope	$\overline{\text{5-mc clock}}$ (same as Q, fig. 20–10).	If abnormal, flip-flop A3B is defective.
37	J1–7	Oscilloscope	Low	If abnormal, flip-flop A4A is defective.
38	J1–3	Oscilloscope	High	If abnormal, AND A5A is defective.

20–83. Test Procedure

a. The test procedure for the coder card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the coder card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–84. Then prepare a hot mockup as for troubleshooting (para 20–81) and perform the preliminary procedure given in paragraph 20–82*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A4–14, mode 2, 3/A enable (should be high).

(2) 1A2A2A4–20, sif P2 (isls) trig. (same as D, fig. 20–10).

(3) 1A2A2A4–24, 5 mc clock (Q, fig. 20–10).

(4) 1A2A2A4–29, $\overline{\text{reply enable 1}}$ (R, fig. 20–10).

(5) 1A2A2A4–31, p1 trigger/fourth sync pulse (T, fig. 20–10).

(6) 1A2A2A4–34, $\overline{\text{isls gate}}$ (W, fig. 20–10).

(7) 1A2A2A4–35, $\overline{\text{sif enable}}$ (should be low).

(8) 1A2A2A4–36, $\overline{\text{sif p3 trigger}}$ (X, fig. 20–10).

c. At control box, challenge in mode 1 by holding CHALLENGE switch at ON with MODE SELECT switch at 1 and observe the signals at the following points:

(1) 1A2A2A4–14, mode 2, 3/A enable (should be low).

(2) 1A2A2A4–31, p1 trigger/fourth sync pulse (V, fig. 20–10).

(3) 1A2A2A4–35, sif enable (should be low).

d. At control box, challenge in mode 2 by holding CHALLENGE switch at ON with MODE SELECT switch at 2 and observe the signals at the following points:

(1) 1A2A2A4–14, mode 2, 3/A enable (should be low).

(2) 1A2A2A4–31, p1 trigger/fourth sync pulse (U, fig. 20–10).

(3) 1A2A2A4–35, $\overline{\text{sif enable}}$ (should be high).

e. At control box, challenge in mode 4 by holding CHALLENGE switch at ON with MODE SELECT switch at 4 and observe the signals at the following points:

(1) 1A2A2A4–18, $\overline{\text{mode 4 isls trig}}$ (P, fig. 20–10).

(2) 1A2A2A4–31, p1 trigger/fourth sync pulse same as J, fig. 20–11).

(3) 1A2A2A4–35, $\overline{\text{sif enable}}$ (should be high).

20–84. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating coder card.

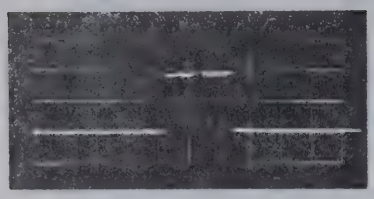
(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20–80 and 20–81). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–82*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Coder Card 1A2A2A4 Etched Connector Pin Voltage and Resistance Measurements.

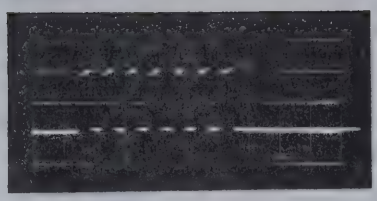
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1400	RX100	280
4	5.0	RX100	1400	RX100	280
5	3.8	RX100	3300	RX100	400
6	0.08	RX10,000	580K	RX100	1050
7	−0.6	RX10,000	550K	RX100	1000
8	−0.6	RX10,000	550K	RX100	1000
9	0.0	RX10,000	550K	RX100	1100
10	0.14	RX10,000	550K	RX100	1100
11	0.1	RX10,000	550K	RX100	1100
12	0.1	RX100	4900	RX100	600
13	−0.6	RX10,000	550K	RX100	950
14	0.08	RX100	6000	RX100	700
15	0.1	RX10,000	580K	RX100	1100
16	0.15	RX100	6000	RX100	700

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
17	4.1	RX100	6000	RX100	700
18	4.4	RX100	5800	RX100	700
19	0.14	RX10,000	720K	RX100	1050
20	4.4	RX100	5800	RX100	830
21	4.2	RX100	5500	RX100	1400
22	0.12	RX100	5800	RX100	700
23	Not used				
24	2.2	RX100	5000	RX100	660
25	0.0	RX100	2800	RX100	950
26	2.2	RX100	6000	RX100	640
27	0.12	RX100	6000	RX100	700
28	3.9	RX100	6000	RX100	1400
29	0.13	RX100	3000	RX100	400
30	5.0	RX10,000	650K	RX100	3300
31	0.13	RX100	5800	RX100	700
32	4.0	RX100	5800	RX100	700
33	4.2	RX10,000	600K	RX100	1100
34	5.3	RX100	5800	RX100	700
35	4.0	RX100	5600	RX100	700
36	4.1	RX100	5800	RX100	700
37	5.0	RX100	1700	RX100	460
38	3.9	RX10,000	620K	RX100	1000
39	1.37	RX10,000	620K	RX100	1000
40	0.11	RX100	6000	RX100	700
41	5.0	RX100	1400	RX100	280
42	5.0	RX100	1400	RX100	280
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0



A

J1-5 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)

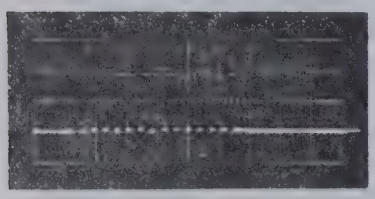


F

J2-2 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)

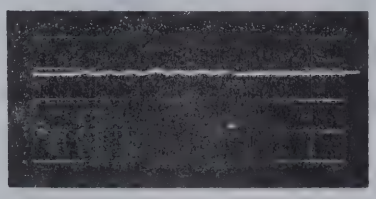
L

J2-8 V/CM: 2
SWEEP DELAY: 355 USEC USEC/CM: 2
SYNC: EXT + (IJI)



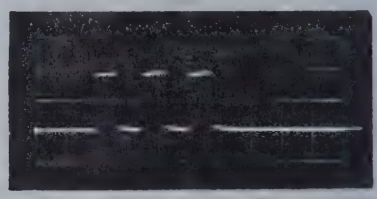
B

J1-6 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USES USEC/CM: 0.5
SYNC: EXT + (IJI)



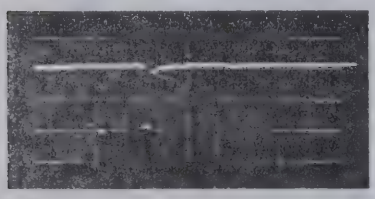
G

J2-3 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



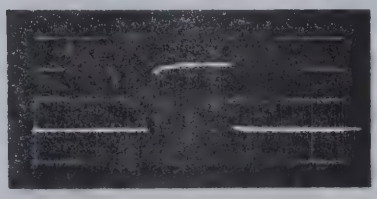
M

J2-9 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



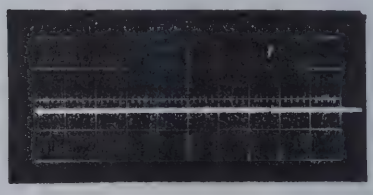
C

J1-9 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



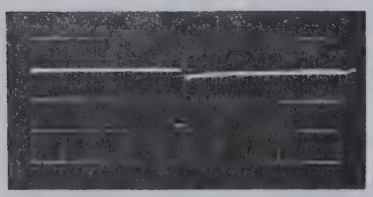
H

J2-4 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



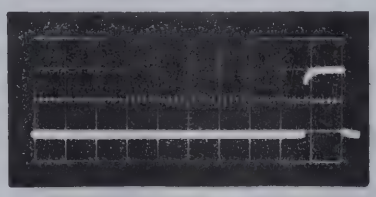
N

J2-10 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)



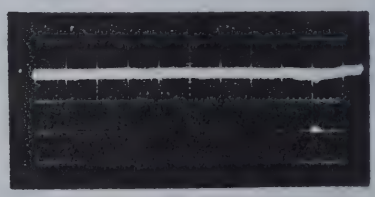
D

J1-10 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



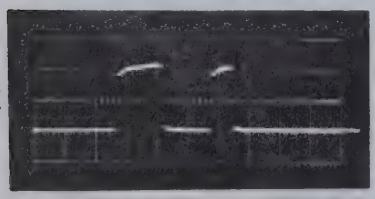
J

J2-4 (NOTE 4) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (IJI)



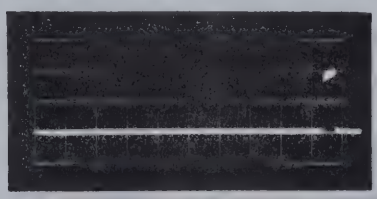
P

PIN 18 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (IJI)



E

J2-1 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



K

J2-7 V/CM: 2
SWEEP DELAY: 356 USEC USEC/CM: 2
SYNC: EXT + (IJI)

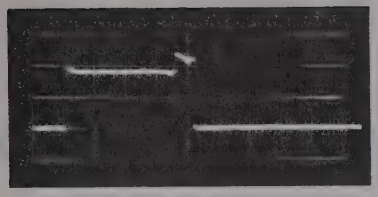
Q

PIN 24 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.1
SYNC: INT +

EL 5895-687-35-3-TM-145 ①

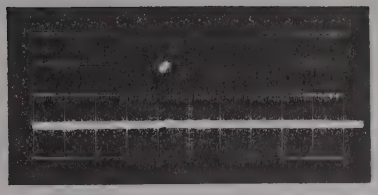
Figure 20-10①. Coder card 1A2A2A4 waveforms (sheet 1 of 2).

R



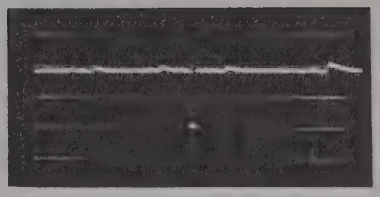
PIN 29 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

U



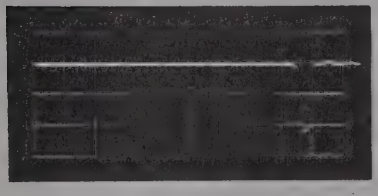
PIN 31 (NOTE 3) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

X



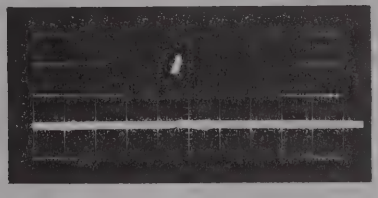
PIN 36 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

S



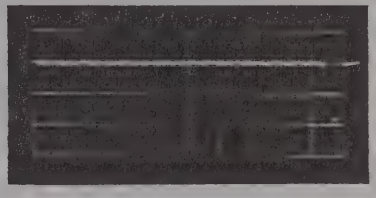
PIN 30 V/CM: 5
SWEEP DELAY: 355 USEC USEC/CM: 2
SYNC: EXT + (IJI)

V



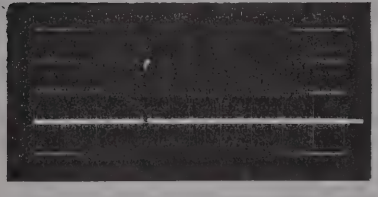
PIN 31 (NOTE 4) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

Y



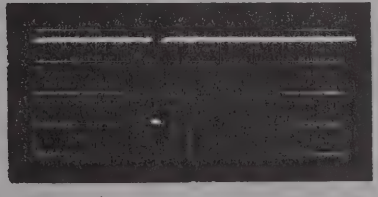
PIN 37 V/CM: 5
SWEEP DELAY: 357 USEC USEC/CM: 2
SYNC: EXT + (IJI)

T



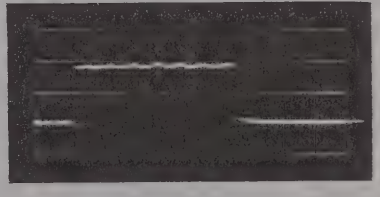
PIN 31 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

W



PIN 34 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (IJI)

Z



A15-13 (NOTE 1) V/CM: 2
SWEEP DELAY: 422 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)

NOTES :

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7700, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7700.
2. AT CONTROL BOX, CHALLENGE IN MODE 4 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 4.
3. AT CONTROL BOX, CHALLENGE IN MODE 2 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 2.
4. AT CONTROL BOX, CHALLENGE IN MODE 1 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 1.

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Figure 20–10②. Coder card 1A2A2A4 waveforms (sheet 2 of 2).

20-85. Waveforms
(fig. 20-10)

Figure 20-10 shows the coder card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-80, 20-81, and 20-82*a*).

Section XIII. CHALLENGE VIDEO CARD 1A2A2A5 TROUBLESHOOTING AND REPAIR

20-86. General

This section presents specific troubleshooting and testing information for Challenge video card 1A2A2A5. For troubleshooting, paragraph 20-87 lists helpful data located in other parts of this manual, and paragraphs 20-88 and 20-89 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20-90 references the applicable adjustment procedures, and paragraph 20-91 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-92 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-11 shows the card waveforms which are of significance in troubleshooting and testing.

20-87. Reference Data

The data listed in the following chart will be helpful when troubleshooting the challenge video card:

Reference	*Data*
Para 5-6 -----	Sif pretrigger selection, self test and sif pretrigger reshaping circuit functioning.
Para 5-12 ----	Challenge video output circuit functioning.
Para 5-11 ----	Mode 4 enabling and mode 4 sync pulse counter circuit functioning.
Fig. 24-31 ---	Challenge video card 1A2A2A5 schematic diagram.

20-88. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the challenge video card are the same as for overall synchronizer troubleshooting (paras 12-4 and 12-5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24-16, and if all initial control settings have been made as directed in paragraph 12-5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24-16, and proceed as directed in paragraph 12-5*c* through *i*.

20-89. Troubleshooting Chart

a. Preliminary Procedure. With the challenge video card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24-16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Challenge Video Card 1A2A2A5 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 27	Oscilloscope	Sif enable (high)	If abnormal. isolate to AND's A9C or A6D.
2	Pin 36	Oscilloscope	Mode 4 enable	Place MODE SELECT switch to mode 4. Pin 36 should be high. If abnormal, isolate to A7A or A13. If normal return MODE SELECT switch to mode 3/A and proceed with step 3.
3	Pin 6	Oscilloscope	Reshaped self-test and sif pretriggers (H, fig. 20–11).	If normal, proceed with step 10. If abnormal, proceed with step 4.
4	Pin 21	Oscilloscope	$\overline{\text{Self-test pretrigger}}$ (same as M, fig. 20–19).	If abnormal, inverter A6B is defective.
5	Pin 19	Oscilloscope	$\overline{\text{Sif pretrigger}}$ (same as L, fig. 20–19).	If normal, proceed with step 8. If abnormal, proceed with step 6.
6	A12–5	Oscilloscope	High	If abnormal, A12 is defective.
7	A12–3	Oscilloscope	$\overline{\text{Sif pretrigger}}$ (same as L, fig. 20–19).	If abnormal, A12 is defective. If normal, A9 is defective.
8	A9–14	Oscilloscope	$\overline{\text{Self-test and sif pretrigger}}$ (same as A, fig. 20–11, except inverted).	If normal, single shot stage A1 is defective. If abnormal, proceed with step 9.
9	A6–8	Oscilloscope	Self-test and sif pretrigger (Q, fig. 20–11).	If abnormal, OR A6C is defective. If normal, inverter A9D is defective.
10	Pin 33	Oscilloscope	$\overline{\text{Sif P1 trigger}}$ (same as T, fig. 20–10, except inverted).	If abnormal, isolate to OR's A7B or A13A.
11	J1–2	Oscilloscope	$\overline{\text{Challenge video}}$ (sif) (A, fig. 20–11).	If normal, proceed with step 20. If P1, P2 or P3 pulses are too long or too short (they should be nominally 0.77 μsec wide), perform the adjustment procedure detailed in paragraph 14–10, 11 and 12. If J1–2 is still abnormal, proceed with step 12.
12	A2–7	Oscilloscope	(High in sif)	If normal, proceed with step 16. If abnormal, proceed with step 13.
13	J1–3	Oscilloscope	(Low in sif)	If normal, proceed with step 15. If abnormal, proceed with step 14.
14	A3–9	Oscilloscope	(High in sif)	If normal, OR A3C is defective. If abnormal, AND A13B is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
15	A6-3	Oscilloscope	(High in sif)	If normal, single-shot stage A5 is defective. If abnormal, inverter A6A is defective.
16	A11-1	Oscilloscope	$\overline{\text{Reshaped P2 trigger}}$ (S, fig. 20-11).	If abnormal, single-shot stage A11 is defective. If normal, proceed with step 17.
17	A8-1	Oscilloscope	$\overline{\text{Reshaped P1+P3 triggers}}$ (R, fig. 20-11).	If normal, A2 is defective. If abnormal, proceed with step 18.
18	J1-5	Oscilloscope	Sif P1+P3 triggers (D, fig. 20—11).	If abnormal, A7 is defective. If normal, proceed with step 19.
19	A9-3	Oscilloscope	$\overline{\text{Sif P1+P3 triggers}}$ (same as D, fig. 20-11, except inverted).	If abnormal, inverter A9A is defective. If normal, single-shot stage A8 is defective.
20	Pin 40	Oscilloscope	Suppression gate (L, fig. 20-11).	If normal, proceed with step 22. If abnormal, proceed with step 21.
21	A13-3	Oscilloscope	Sif P1 trigger (same as T, fig. 20-10).	If abnormal, A13 is defective. If normal, A10 is defective.
22	Pin 43	Oscilloscope	$\overline{\text{Gtc trigger}}$ (M, fig. 20-11)	If abnormal, A7 is defective.
23	Pin 39	Oscilloscope	$\overline{\text{Mode 4 pretrigger}}$ (same as K, fig. 20-18).	If abnormal inverter A13C is defective.
			PRIOR TO PERFORMING STEPS 24 THROUGH 34, PLACE CONTROL BOX "MODE SELECT" SWITCH TO "4."	
24	Pin 16	Oscilloscope	$\overline{\text{Mode 4 fourth sync pulse}}$ (J, fig. 20-11).	If normal, proceed with step 29. If abnormal, proceed with step 25.
25	J1-6	Oscilloscope	Sync counter reset (E, fig. 20-11).	If leading edge is abnormal, proceed with step 26. The leading edge should be coincident with the leading edge of the $\overline{\text{mode 4 pretrigger}}$ (step 23). The trailing edge should be coincident with the leading edge of the $\overline{\text{ISLS gate}}$ (J1-4). If the trailing edge of J1-6 is abnormal, A3 is defective. If there is no waveform at J1-4, proceed with step 27. If the leading edge characteristics at J1-6 are normal, also proceed with step 27.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
26	A13-14	Oscilloscope	$\overline{\text{Enabled}}$ mode 4 pretrigger (same as K, fig. 20-18).	If abnormal, AND A13D is defective. If normal, A3 is defective.
27	J1-8	Oscilloscope	Enabled mode 4 challenge video (F, fig. 20-11).	If normal, flip-flop A4 or AND A2C is defective. If abnormal, proceed with step 28.
28	A13-5	Oscilloscope	$\overline{\text{Enabled}}$ mode 4 challenge $\overline{\text{video}}$ (same as F, fig. 20-11, except inverted).	If normal, inverter A3B is defective. If abnormal, AND A13B is defective.
29	Pin 14	Oscilloscope	Challenge video (mode 4) (B, fig. 20-11).	If normal, proceed with step 34. If abnormal, proceed with step 30.
30	A5-1	Oscilloscope	$\overline{\text{Reshaped}}$ mode 4 challenge $\overline{\text{video}}$ (same as B, fig. 20-11, except inverted).	If normal, OR A2B is defective. If abnormal, proceed with step 31.
31	J1-3	Oscilloscope	Mode 4 challenge video train (C, fig. 20-11).	If normal, proceed with step 33. If abnormal, proceed with step 32.
32	A13-5	Oscilloscope	$\overline{\text{Enabled}}$ mode 4 challenge $\overline{\text{video}}$ (same as F, fig. 20-11, except inverted).	If normal, AND A13B is defective. If abnormal, OR A3C is defective.
33	A6-3	Oscilloscope	Enabled mode 4 challenge video (same as F, fig. 20-11).	If normal, single-shot stage A5 is defective. If abnormal, inverter A6A is defective.
34	Pin 43	Oscilloscope	$\overline{\text{Gtc trigger}}$ (mode 4) (N, fig. 20-11).	If abnormal, A7 is defective.

20-90. Adjustments

The three potentiometers on the challenge video card are challenge video pulse width adjustment potentiometers: 1A2A2A5R1 for mode 4 challenge video pulse width, and 1A2A2A5R2 and R3 for sif challenge video pulse widths. The challenge video pulses are used as transmitter modulation (keying) pulses in the receiver-transmitter, which responds to each challenge video pulse by producing an RF challenge pulse whose width is approximately 0.03 μsec greater than the width of the challenge video pulse. Therefore, for the specified mode 4 RF challenge pulse width of 0.5 μsec, 1A2A2A5R1 is adjusted for a mode 4 challenge video pulse width of 0.47 μsec; and for the specified sif RF challenge pulse width of 0.8 μsec, 1A2A2A5R2 and R3 are adjusted for sif challenge video pulse widths of 0.77 μsec. The adjustment procedures are given in paragraphs 14-10, 14-11, and 14-12.

20-91. Test Procedure

a. The test procedure for the challenge video card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the challenge video card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-92. Then

prepare a hot mockup as for troubleshooting (para 20–88) and perform the preliminary procedure given in paragraph 20–89*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A5–6, reshaped self-test and sif pretriggers (H, fig. 20–11).

(2) 1A2A2A5–10, $\overline{\text{challenge video}}$ (same as A, fig. 20–11).

(3) 1A2A2A5–18, $\overline{\text{sif reply enable}}$ (K, fig. 20–11).

(4) 1A2A2A5–40, $\overline{\text{suppression gate}}$ (L, fig. 20–11).

(5) 1A2A2A5–43, $\overline{\text{gtc trigger}}$ (M, fig. 20–11).

c. At control box, challenge in mode 4 by holding CHALLENGE switch at ON with MODE SELECT switch at 4 and observe the signals at the following points:

(1) 1A2A2A5–10, $\overline{\text{challenge video}}$ (same as B, fig. 20–11).

(2) 1A2A2A5–16, $\overline{\text{fourth sync pulse}}$ (J, fig. 20–11).

(3) 1A2A2A5–39, $\overline{\text{mode 4 pretrigger}}$ (same as K, fig. 20–18).

(4) 1A2A2A5–43, $\overline{\text{gtc trigger}}$ (N, fig. 20–11).

20–92. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating challenge video card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20–88). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–89*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

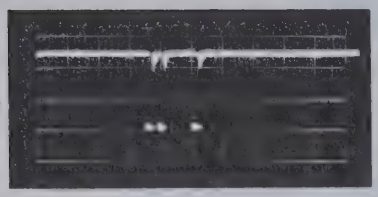
(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Challenge Video Card 1A2A2A5 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	Not used				
2	0.0	RX1	0.0	RX1	0.0
3	Not used				
4	5.0	RX100	1800	RX100	350
5	Not used				

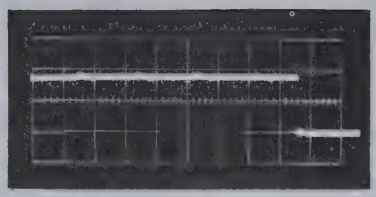
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
6	0.2	RX100	2300	RX100	600
7	Not used				
8	5.0	RX100	3600	RX100	1400
9	Not used				
10	5.7	RX10,000	5 Mego	RX100	1000
11	0.0	RX10,000	5 Mego	RX10,000	5 Mego
12	0.0	RX10,000	5 Mego	RX10,000	5 Mego
13	Not used				
14	0.13	RX10,000	700K	RX100	950
15	Not used				
16	3.9	RX10,000	5 Mego	RX100	900
17	Not used				
18	3.8	RX10,000	80K	RX100	760
19	3.9	RX10,000	270K	RX100	760
20	4.4	RX10,000	5 Mego	RX100	870
21	4.2	RX10,000	850K	RX100	800
22	3.8	RX10,000	780K	RX100	1620
23	5.1	RX10,000	780K	RX100	1600
24	0.14	RX10,000	210K	RX100	1500
25	0.0	RX10,000	780K	RX100	1600
26	5.3	RX10,000	720K	RX100	1700
27	0.15	RX10,000	600K	RX100	1500
28	4.4	RX10,000	680K	RX100	1700
29	Not used				
30	5.1	RX10,000	850K	RX100	1600
31	0.15	RX10,000	600K	RX100	1800
32	5.0	RX10,000	800K	RX100	1600
33	4.0	RX10,000	600K	RX100	1500

A



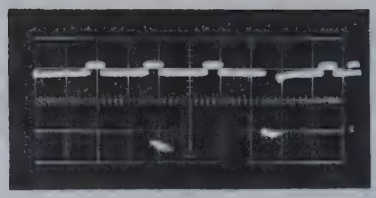
J1-2 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (1J1)

E



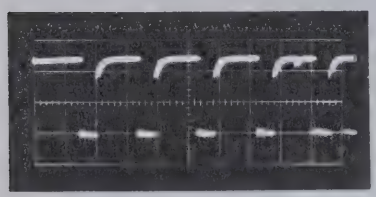
J1-6 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

J



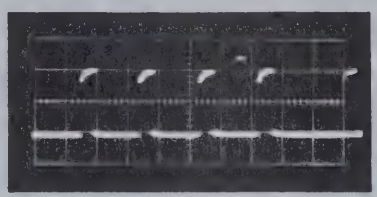
PIN 16 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

B



J1-2 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

F

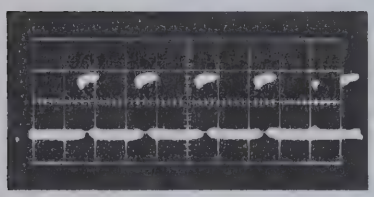


J1-8 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

K

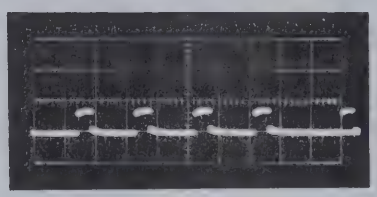
PIN 18 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (1J1)

C



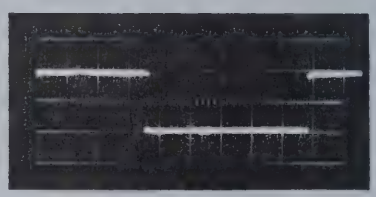
J1-3 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

G



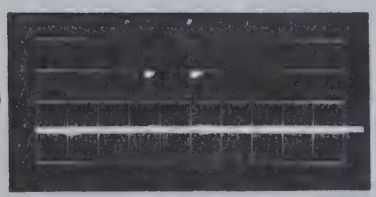
J1-9 (NOTE 2) V/CM: 2
SWEEP DELAY: 180 USEC USEC/CM: 1
SYNC: EXT + (1J1)

L



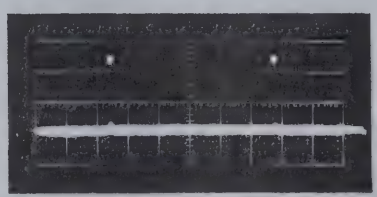
PIN 40 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (1J1)

D



J1-5 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (1J1)

H



PIN 6 (NOTE 1) V/CM: 2
SWEEP DELAY: 330 USEC USEC/CM: 10
SYNC: EXT + (1J1)

M

PIN 43 (NOTE 1) V/CM: 2
SWEEP DELAY: 405 USEC USEC/CM: 5
SYNC: EXT + (1J1)

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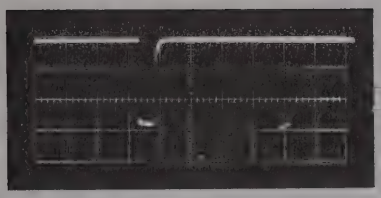
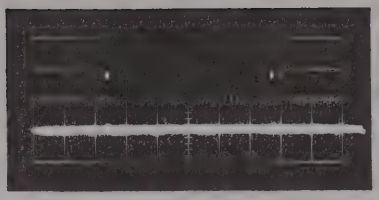
Figure 20-11①. Challenge video card 1A2A2A5 waveforms (sheet 1 of 2).

N



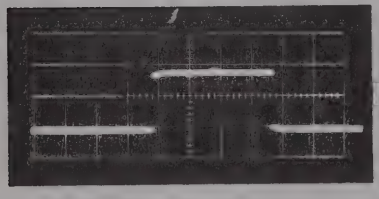
PIN 43 (NOTE 2) V/CM:2
SWEEP DELAY:380 USEC USEC/CM:5
SYNC:EXT + (IJI)

Q



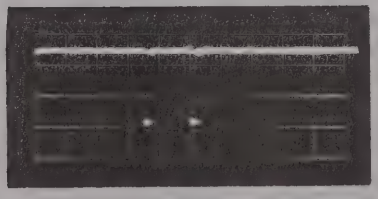
A6-8 (NOTE 1) V/CM:2
SWEEP DELAY:330 USEC USEC/CM:10
SYNC:EXT + (IJI)

P



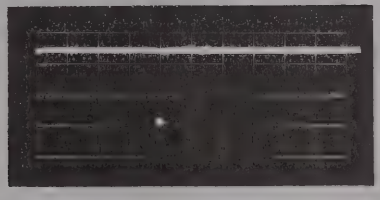
A4-12 (NOTE 2) V/CM:2
SWEEP DELAY: 180USEC USEC/CM:1
SYNC:EXT + (IJI)

R



A8-1 (NOTE 1) V/CM:2
SWEEP DELAY:405 USEC USEC/CM:5
SYNC:EXT + (IJI)

S



A11-1 (NOTE 1) V/CM:2
SWEEP DELAY:405 USEC USEC/CM:5
SYNC:EXT + (IJI)

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT CONTROL BOX, CHALLENGE IN MODE 4 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 4.

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Figure 20-11②. Challenge video card 1A2A2A5 waveforms (sheet 2 of 2).

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
34	4.1	RX10,000	600K	RX100	1500
35	0.13	RX10,000	800K	RX100	1600
36	0.14	RX10,000	600K	RX100	1400

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
37	0.1	RX10,000	680K	RX100	1800
38	0.1	RX10,000	800K	RX100	1500
39	3.9	RX10,000	500K	RX100	750
40	3.8	RX10,000	700K	RX100	750
41	Not used				
42	5.0	RX100	1800	RX100	350
43	5.6	RX10,000	3 Mego	RX100	800
44	0.0	RX1	0.0	RX1	0.0

20–93. Waveforms

(fig. 20–11)

Figure 20–11 shows the challenge video card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–88 and 20–89*a*).

Section XIV. REPLY VIDEO CARD 1A2A2A6 TROUBLESHOOTING AND REPAIR

20–94. General

This section presents specific troubleshooting and testing information for reply video card 1A2A2A6. For troubleshooting, paragraph 20–95 lists helpful data located in other parts of this manual, and paragraphs 20–96 and 20–97 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20–98 references the applicable adjustment procedure, and paragraph 20–99 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–100 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–12 shows the card waveforms which are of significance in troubleshooting and testing.

20–95. Reference Data

The data listed in the following chart will be helpful when troubleshooting the reply video card:

Reference	*Data*
Para 5–7 -----	Delayed self-test pretrigger selection and delay line time-sharing control circuit functioning.
Para 5–8 -----	Delay line input selection and delay line driver circuit functioning.
Para 6–5 -----	Video amplifier, 0.25 μsec pulse width discriminator, and receiver reshaping circuit functioning.
Para 6–8 -----	Delay line buffers, triple pulse decoding, and triple pulse decoded reshaping circuit functioning.
Fig. 24–32 ---	Reply video card 1A2A2A6 schematic diagram.

20–96. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the reply video card are the same as for overall synchronizer troubleshooting (paras 12–4 and 12–5), with the card installed in an other-

wise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24–16, and if all initial control settings have been made as directed in paragraph 12–5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24–16, and proceed as directed in paragraph 12–5*c* through *i*.

20–97. Troubleshooting Chart

a. Preliminary Procedure. With the reply video card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24–16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

(4) At the radar test set, simulate a mode 3/A code 7777 normal reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column.

b. Reply Video Card 1A2A2A6 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 18	Oscilloscope	Mode 4 enable	In mode 3/A, the normal indication is low. Place MODE SELECT switch into mode 4; Pin 18 should now be high. If either reading was abnormal, isolate to A7D or A2A. If normal, return to mode 3/A.
2	Pin 11	Oscilloscope	Reshaped self-test pretrigger (same as S, fig. 20–14).	If abnormal, isolate to A7C or A8C.
3	Pin 40	Oscilloscope	0.00 μsec (P, fig. 20–12)	If normal, proceed with step 8. If abnormal, proceed with step 4.
4	J1–2	Oscilloscope	Delay line driver input (A, fig. 20–12).	If normal, delay line driver stage Q2 is defective. If abnormal, proceed with step 5.
5	A4–10	Oscilloscope	Reply enable 2 (Q, fig. 20–12)	Leading edge should be coincident with leading edge of mode 4 pretrigger (Pin 5). If abnormal, flip-flop A4B is defective. Trailing edge should be coincident with the trailing edge of SIF P3 trigger (Pin 14). If there is a trailing edge at Pin 14 and A4–10 is abnormal,

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				flip-flop A4B is defective. If there is no trailing edge at Pin 14, or if A4–10 is normal, proceed with step 6.
6	J1–5	Oscilloscope	$\overline{\text{Buffered Receiver video}}$ high whenever A4–10 (step 5) is high.	If abnormal, AND A3B is defective.
7	A3–8	Oscilloscope	$\overline{\text{Reshaped self-test sif pretriggers}}$ (same as H, fig. 20–11).	If normal, OR A2B is defective. If abnormal, AND A3C is defective.
8	Pin 13	Oscilloscope	$\overline{\text{Delayed self-test pretrigger}}$ (same as K, fig. 20–10, except inverted).	If normal, proceed with step 11. If abnormal, proceed with step 9.
9	A4–12	Oscilloscope	$\overline{\text{Delayed self-test pretrigger enable}}$ (R, fig. 20–12).	Leading edge should be coincident with the leading edge of $\overline{\text{self-test pretrigger}}$ (Pin 16). The trailing edge should occur approximately 21 μsec later, coincident with the trailing edge of the buffered 21.0 μsec at Pin 10. If the leading edge is abnormal, flip-flop A4A is defective. If the trailing edge is defective or if the waveform is normal, proceed with step 10.
10	J1–1	Oscilloscope	$\overline{\text{Delayed self-test pretrigger}}$ (same as K, fig. 20–10, except inverted).	If abnormal, AND A6B is defective. If normal, A7 is defective.
11	A7–14	Oscilloscope	High	If abnormal, AND A7D is defective. If normal, temporarily place control box MODE SELECT switch to 4. The indication should now be the same as T, fig. 20–12. If it is not, AND A7D is defective. If normal, check that A4–9 goes high when A7–14 goes low. If A4–9 does not check, flip-flop A4A is defective. If it does check, return to Mode 3/A and proceed with step 12.
12	Pin 21	Oscilloscope	Buffered 1.8 μsec (L, fig. 20–12).	If abnormal, OR A8C is defective.
13	Pin 20	Oscilloscope	Buffered 3.6 μsec (K, fig. 20–12).	If abnormal, OR A7C is defective.
14	J1–7	Oscilloscope	Reshaped triple pulse decoded video (self-test) (F, fig. 20–12).	If normal, proceed with step 16. If abnormal, proceed with step 15.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
15	A6-13	Oscilloscope	Triple pulse decoded video (self-test) (S, fig. 20-12).	If normal, single-shot stage A1 is defective. If abnormal, AND A6C is defective.
16	Pin 22	Oscilloscope	High	If abnormal, AND A2A is defective.
17	Pin 23	Oscilloscope	Low	If abnormal, OR A8B is defective.
18	J1-5	Oscilloscope	Buffered receiver video (D, fig. 20-12).	If normal, proceed with step 23. If abnormal, proceed with step 19.
19	J1-4	Oscilloscope	Receiver video (C, fig. 20-12).	If abnormal, perform adjustment procedure for video level potentiometer R6 as described in paragraphs 15-10 and 15-11. If still abnormal, video amplifier stage Q1 is defective.
20	J1-9	Oscilloscope	Delayed receiver video (H, fig. 20-12).	If continuously low, isolate to A3 or delay line DL1. If continuously high, observe receiver video pulses at J1-6. If a train of positive-going pulses is observed at J1-6, A3 or delay line DL1 is defective. If a train of positive-going pulses is not observed at J1-6, OR A6A is defective.
21	A8-14	Oscilloscope	High	If abnormal, inverter A8D is defective.
22	J1-8	Oscilloscope	Buffered receiver video (G, fig. 20-12).	If normal, AND A3B is defective. If abnormal, single-shot stage A5 is defective.
			STEPS 23 AND 24 ARE TO BE CARRIED OUT IN TEST TARGET MODE, AT CONTROL BOX, HOLD "CHALLENGE" SWITCH AT "TEST."	
23	Pin 17	Oscilloscope	Test target video (same as F, fig. 20-2, except inverted).	If normal, proceed with step 25. If abnormal, proceed with step 24.
24	Pin 23	Oscilloscope	Test target video (same as F, fig. 20-2, except inverted).	If normal, R15 is open. If abnormal, OR A8B is defective.
			STEPS 25 AND 26 ARE TO BE CARRIED OUT WHILE CHALLENGING IN MODE 4 AND RECEIVING A SIMULATED MODE 4 REPLY. AT	

Step No.	Test point	Test equipment	Normal indication	Corrective measures
			CONTROL BOX, SET "MODE SELECT" SWITCH TO "4" AND HOLD "CHALLENGE" SWITCH AT "ON." MODIFY HOT MOCKUP TO SIMULATE A MODE 4 REPLY AT A RANGE SUCH THAT THE FIRST REPLY APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 470 μSEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.	
25	Pin 23	Oscilloscope	Triple pulse decoded video (same as M, fig. 20-12, except inverted).	If abnormal, proceed with step 26.
26	Pin 22	Oscilloscope	Triple pulse decoded video (M, fig. 20-12).	If normal, OR A8B is defective. If abnormal, AND A2A is defective.

20-98. Adjustment

The single potentiometer on the reply video card is video level adjustment potentiometer 1A2A2A6R6. This potentiometer is adjusted for a receiver video threshold amplitude of 1.5 volt. The adjustment procedure is given in paragraphs 15-10 and 15-11.

20-99. Test Procedure

a. The test procedure for the reply video card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the reply video card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-100. Then prepare a hot mockup as for troubleshooting (para 20-96) and perform the preliminary procedure given in paragraph 20-97*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A2A6J1-2, delay line driver input (same as D, fig. 20-12, except inverted).

(2) 1A2A2A6J1-7, reshaped triple pulse decoded video (F, fig. 20-12).

(3) 1A2A2A6-13, $\overline{\text{delayed self-test pretrigger}}$ (sif) (same as K, fig. 20-10, except inverted).

(4) 1A2A2A6-34, buffered receiver video (G, fig. 20-12).

(5) 1A2A2A6-40, $\overline{0.0\ \mu\text{sec}}$ (P, fig. 20-12).

c. At control box, enable test target mode by holding CHALLENGE switch at TEST and observe the signal at 1A2A2A6-17, spoof counter video (same as F, fig. 20-2, except inverted).

d. At control box, challenge in mode 4 by holding CHALLENGE switch at ON with MODE SELECT switch at 4 and observe the signal at 1A2A2A6-17, spoof counter video (same as M, fig. 20-12, except inverted).

20-100. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were

measured at the etched connector pins of a properly operating reply video card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20–96). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–97*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Reply Video Card 1A2A2A6 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	800	RX100	370
4	5.0	RX100	800	RX100	370
5	3.9	RX10,000	1.4 Mego	RX10,000	35K
6	−12.0	RX100	1350	RX100	1350
7	0.0	RX1	0.0	RX1	0.0
8	0.18	RX1	62	RX1	62
9	0.15	RX10,000	700K	RX100	1050
10	0.11	RX10,000	650K	RX100	1050
11	4.1	RX10,000	600K	RX100	1000
12	5.0	RX10,000	650K	RX100	8000
13	4.2	RX100	4500	RX100	700
14	4.1	RX10,000	1.5 Mego	RX10,000	36K
15	0.25	RX100	1400	RX100	600
16	4.2	RX10,000	1.4 Mego	RX10,000	36K
17	0.1	RX100	4600	RX100	750

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
18	0.14	RX10,000	550K	RX100	1050
19	0.1	RX10,000	600K	RX100	1050
20	0.1	RX100	4500	RX100	700
21	0.12	RX100	4500	RX100	700
22	5.7	RX10,000	650K	RX100	1050
23	0.1	RX100	4500	RX100	700
24	4.4	RX10,000	650K	RX100	1050
25	Not used				
26	5.1	RX10,000	650K	RX100	8500
27	Not used				
28	0.1	RX100	4500	RX100	700
29	Not used				
30	1.53	RX10,000	680K	RX100	1050
31	—12.0	RX100	17K	RX10,000	46K
32	1.53	RX10,000	650K	RX100	1050
33	Not used				
34	0.14	RX100	4300	RX100	800
35	Not used				
36	5.2	RX100	11K	RX10,000	36K
37	Not used				
38	0.2	RX10,000	1.5K	RX10,000	38K
39	Not used				
40	5.0	RX100	4800	RX100	5500
41	5.0	RX100	4500	RX100	4800
42	5.0	RX100	4500	RX100	4800
43	0.0	RX100	1880	RX100	20K
44	0.0	RX100	1880	RX100	20K

20-101. Waveforms
(fig. 20-12)

Figure 20-12 shows the reply video card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-96 and 20-97*a*).

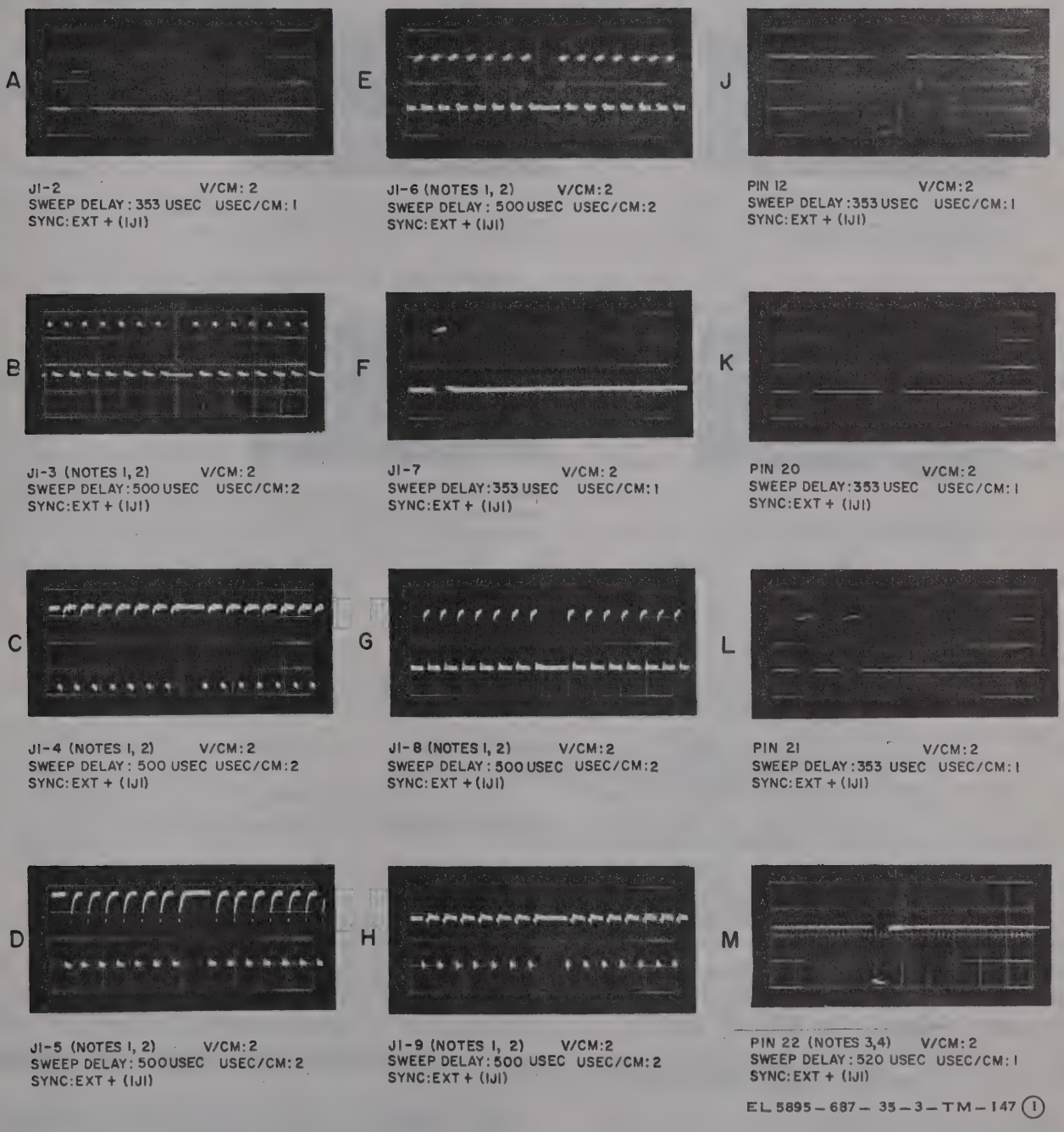
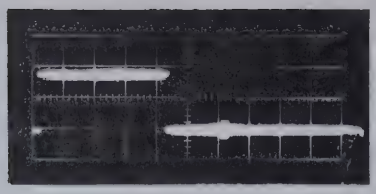


Figure 20-12①. Reply video card 1A2A2A6 waveforms (sheet 1 of 2).

N

PIN 26 V/CM: 2
SWEEP DELAY: 353 USEC USEC/CM: 1
SYNC: EXT + (1J1)

Q

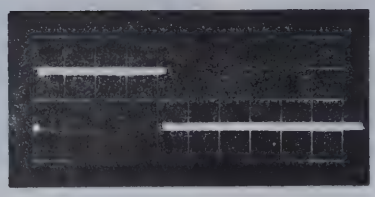


A4-10 (NOTES 1, 2) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 100
SYNC: EXT + (1J1)

P

PIN 40 V/CM: 2
SWEEP DELAY: 353 USEC USEC/CM: 1
SYNC: EXT + (1J1)

R

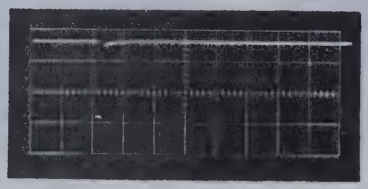


A4-12 V/CM: 2
SWEEP DELAY: 353 USEC USEC/CM: 5
SYNC: EXT + (1J1)

S

A6-13 V/CM: 2
SWEEP DELAY: 353 USEC USEC/CM: 1
SYNC: EXT + (1J1)

T



A7-14 (NOTE 3) V/CM: 2
SWEEP DELAY: 374 USEC USEC/CM: 0.5
SYNC: EXT + (1J1)

NOTES :

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 NORMAL REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, CHALLENGE IN MODE 4 BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 4.
4. MODIFY HOT MOCK-UP TO SIMULATE AN RF MODE 4 REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 517 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.

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Figure 20-12(2). Reply video card 1A2A2A6 waveforms (sheet 2 of 2).

Section XV. I/p AND EMERGENCY CODE CARD 1A2A2A7 TROUBLESHOOTING AND REPAIR

20-102. General

This section presents specific troubleshooting and testing information for i/p and emergency code card 1A2A2A7. For troubleshooting, paragraph 20-103 lists helpful data located in other parts of this manual, and paragraphs 20-104, 20-105, and 20-106 provide a troubleshooting procedure which

isolates any trouble to a stage or part. For testing after repair, paragraph 20–107 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–108 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–13 shows the card waveforms which are of significance in troubleshooting and testing.

20–103. Reference Data

The data listed in the following chart will be helpful when troubleshooting the i/p and emergency code card:

Reference	*Data*
Para 6–10 ----	I/p and emergency decoding circuit functioning.
Fig. 24–33 ---	I/p and emergency code card 1A2A2A7 schematic diagram.

20–104. Test Equipment Required

a. If the i/p and emergency code card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 generator is not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set.

(3) Test facilities set.

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–105. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. Interconnect the test equipment listed in paragraph 20–104, above, and the hot mockup IFF set as shown in figure 24–16, except disregard the mode word generator connections shown. (The mode 4 word generator is not needed.)

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker to ON.

e. Set the controls on the radar test set as directed in paragraph 12–5*e*, except set the FUNCTION switch on the SIF CODER panel to ID. This will provide a code 7777 i/p reply.

f. Set the controls on the oscilloscope as directed in paragraph 12–5*f*.

g. At the hybrid attenuator of the test facilities set, turn the ATTENUATOR to maximum attenuation.

h. Turn on the 28-volt dc power supply and adjust it for an output voltage of 28 volts.

20–106. Troubleshooting Chart

a. Preliminary Procedure. With the i/p and emergency code card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–105*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 0000 (or any code other than 7777), by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 0000 (or any code other than 7777).

(4) At the radar test set, simulate a mode 3/A code 7777 ID (i/p) reply at a range such that the first reply pulse appears at 1A2A2A6J1–3 as a receiver video pulse 500 μsec after the simulated radar trigger applied to 1J1.

(5) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. I/p and Emergency Code Card 1A2A2A7 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 34	Oscilloscope	Reply Enable 1 (same as R, fig. 20–10, except inverted).	If abnormal, isolate to A7, A10C or A13C.
2	Pin 38	Oscilloscope	Buffered 20.3 μsec (same as V, fig. 20–9).	If abnormal, isolate to A7C or A15B.
3	Pin 24	Oscilloscope	Buffered 4.35 μsec (same as W, fig. 20–9).	If abnormal, isolate to A3B or A10A.
			FOR STEPS 4 THROUGH 37, SET "MODE 3/A CODE SELECT" SWITCHES ON CONTROL BOX TO "7777."	
4	Pin 40	Oscilloscope	$\overline{\text{I/P video}}$ (M, fig. 20–13)	If abnormal, proceed with step 4. If normal, proceed with step 38.
5	J1–6	Oscilloscope	$\overline{\text{Gated sif correct code pulse}}$ (G, fig. 20–13).	If abnormal, proceed with step 6. If normal, proceed with step 7.
6	J1–4	Oscilloscope	Counter reset (D, fig. 20–13).	If abnormal, check that J1–4 is high whenever reply enable 1 (pin 34) is low. If J1–4 is high when Pin 34 is low, A3 is defective. If J1–4 is not high when Pin 34 is low, OR A10C is defective.
7	A12–8	Oscilloscope	$\overline{\text{5 Mc clock}}$ (same as Q, fig. 20–10).	If abnormal, inverter A12C is defective.
8	J1–5	Oscilloscope	Short count-decode enable (F, fig. 20–13).	If abnormal, observe waveform at Pin 5 of A13. It should go low at the leading edge of the incoming $\overline{\text{sif correct code pulse}}$ (step 5). If it does, flip-flop A6A is defective. If it does not, A13 is defective.
9	A8–12	Oscilloscope	$\overline{\text{Short count stop pulse}}$ (V, fig. 20–13).	If normal, proceed with step 24. If abnormal, proceed with step 10.
10	A10–5	Oscilloscope	Sif correct code pulse (X, fig. 20–13).	At this point only the first pulse is of importance. If the first pulse is normal, proceed with step 15. If the first pulse is abnormal, proceed with step 11.
11	A15–3	Oscilloscope	High at time of first pulse in X, fig. 20–13.	If normal, proceed with step 13. If abnormal, proceed with step 12.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
12	J1-9	Oscilloscope	Low at time of first pulse in X, fig. 20-13.	If normal, AND A15A is defective. If abnormal, isolate to A7B, A11B or A15B.
13	A10-3	Oscilloscope	High at time of first pulse in X, fig. 20-13.	If normal, OR A10B is defective. If abnormal, proceed with step 14.
14	J1-2	Oscilloscope	Low at time of first pulse in X, fig. 20-13.	If normal, AND A10A is defective. If abnormal, isolate to A2B or A3.
15	A13-8	Oscilloscope	$\overline{\text{Counter start}}$ (same as step 10, except inverted).	As in step 10, only the first pulse is of importance. If abnormal, AND A13C is defective.
16	J1-7	Oscilloscope	Goes high at leading edge of pulse observed in step 15. (H, fig. 20-13).	If abnormal, flip-flop A6B is defective. *Note.* Only the response at the leading edge of the first $\overline{\text{counter start}}$ pulse is of importance at this time.
17	A14-13	Oscilloscope	$\overline{\text{0.2 μsec digital single-shot}}$ (Z, fig. 20-13).	Only the first pulse is important at this time. If the first pulse is abnormal, isolate to flip-flop A14 or AND A13A.
18	J1-4	Oscilloscope	Counter reset goes low at leading edge of pulse observed in step 17 (D, fig. 20-13).	If abnormal, OR A10C is defective.
19	A12-3	Oscilloscope	Inverts whatever is present at step 18.	If abnormal, inverter A12A is defective.
20	A12-5	Oscilloscope	Same as step 19	If abnormal, inverter A12B is defective.
21	J1-3	Oscilloscope	$\overline{2^1}$ (C, fig. 20-13)	At this point, only the first four negative going pulses are important. If they are abnormal, flip-flop A5 is defective.
22	A4-8	Oscilloscope	$\overline{2^3}$ (S, fig. 20-13)	At this point, only the first negative going pulse is of importance. If this pulse is abnormal, flip-flop A4 is defective.
23	A1-12	Oscilloscope	2^4 (same as Q, fig. 20-13, except inverted).	At this point, only the first positive going pulse at A1-12 is of importance. If the first pulse is normal, AND A8 is defective. If this pulse is abnormal, flip-flop A1A is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
24	J1-8	Oscilloscope	$\overline{\text{Long count stop pulse}}$ (J, fig. 20-13).	If normal, proceed with step 35. If abnormal, proceed with step 25.
25	A7-3	Oscilloscope	Counter stop pulse (T, fig. 20-13).	At this point only the first pulse is important. It should be the same as V, fig. 20-13, except inverted. If this pulse is normal, proceed with step 26. If abnormal, OR A7A is defective.
26	J1-2	Oscilloscope	(B, fig. 20-13)	The leading edge goes high when the $\overline{\text{short count stop}}$ pulse goes low (step 9). If this is abnormal, flip-flop A2B is defective. If the trailing edge is abnormal, proceed with step 27. If J1-2 is normal, proceed with step 28.
27	A3-3	Oscilloscope	(R, fig. 20-13)	If abnormal, A3 is defective. If normal, flip-flop A2B is defective.
28	A10-3	Oscilloscope	$\overline{\text{Long count start}}$ (W, fig. 20-13).	If abnormal, AND A10A is defective.
29	A10-5	Oscilloscope	Counter start pulses (X, fig. 20-13).	If abnormal, proceed with step 30. If normal, proceed with step 31.
30	A15-3	Oscilloscope	High	If normal, OR A10B is defective. If abnormal, AND A15A is defective.
31	J1-7	Oscilloscope	(H, fig. 20-13)	At this time only the narrow negative going pulse is important. If this pulse is abnormal, flip-flop A6B is defective. If this pulse is normal, proceed with step 32.
32	J1-4	Oscilloscope	Counter reset (D, fig. 20-13)	At this time only the narrow positive going pulse is important. If this pulse is abnormal, OR A10C is defective. If the pulse is normal, proceed with step 33.
33	A1-9	Oscilloscope	2^5 (P, fig. 20-13)	There should be two positive going pulses. If two pulses are not present, flip-flop A1 is defective. If normal, or if more than two pulses are present, proceed with step 34.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
34	A2–12	Oscilloscope	2^6 (same as A, fig. 20–13 except inverted).	There should be one positive going pulse. If the one pulse is normal AND A9 is defective. If there is more than one pulse, but the first is normal, AND A9 is defective. If the first pulse is abnormal, flip-flop A2A is defective.
35	A7–3	Oscilloscope	Counter stop pulse (T, fig. 20–13).	If abnormal, OR A7A is defective.
36	J1–9	Oscilloscope	I/p for emergency video enable (K, fig. 20–13).	The leading edge should be coincident with the leading edge of the long count stop pulse (step 24). If the leading edge is abnormal, flip-flop A11B is defective. If the trailing edge is defective check A7–5 (U, fig. 20–13). If A7–5 is normal, flip-flop A11B is defective. If A7–5 is abnormal, isolate to A7B or A15B. If J1–9 is normal, proceed with step 37.
37	J1–10	Oscilloscope	I/p reply (L, fig. 20–13)	If abnormal, AND A7C is defective. If normal, A15 is defective.
			FOR STEPS 38 AND 39, SET "MODE 3/A CODE SELECT" SWITCHES ON CONTROL BOX TO "7700." THEN, AT RADAR TEST SET, CHANGE THE SIMULATED CODE 7777 I/P REPLY TO A CODE 7700 EMERGENCY REPLY.	
38	Pin 40	Oscilloscope	Emergency video (N, fig. 20–13).	If abnormal, proceed with step 39.
39	A15–3	Oscilloscope	Emergency enabled bracket decoded video (AA, fig. 20–13).	If normal, OR A10B is defective. If abnormal, A15 is defective.

20–107. Test Procedure

a. The test procedure for the i/p and emergency code card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the i/p and emergency code card after repair, first check the card for short circuits that might have been introduced during repair by com-

paring resistance measurements at its etched connector pins with the values listed in paragraph 20-108. Then prepare a hot mockup as for troubleshooting (paras 20-104 and 20-105) and perform the preliminary procedure given in paragraph 20-106*a*, except set the MODE 3/A CODE SELECT switches at 7777. Do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signal at 1A2A2A7-40, i/p or emergency video (M, fig. 20-13).

c. At control box, set MODE 3/A CODE SELECT switches at 7700. Then, at radar test set, change the simulated code 7777 i/p reply to a code 7700 emergency reply and observe the signal at 1A2A2A7-40, i/p or emergency video (N, fig. 20-13).

20-108. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating i/p and emergency code card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-104 and 20-105). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-106a), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. I/p and Emergency Code Card 1A2A2A7 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1500	RX100	300
4	5.0	RX100	1500	RX100	300
5	Not used				
6	Not used				
7	Not used				
8	2.2	RX10,000	740K	RX100	1500
9	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
10	1.65	RX10,000	700K	RX100	1550
11	Not used				
12	1.55	RX10,000	700K	RX100	1550
13	Not used				
14	0.08	RX10,000	700K	RX100	750
15	Not used				
16	Not used				
17	Not used				
18	Not used				
19	Not used				
20	Not used				
21	Not used				
22	Not used				
23	Not used				
24	0.12	RX10,000	600K	RX100	1350
25	Not used				
26	Not used				
27	Not used				
28	Not used				
29	Not used				
30	3.9	RX10,000	400K	RX100	1700
31	Not used				
32	0.1	RX10,000	600K	RX100	1500
33	Not used				
34	3.8	RX10,000	380K	RX100	1250
35	Not used				
36	0.1	RX10,000	700K	RX100	1700
37	Not used				
38	0.13	RX10,000	360K	RX100	1450

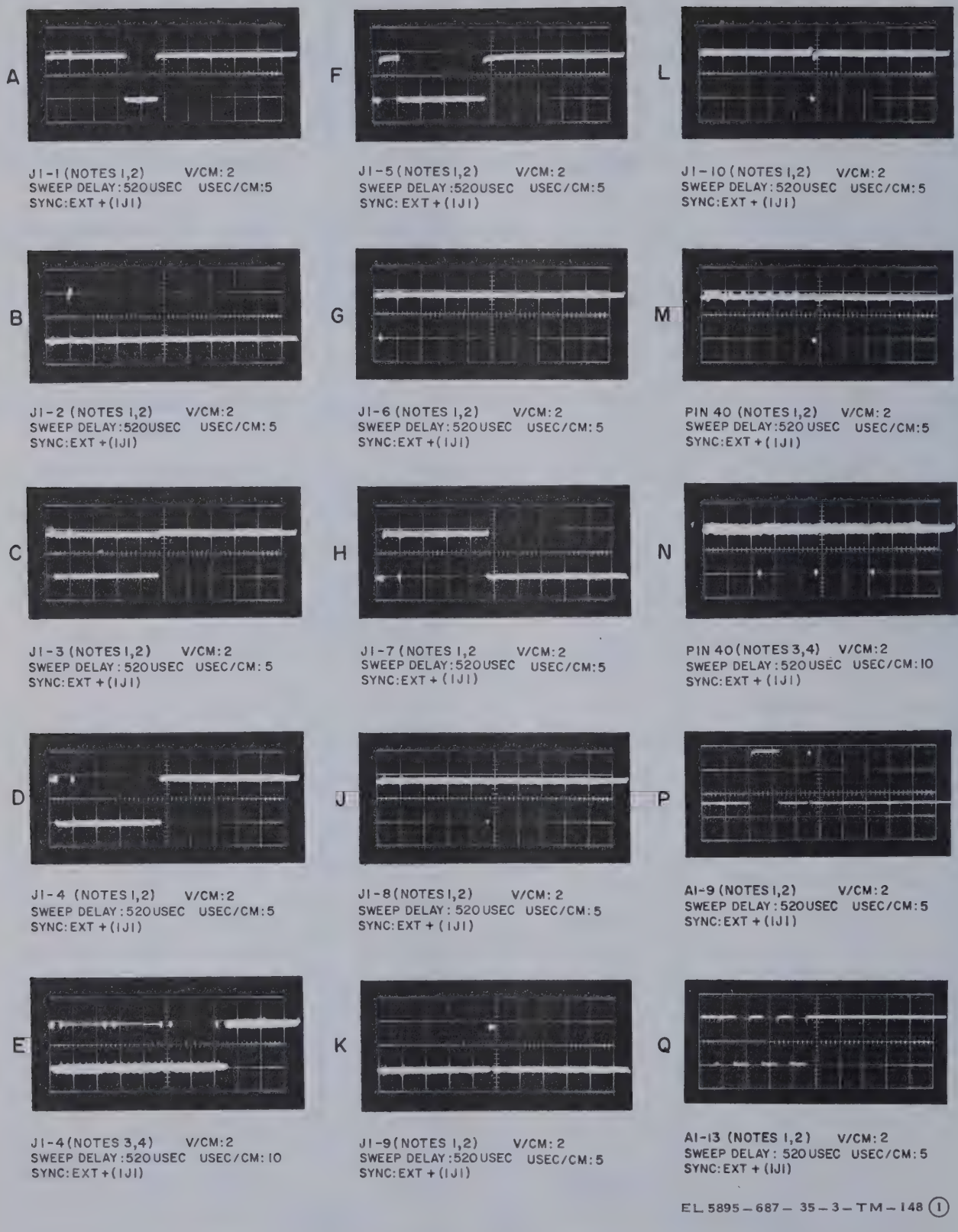
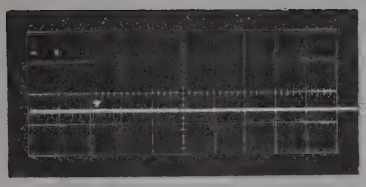


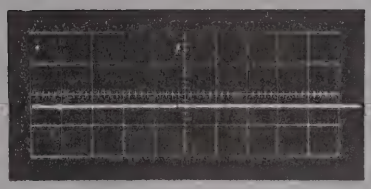
Figure 20-13①. I/p and emergency code card 1A2A2A7 waveforms (sheet 1 of 2).

R



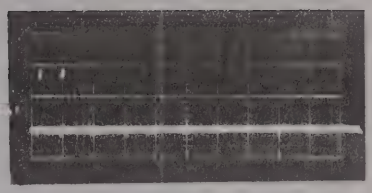
A3-3 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

U



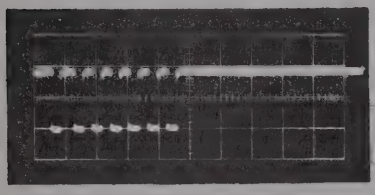
A7-5 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

X



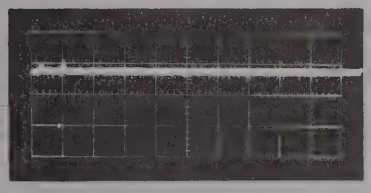
A10-5 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

S



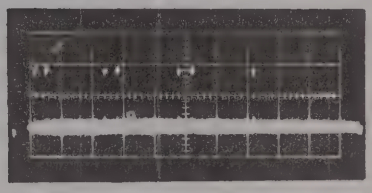
A4-8 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

V



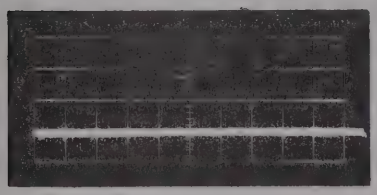
A8-12 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

Y



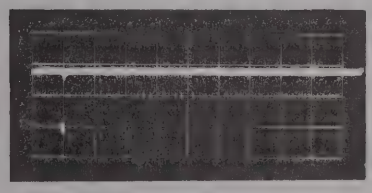
A10-5 (NOTES 3,4) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 10
SYNC: EXT + (1J1)

T



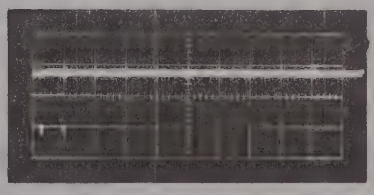
A7-3 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

W



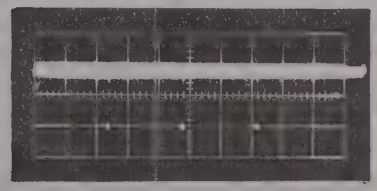
A10-3 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

Z



A14-13 (NOTES 1,2) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 5
SYNC: EXT + (1J1)

AA



A15-3 (NOTES 3,4) V/CM: 2
SWEEP DELAY: 520 USEC USEC/CM: 10
SYNC: EXT + (1J1)

NOTES:

1. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7777, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7777.
2. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7777 I/P REPLY AT A RANGE SUCH THAT FIRST REPLY PULSE APPEARS AT 1A2A2A6J1-3 AS A RECEIVER VIDEO PULSE 500 USEC AFTER THE SIMULATED RADAR TRIGGER APPLIED TO 1J1.
3. AT CONTROL BOX, CHALLENGE IN MODE 3/A, CODE 7700, BY HOLDING CHALLENGE SWITCH AT ON WITH MODE SELECT SWITCH AT 3/A AND WITH MODE 3/A CODE SELECT SWITCHES AT 7700.
4. AT RADAR TEST SET, SIMULATE A MODE 3/A CODE 7700 EMERGENCY REPLY AT THE SAME RANGE AS SPECIFIED IN NOTE

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Figure 20-13②. I/p and emergency code card 1A2A2A7 waveforms (sheet 2 of 2).

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
39	0.08	RX10,000	430K	RX100	1600
40	3.8	RX10,000	5 Mego	RX100	800
41	5.0	RX100	1500	RX100	300
42	5.0	RX100	1500	RX100	300
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–109. Waveforms
(fig. 20–13)

Figure 20–13 shows the i/p and emergency code card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–104, 20–105, and 20–106*a*).

Section XVI. CODER-DECODER SELF-TEST CARD 1A2A2A8 TROUBLESHOOTING AND REPAIR

20–110. General

This section presents specific troubleshooting and testing information for coder-decoder self-test card 1A2A2A8. For troubleshooting, paragraph 20–111 lists helpful data located in other parts of this manual, and paragraphs 20–112 and 20–113 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–114 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–115 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–14 shows the card waveforms which are of significance in troubleshooting and testing.

20–111. Reference Data

The data listed in the following chart will be helpful when troubleshooting the coder-decoder self-test card:

Reference	*Data*
Para 5–13 ----	Challenge encoding self-test circuit functioning.
Para 6–11 ----	Reply decoding self test circuit functioning.
Para 5–14 ----	Fault accumulator circuit functioning.
Fig. 24–34 ---	Coder-decoder self-test card 1A2A2A8 schematic diagram.

20–112. Test Equipment and Preparation

The test equipment and preparation required for troubleshooting the coder-decoder self-test card are the same as for overall synchronizer troubleshooting (paras 12–4 and 12–5), with the card installed in an otherwise satisfactory synchronizer as the item to be repaired. Therefore, if the card is installed in a synchronizer which is already connected into the complete hot mockup shown in figure 24–16, and if all initial control settings have been made as directed in paragraph 12–5, no further preparation is required. Otherwise, install the card in a satisfactory synchronizer, connect the synchronizer to the hot mockup as shown in figure 24–16, and proceed as directed in paragraph 12–5*c* through *i*.

20–113. Troubleshooting Chart

a. Preliminary Procedure. With the coder-decoder self-test card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into the complete hot mockup shown in figure 24–16, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and challenge in mode 3/A, code 7777, by holding the CHALLENGE switch at ON with the MODE SELECT switch at 3/A and with the MODE 3/A CODE SELECT switches at 7777.

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Coder-Decoder Self-Test Card 1A2A2A8 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	J1–6	Oscilloscope	Continuously low	If normal, proceed with step 44. If abnormal, proceed with step 2.
2	J2–2	Oscilloscope	$\overline{\text{Decoding fault}}$ (K, fig. 20–14).	If normal, proceed with step 20. If abnormal, proceed with step 3.
3	J1–8	Oscilloscope	Self-test gate (F, fig. 20–14)	If abnormal, flip-flop A14B is defective.
4	Pin 19	Oscilloscope	$\overline{\text{Reshaped self-test pretrigger}}$ (S, fig. 20–14).	If abnormal, inverter A11A is defective.
5	Pin 20	Oscilloscope	$\overline{\text{Reshaped self-test pretrigger}}$ (S, fig. 20–14).	If abnormal, inverter A11B is defective.
6	Pin 9	Oscilloscope	$\overline{\text{Code override}}$ (R, fig. 20–14).	If abnormal, flip-flop A14A is defective.
7	J1–7	Oscilloscope	Code override (E, fig. 20–14).	If abnormal, flip-flop A15A is defective.
8	J1–9	Oscilloscope	$\overline{\text{1.8 μsec fault}}$ (G, fig. 20–14)	If abnormal, flip-flop A15B is defective.
9	J1–1	Oscilloscope	$\overline{\text{3.6 μsec fault}}$ (A, fig. 20–14)	If abnormal, flip-flop A10B is defective.
10	J1–10	Oscilloscope	C1–D4 kill (H, fig. 20–14)	If abnormal, OR A11C is defective.
11	Pin 28	Oscilloscope	$\overline{\text{ISLS gate}}$ (same as W, fig. 20–10).	If abnormal, isolate to A6B or A12A.
12	J1–3	Oscilloscope	Kill count 2^1 (D, fig. 20–14)	If normal, proceed with step 14. If abnormal, proceed with step 13.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
13	A10-12	Oscilloscope	Kill count 2^0 (W, fig. 20-14)	If normal, flip-flop A6B is defective. If abnormal, flip-flop A10A is defective.
14	J1-4	Oscilloscope	$\overline{\text{Gtc trigger}}$ (same as M, fig. 20-11).	If abnormal, isolate to A6A or A13B.
15	J2-6	Oscilloscope	Kill count 2^3 (N, fig. 20-14)	If abnormal, flip-flop A6A is defective.
16	J2-1	Oscilloscope	Kill count 2^5 (J, fig. 20-14)	If normal, proceed with step 19. If abnormal, proceed with step 17.
17	Pin 26	Oscilloscope	Buffered 20.3 μsec (same as Y, fig. 20-9).	If abnormal, isolate to A8A or A11D.
18	A11-14	Oscilloscope	$\overline{\text{Buffered 20.3 μsec}}$ (same as Y, fig. 20-9 except inverted).	If normal, flip-flop A7A is defective. If abnormal, inverter A11D is defective.
19	A8-3	Oscilloscope	$\overline{\text{Gated 20.3 μsec pulse}}$ (V, fig. 20-14).	If normal, flip-flop A7B is defective. If abnormal, AND A8A is defective.
20	J2-5	Oscilloscope	$\overline{\text{Sif fault}}$ (M, fig. 20-14)	If normal, proceed with step 36. If abnormal, proceed with step 21.
21	Pin 23	Oscilloscope	Sif enable	If abnormal, isolate to A1C, A16A, or A17B.
22	A12-14	Oscilloscope	$\overline{\text{Self test pretrigger}}$ (same as L, fig. 20-19).	If normal, proceed with step 24. If abnormal, proceed with step 23.
23	A16-14	Oscilloscope	Self-test pretrigger (same as L, fig. 20-19, except inverted).	If normal, inverter A12D is defective. If abnormal, A16 is defective.
24	A5-8	Oscilloscope	Goes high at leading edge of self-test pretrigger observed in step 22, and goes low at trailing edge of mode 4 pretrigger (trailing edge of K, fig. 20-18).	If abnormal, flip-flop A5B is defective.
25	J2-10	Oscilloscope	P1 trigger (Q, fig. 20-14)	If normal, proceed with step 29. If abnormal, proceed with step 26.
26	Pin 39	Oscilloscope	Challenge video (same as A, fig. 20-11, except inverted).	If abnormal, isolate to A8B, A9D, A12B, A16C or A17B.
27	A16-8	Oscilloscope	P1 trigger (same as T, fig. 20-10, except inverted).	If abnormal, AND A16C is defective.
28	A12-8	Oscilloscope	Continuously high	If normal, A8 is defective. If abnormal, A12 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
29	A5-12	Oscilloscope	$\overline{\text{P1 fault}}$ (T and U, fig. 20-14)	If abnormal, flip-flop A5A is defective.
30	J2-9	Oscilloscope	Isls pulse (P, fig. 20-14)	If normal, proceed with step 32. If abnormal, proceed with step 31.
31	A12-5	Oscilloscope	Isls pulse (same as P, fig. 20-14, except inverted).	If normal, A9 is defective. If abnormal, A12 is defective.
32	A13-12	Oscilloscope	$\overline{\text{Isls fault}}$ (Z and AA, fig. 20-14).	If abnormal, flip-flop A13A is defective.
33	A13-9	Oscilloscope	$\overline{\text{Gtc fault}}$ (X and Y, fig. 20-14).	If abnormal, flip-flop A13B is defective.
34	A13-8	Oscilloscope	$\overline{\text{Gtc fault}}$ (same as step 33, except inverted).	If abnormal, flip-flop A13B is defective.
35	A17-8	Oscilloscope	P3 fault (AB and AC, fig. 20-14).	If normal, AND A1C is defective. If abnormal, flip-flop A17B is defective.
36	J2-7	Oscilloscope	$\overline{\text{Mode 4}}$ fault continuously high.	If normal, proceed with step 38. If abnormal, proceed with step 37.
37	A17-12	Oscilloscope	Continuously low	If normal, AND A1D is defective. If abnormal, flip-flop A17A is defective.
38	J2-8	Oscilloscope	$\overline{\text{Excess pulse fault}}$ (continuously high).	If normal, proceed with step 42. If abnormal, proceed with step 39.
39	A1-5	Oscilloscope	Continuously high	If abnormal, AND A1B is defective.
40	J2-4	Oscilloscope	Continuously high	If abnormal, AND A9D is defective.
41	A9-8	Oscilloscope	Continuously high	If abnormal, AND A9C is defective. If normal, isolate to A1A or A4A.
42	J1-2	Oscilloscope	Sif coder decoder fault (B, fig. 20-14).	If abnormal, OR A4B is defective.
43	A3-12	Oscilloscope	Continuously low	If abnormal, A3 is defective. If normal, A2 is defective.
44	Pin 22	Oscilloscope	$\overline{\text{Code override}}$ (same as E, fig. 20-14, except inverted).	If abnormal, flip-flop A15A is defective.
45	A12-3	Oscilloscope	Isls gate (same as W, fig. 20-10, except inverted).	If abnormal, inverter A12A is defective.
			PRIOR TO PERFORMING STEPS 46 THROUGH 50 PLACE CONTROL BOX "MODE SELECT" SWITCH TO "4."	

Step No.	Test point	Test equipment	Normal indication	Corrective measures
46	J2–5	Oscilloscope	$\overline{\text{Sif fault}}$ continuously high	If abnormal, AND A1C is defective.
47	A16–14	Oscilloscope	Mode 4 challenge video (same as F, fig. 20–11).	If abnormal, A16 is defective.
48	J2–7	Oscilloscope	$\overline{\text{Mode 4 fault}}$ (continuously high).	If normal, proceed with step 50. If abnormal, proceed with step 49.
49	A17–12	Oscilloscope	(AD, fig. 20–14)	If normal, AND A10A is defective. If abnormal, flip-flop A17A is defective.
50	J1–2	Oscilloscope	Mode 4 coder decoder fault (C, fig. 20–14).	If abnormal, OR A4B is defective.
			FOR STEPS 51 AND 52 PLACE CONTROL BOX "MODE SELECT" SWITCH TO "3/A," AND REMOVE THE GROUND FROM THE ISLS PULSE INHIBIT LINE FROM R/T.	
51	J2–10	Oscilloscope	P1 trigger (Q, fig. 20–14)	If abnormal, A8 is defective.
52	J2–9	Oscilloscope	Isls gate (same as W, fig. 20–10, except inverted).	If abnormal, A9 is defective.

20–114. Test Procedure

a. The test procedure for the coder-decoder self-test card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the coder-decoder self-test card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–115. Then prepare a hot mockup as for troubleshooting (para 20–112) and perform the preliminary procedure given in paragraph 20–113*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A2A8J1–1, $\overline{\text{3.6 μsec fault}}$ (A, fig. 20–14).

(2) 1A2A2A8J1–2, sif coder-decoder fault (B, fig. 20–14).

(3) 1A2A2A8J1–3, kill count 2^1 (D, fig. 20–14).

(4) 1A2A2A8J1–6, coder-decoder fault (should be low).

(5) 1A2A2A8J1–7, code override (E, fig. 20–14).

(6) 1A2A2A8J1–8, self-test gate (F, fig. 20–14).

(7) 1A2A2A8J1–9, $\overline{\text{1.8 μsec fault}}$ (G, fig. 20–14).

(8) 1A2A2A8J1–10, c1–d4 kill (H, fig. 20–14).

(9) 1A2A2A8J2–1, kill count 2^3 (J, fig. 20–14).

(10 1A2A2A8J2–2, $\overline{\text{decoding fault}}$ (K, fig. 20–14).

(11) 1A2A2A8J2–5, $\overline{\text{sif fault}}$ (M, fig. 20–14).

(12) 1A2A2A8J2–6, kill count 2^2 (N, fig. 20–14).

(13) 1A2A2A8J2-9, isls gate (P, fig. 20-14).

(14) 1A2A2A8J2-10, p1 trigger (Q, fig. 20-14).

(15) 1A2A2A8-9, $\overline{\text{code override}}$ (R, fig. 20-14).

(16) 1A2A2A8-19, $\overline{\text{reshaped self-test pretrigger}}$ (S, fig. 20-14).

(17) 1A2A2A8-20, $\overline{\text{reshaped self-test pretrigger}}$ (S, fig. 20-14).

(18) 1A2A2A8-22, $\overline{\text{code override}}$ (same as R, fig. 20-14).

c. Turn off receiver-transmitter and slide outward from interrogator group case approximately one inch to disconnect the rear connectors. Observe the signals at the following points:

(1) 1A2A2A2J2-9, isls gate (same as W, fig. 20-10, except inverted).

(2) 1A2A2A2J2-10, p1 trigger (Q, fig. 20-14).

Return receiver-transmitter to its original position and turn on.

d. At control box, challenge in mode 4 by holding CHALLENGE switch at ON with MODE SELECT switch at 4 and observe the signals at the following points:

(1) 1A2A2A8J1-2, sif coder-decoder fault (C, fig. 20-14).

(2) 1A2A2A8J2-7, $\overline{\text{mode 4 fault}}$ (should be high).

e. At mode 4 word generator, set TEST WORD switch 5 to ON (up). CODER DECODER FAULT lamp on synchronizer front panel should light. Return TEST WORD switch 5 to OFF (down).

20-115. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating coder-decoder self-test card.

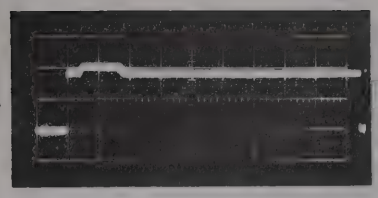
(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (para 20-112). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-113*a*), except that at the control box the CHALLENGE switch was left at OFF (released).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Coder-Decoder Self-Test Card 1A2A2A8 Etched Connector Pin Voltage and Resistance Measurements.

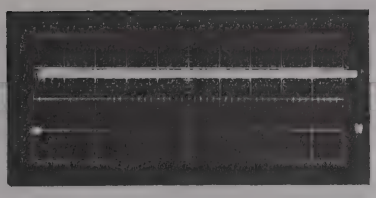
Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	5.7	RX10,000	900K	RX100	1500
2	0.0	RX1	0.0	RX1	0.0
3	0.25	RX100	3200	RX100	1400
4	5.0	RX100	900	RX100	240

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
5	4.2	RX10,000	600K	RX100	1400
6	5.0	RX100	3500	RX100	1300
7	2.2	RX10,000	800K	RX100	1500
8	0.1	RX10,000	800K	RX100	1350
9	4.3	RX100	3500	RX100	650
10	0.1	RX10,000	700K	RX100	1600
11	0.13	RX100	3500	RX100	650
12	2.2	RX10,000	900K	RX100	1500
13	0.1	RX100	3300	RX100	1050
14	4.0	RX100	3500	RX100	1300
15	0.12	RX10,000	800K	RX100	1450
16	3.9	RX10,000	800K	RX100	1500
17	0.2	RX10,000	550K	RX100	1000
18	0.1	RX100	3300	RX100	1450
19	4.1	RX100	3500	RX100	700
20	4.1	RX100	3500	RX100	700
21	3.9	RX10,000	520K	RX100	1000
22	4.1	RX100	3400	RX100	630
23	0.15	RX10,000	600K	RX100	1000
24	3.9	RX10,000	550K	RX100	1000
25	0.14	RX10,000	650K	RX100	1000
26	0.13	RX10,000	450K	RX100	1000
27	Not used				
28	5.3	RX100	3200	RX100	1000
29	Not used				
30	0.13	RX10,000	700K	RX100	1000
31	Not used				
32	0.14	RX10,000	680K	RX100	1000
33	Not used				



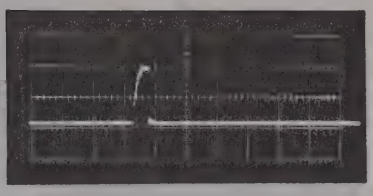
A

J1-1 V/CM:2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



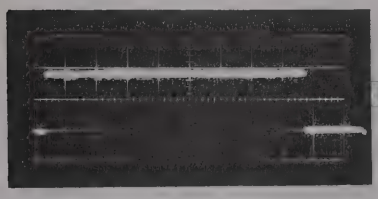
F

J1-8 V/CM:2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



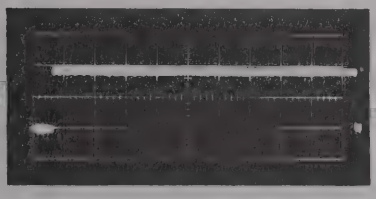
L

J2-3 (NOTE 2) V/CM:2
SWEEP DELAY: 370 USEC USEC/CM: 2
SYNC: EXT + (1J1)



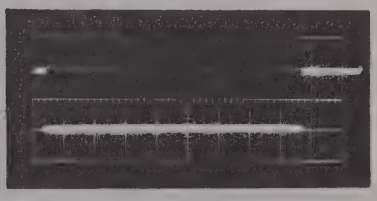
B

J1-2 (NOTE 1) V/CM:2
SWEEP DELAY: NONE USEC/CM: 50
SYNC: EXT + (1J1)



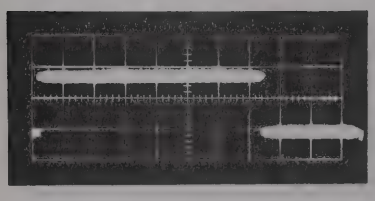
G

J1-9 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



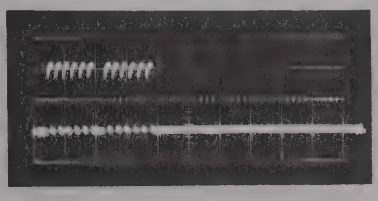
M

J2-5 (NOTE 1) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 50
SYNC: EXT + (1J1)



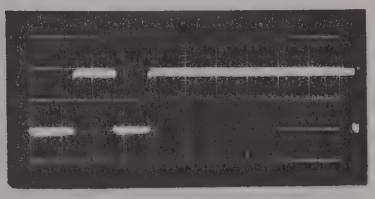
C

J1-2 (NOTE 2) V/CM: 2
SWEEP DELAY: NONE USEC/CM: 50
SYNC: EXT + (1J1)



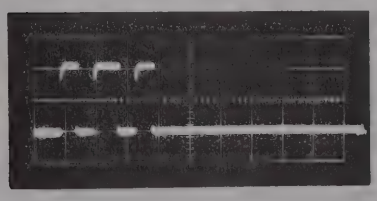
H

J1-10 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



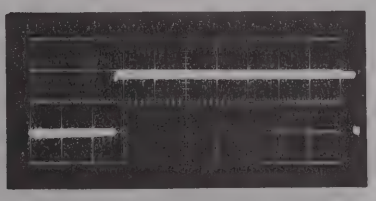
N

J2-6 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



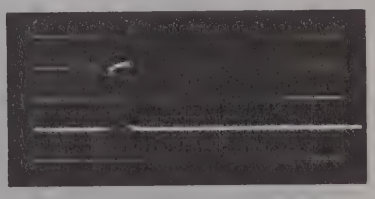
D

J1-3 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



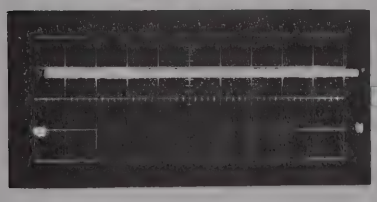
J

J2-1 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



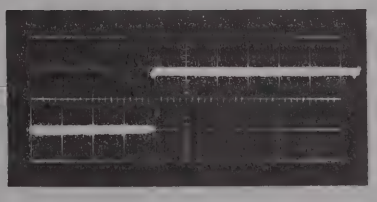
P

J2-9 (NOTE 1) V/CM: 2
SWEEP DELAY: 423 USEC USEC/CM: 1
SYNC: EXT + (1J1)



E

J1-7 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)



K

J2-2 V/CM: 2
SWEEP DELAY: 354 USEC USEC/CM: 5
SYNC: EXT + (1J1)

Q

J2-10 (NOTE 1) V/CM: 2
SWEEP DELAY: 423 USEC USEC/CM: 1
SYNC: EXT + (1J1)

EL 5895-687-35-3-TM-149 ①

Figure 20-14①. Coder-decoder self-test card 1A2A2A8 waveforms (sheet 1 of 2).

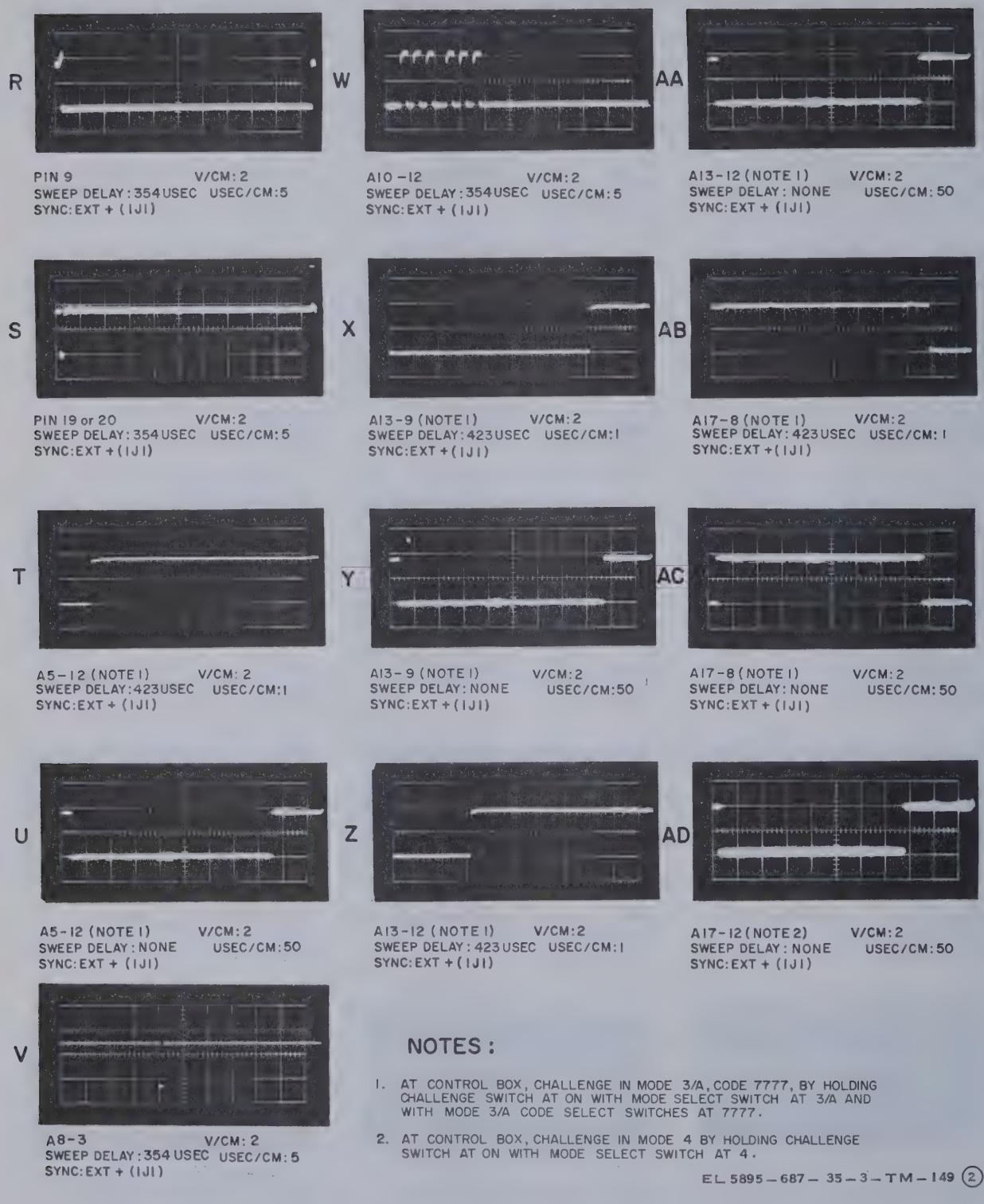


Figure 20-14②. Coder-decoder self-test card 1A2A2A8 waveforms (sheet 2 of 2).

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
34	0.13	RX10,000	600K	RX100	1000
35	Not used				
36	5.6	RX10,000	600K	RX100	1350
37	Not used				
38	0.0	RX10,000	450K	RX100	1000
39	0.13	RX10,000	300K	RX100	1000
40	0.15	RX100	3200	RX100	1450
41	5.0	RX100	900	RX100	240
42	5.0	RX100	900	RX100	240
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–116. Waveforms

(fig. 20–14)

Figure 20–14 shows the coder-decoder self-test card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–112 and 20–113*a*).

Section XVII. +12-VOLT REGULATOR CARD 1A2A3A1 TROUBLESHOOTING AND REPAIR

20–117. General

This section presents specific troubleshooting and testing information for +12-volt regulator card 1A2A3A1. For troubleshooting, paragraph 20–118 lists helpful data located in other parts of this manual, and paragraphs 20–119, 20–120, and 20–121 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20–122 references the applicable adjustment procedure, and paragraph 20–123 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–124 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–15 shows the card waveforms which are of significance in troubleshooting and testing.

20–118. Reference Data

The data listed in the following chart will be helpful when troubleshooting the +12-volt regulator card:

Reference	*Data*
Para 9–2 -----	+12-volt regulator functioning.
Fig. 24–36 ---	+12-volt regulator card 1A2A3A1 schematic diagram.

20–119. Test Equipment Required

a. If the +12-volt regulator card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup.

However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Oscilloscope.

(3) Radar test set (only to supply "0" TRIGGER output to 1J1).

(4) Test facilities set (only for cables W32, W41, W42, and W47).

(5) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–120. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls at the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output of 28 volts.

20–121. Troubleshooting Chart

a. Preliminary Procedure. With the +12-volt regulator card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–120*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to OFF.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the indications at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. +12-Volt Regulator Card 1A2A3A1 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	POWER circuit breaker 1A2CB1 (set to ON).	None	Remains at ON	If normal, leave 1A2CB1 at ON and proceed with step 2. If 1A2CB1 trips to OFF, remove interface module 1A2A1 and coder-decoder module 1A2A2 for their protection. Then remove +5-volt regulator card 1A2A3A2 and −12-volt inverter card 1A2A3A3 and proceed with step 2.
2	1A2CB1 (set to ON).	None	Remains at ON	If normal, leave 1A2CB1 at ON and proceed with step

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				10. If 1A2CB1 trips to OFF, prepare for step 3 as follows, and then proceed with step 3: *a.* Turn off the processor and the receiver-transmitter by setting their POWER circuit breakers to OFF. *b.* Reduce the primary power voltage from the 28-volt dc power supply to zero (or minimum). *c.* Ground 1A2A3A1E14 with a jumper wire. *d.* Set 1A2CB1 to ON.
3	Voltmeter and ammeter on 28-volt dc power supply.	Slowly increase primary power voltage until voltmeter reading reaches 12.5 volts, or until ammeter reading reaches 1.5 amperes, whichever occurs first.	Primary power voltage reaches 12.5 volts before ammeter reading reaches 1.5 ampere.	If normal, leave primary power voltage at 12.5 volts and proceed with step 5. If ammeter reading reaches 1.5 ampere before voltmeter reading reaches 12.5 volts, proceed with step 4.
4	1A2A3A1E3 and 1A2A3A1E4 (voltage across R1).	Multimeter (measure voltage between test points).	Zero volts across R1 ----------	If normal, check Q1 and associated flywheel circuit. If abnormal, check Q4.
5	1A2CB1 ----------	(Remove grounding jumper from E14.)	1A2CB1 remains at ON -----	If normal, proceed with step 6. If 1A2CB1 trips to OFF, check Q3 and associated parts, including VR3.
6	1A2A3A1E10 ------	Multimeter (Ground Q5–B with a jumper wire).	Less than +2.5 volts at E10 when Q5–B is grounded.	If normal, remove the grounding jumper from Q5–B and proceed with step 9. If abnormal, leave Q5–B grounded and proceed with step 7.
7	1A2A3A1E11 and 1A2A3A1Q5–C.	Multimeter (Measure voltage between test points).	0.5 volt or less between E11 and Q5–C when Q5–B is grounded.	If abnormal, check Q5. If normal, prepare for step 8 as follows, and then proceed with step 8: *a.* Set 1A2CB1 to OFF. *b.* Disconnect Q1–C from E11 by unsoldering the corresponding wire from E11. *c.* Set 1A2CB1 to ON. (Leave Q5–B grounded.)
8	1A2A3A1E10 ------	Multimeter --------	Less than +2.5 volts at E10 when Q5–B is grounded.	If normal, check Q1. If abnormal, check Q2 and associated parts.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
9	1A2A3A1E10 ------	Multimeter (Slowly increase primary power voltage at 28-volt dc power supply, observing ammeter readiing. Stop increasing the voltage if ammeter reading reaches 2.5 amperes or if 1A2CB1 trips to OFF).	Voltage at E10 stops increasing at a value between +12 and +14 volts before ammeter reading reaches 2.5 amperes, and 1A2CB1 does not trip to OFF.	*a.* If ammeter reading on 28-volt dc power supply reaches 2.5 amperes, check C1 and the flywheel circuit associated with Q1. *b.* If 1A2CB1 trips to OFF before the voltage at E10 reaches +14 volts, check Q3 and associated parts, including VR3. *c.* If voltage at E10 reaches +14 volts and continues to increase, check Q6 and associated parts, including VR4. (1A2CB1 may trip above +14 volts at E10).
10	1A2A3A1E10 ------	Multimeter --------	+12 volts or higher ---------	If normal, set 1A2CB1 to OFF, reinstall 1A2A3A3, and proceed with step 16. If abnormal, check voltage at E12. If voltage at E12 is +12 volts or higher, check L1. If voltage at E12 is lower than +12 volts, proceed with step 11.
11	1A2A3A1E10 ------	Multimeter (Ground Q7-B with a jumper wire).	+12 volts or higher ---------	If normal, leave Q7-B grounded and proceed with step 14. If abnormal, leave Q7-B grounded and proceed with step 12.
12	1A2A3A1E11 and 1A2A3A1Q5-C.	Multimeter (Measure voltage between test points).	+10 volts or more between test points.	If normal, check Q2 and associated parts. If abnormal, remove the grounding jumper from Q7-B and proceed with step 13.
13	1A2A3A1Q5-B -----	Multimeter (Place a temporary short circuit between Q9-E and Q9-C).	+2.0 volts or higher --------	If normal, check Q5, CR9, and CR10. If voltage is between +1 and +2.0 volts, check Q7 and CR6. If voltage is +1 volt or less, check Q6 and associated parts, including VR4.
14	1A2A3A1-21 -------	Multimeter --------	+5.1 volts (approx) --------	If abnormal, check VR5, C9, and R26. If normal, remove the grounding jumper from Q7-B and proceed with step 15.
15	1A2A3A1E10 ------	Multimeter (Place a temporary short circuit between Q14-1 and Q14-2).	+12 volts or higher ---------	If normal, check Q14 and associated parts. If abnormal, check Q9 and Q12.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
16	1A2CB1 (Set to ON.)	None	Remains at ON	If normal, set 1A2CB1 to OFF, reinstall 1A2A1 and 1A2A2, and proceed with step 20. If 1A2CB1 trips to OFF, ground 1A2A3A3J4 with a jumper wire, set 1A2CB1 to ON, and proceed with step 17.
17	1A2A3A1E10	Multimeter	+11 volts or higher	If normal, check Q13 and associated parts. If abnormal, proceed with step 18.
18	1A2A3A1Q5–C	Oscilloscope	Waveform E, fig. 20–15	If normal, check Q1. If abnormal, proceed with step 19.
19	1A2A3A1Q12–B	Multimeter	+8 volts or lower	If normal, check Q12 and associated parts, including C6. If abnormal, check Q14 and associated parts, including VR5.
20	1A2CB1 (Set to ON.)	None	Remains at ON	If normal, set 1A2CB1 to OFF, reinstall 1A2A3A , and proceed with step 21. If 1A2CB1 trips to OFF, check Q1 and its associated flywheel circuit.
21	1A2CB1 (Set to ON.)	None	Remains at ON	If 1A2CB1 trips to OFF, check Q1 and its associated flywheel circuit.
22	1A2A3A1E10	Multimeter	+12 ±0.37 volts	If normal, proceed with step 27. If abnormal, adjust R27 as directed in paragraphs 18–10 and 18–11. If adjustment fails to produce normal indication, proceed with step 23.
23	1A2A3A1–21	Multimeter	+5.1 volts (approx)	If abnormal, check VR5, C9, and R26. If normal, proceed with step 24.
24	1A2A3A1Q5–C	Oscilloscope	Waveform E, fig. 20–15	If normal, check Q14 and associated parts. If abnormal, proceed with step 25.
25	1A2A3A1Q7–B	Oscilloscope	Waveform F, fig. 20–15	If normal, check Q7. If abnormal, proceed with step 26.
26	1A2A3A1Q10–C	Oscilloscope	Waveform K, fig. 20–15	If normal, check Q7 and associated parts, including CR6. If no waveform (continuously high or low), check Q10, Q11, and associated parts. If negative-going portions of waveform

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				are too narrow, check Q9, Q10, CR7, and R13. If the positive-going risetimes are too long, check Q8. If the negative-going portions of the waveform are too wide, check Q12.
27	1A2A3A1E10 ------	Oscilloscope --------	Waveform A, fig. 20-15 ------	If normal, proceed with step 28. If ripple spikes are excessive, check flywheel circuit associated with Q1. If ripple other than spikes is excessive, check C7 and C8.
28	1A2A3J2 ----------	Multimeter --------	+12 volts (approx) --------	If normal, proceed with step 29. If abnormal, check Q13 and associated parts.
29	1A2A3A1-21 -------	Multimeter --------	+5.1 volts (approx) --------	If abnormal, check VR5 and associated parts C9 and R26.

20-122. Adjustment

The single potentiometer on the +12-volt regulator card is +12-volt adjustment potentiometer 1A2A3A1R27, which is adjusted for an output of +12 volts. The adjustment procedure is given in paragraphs 18-10 and 18-11.

20-123. Test Procedure

a. The test procedure for the +12-volt regulator card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the +12-volt regulator card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-124. Then prepare a hot mockup as for troubleshooting (paras 20-119 and 20-120) and perform the preliminary procedure given in paragraph 20-121*a*, but do not continue with the troubleshooting chart. Instead, proceed as follows:

(1) Set POWER circuit breaker 1A2CB1 to ON.

(2) Measure the dc voltage at 1A2A3A1E10. The voltage should be +12 ±0.37 volts. While observing this voltage, adjust the VOLTAGE CONTROL on the 28-volt dc power supply to vary the input voltage throughout the range from 22 volts to 32 volts. The voltage at 1A2A3A1E10 should remain within tolerance over the entire range.

(3) Readjust the 28-volt dc power supply for an output of 28 volts.

(4) At the synchronizer, use the oscilloscope to observe the ripple waveform at 1A2A3A1E10 (A, fig. 20-15).

(5) Measure the dc voltage at 1A2A3A3J2. This is the current limited +12-volt output of 1A2A3A1, and should be the same, within +0.5 volt, as at 1A2A3A1E10.

(6) Set 1A2CB1 to OFF, remove +5-volt regulator card 1A2A3A2, and set 1A2CB1 back to ON.

(7) Measure the dc voltage at 1A2A3A1E10. While observing this voltage, temporarily ground 1A2A3A3J1 with a clip-lead to place the +12-volt regulator circuit in the AH mode. The voltage at 1A2A3A1E10 should not exceed +14 volts, and 1A2CB1 should not trip to OFF.

(8) Set 1A2CB1 to OFF, unground 1A2A3A3J1, and reinstall 1A2A3A2.

20–124. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating +12-volt regulator card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20–119 and 20–120). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–121*a*), except that the synchronizer POWER circuit breaker was set to ON.

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 9, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 9, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 9, and the negative probe was touched to each of the listed pins.

b. +12-Volt Regulator Card 1A2A3A1 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	Not used				
2	Not used				
3	0.15	RX100	1900	RX100	1900
4	Not used				
5	12.0	RX100	2200	RX100	400
6	12.0	RX100	2200	RX100	400
7	0.0	RX1	0.0	RX1	0.0
8	Not used				
9	0.0	RX1	0.0	RX1	0.0
10	Not used				
11	0.0	RX1	0.0	RX1	0.0
12	Not used				
13	0.0	RX1	0.0	RX1	0.0
14	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
15	12.5	RX100	2200	RX100	400
16	Not used				
17	12.5	RX100	2200	RX100	400
18	Not used				
19	12.5	RX100	2200	RX100	400
20	Not used				
21	4.9	RX100	2250	RX100	750
22	Not used				
23	Not used				
24	Not used				
25	26.0	RX100	10K	RX100	1000
26	Not used				
27	26.0	RX100	10K	RX100	1000
28	Not used				
29	26.0	RX100	10K	RX100	1000
30	Not used				
31	Not used				
32	Not used				
33	Not used				
34	Not used				
35	0.0	RX1	70	RX1	70
36	Not used				
37	Not used				
38	Not used				
39	0.16	RX100	800	RX10,000	5 Mego
40	Not used				
41	1.57	RX100	2700	RX100	800
42	Not used				
43	Not used				
44	Not used				

20–125. Waveforms
(fig. 20–15)

Figure 20–15 shows the +12-volt regulator card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–119, 20–120, and 120–121*a*), except that the synchronizer POWER circuit breaker was set to ON.

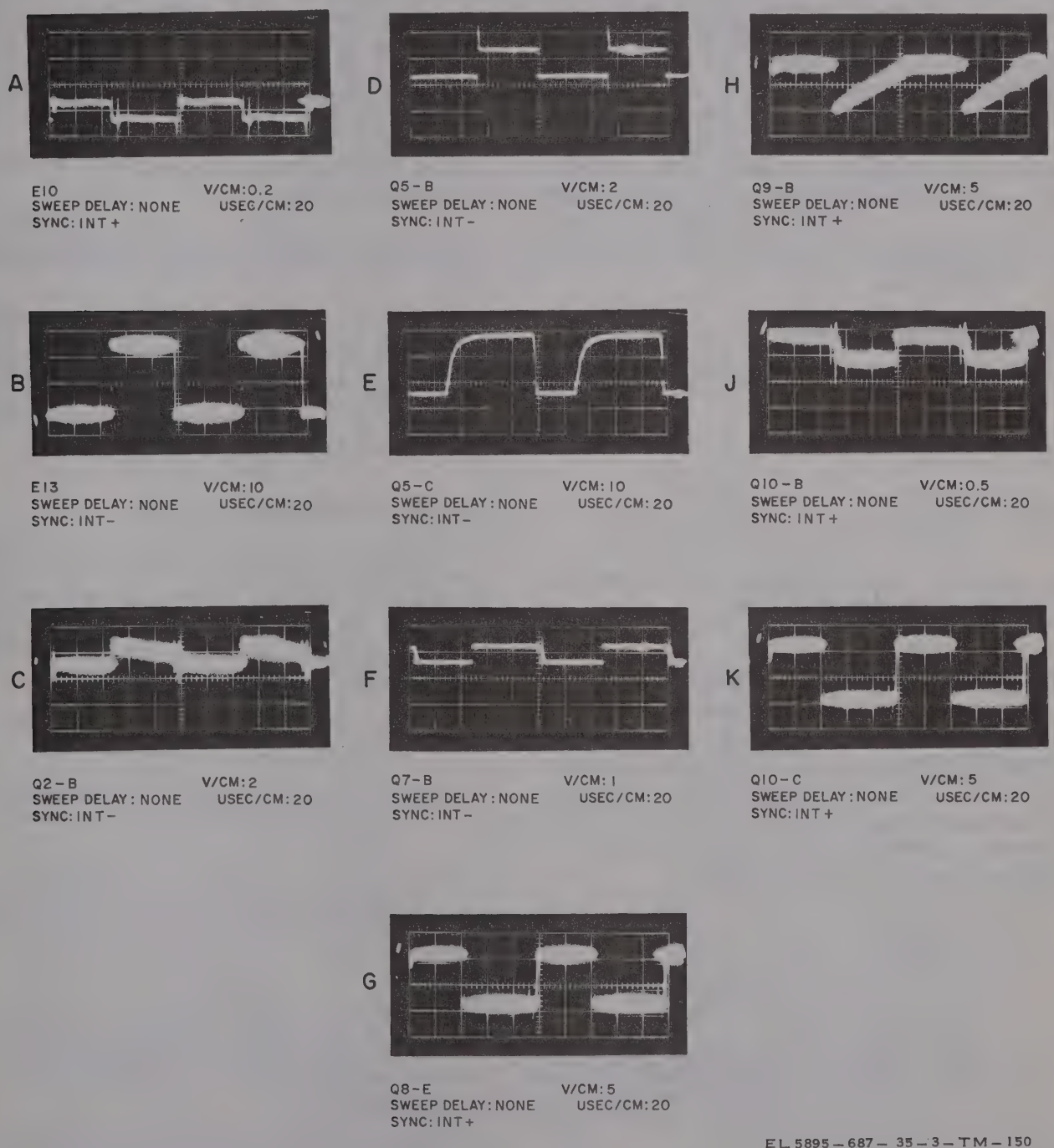


Figure 20–15. +12-volt regulator card 1A2A3A1 waveforms.

Section XVIII. +5-VOLT REGULATOR CARD 1A2A3A2 TROUBLESHOOTING AND REPAIR

20–126. General

This section presents specific troubleshooting and testing information for +5-volt regulator card 1A2A3A2. For troubleshooting, paragraph 20–127 lists helpful data located in other parts of this manual, and paragraphs 20–128, 20–129, and 20–130 provide a troubleshooting procedure which isolates any trouble to a stage or part. For adjustment and testing after repair, paragraph 20–131 references the applicable adjustment procedure, and paragraph 20–132 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–133 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–16 shows the card waveforms which are of significance in troubleshooting and testing.

20–127. Reference Data

The data listed in the following chart will be helpful when troubleshooting the +5-volt regulator card:

Reference	*Data*
Para 9–3 -----	+5 Volt regulator functioning.
Fig. 24–37 ---	+5-Volt regulator card 1A2A3A2 schematic diagram.

20–128. Test Equipment Required

a. If the +5-volt regulator card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Oscilloscope.

(3) Radar test set (only to supply "0" TRIGGER output to 1J1).

(4) Test facilities set (only for cables W32, W41, W42, and W47).

(5) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–129. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output of +28 volts.

20–130. Troubleshooting Chart

a. Preliminary Procedure. With the +5-volt regulator card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–129*b*, proceed as follows:

(1) At the synchronizer, check that the POWER circuit breaker is at OFF.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. +5-Volt Regulator Card 1A2A3A2 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	POWER circuit breaker 1A2CB1 (Set to ON.)	None	Remains at ON	If normal, leave 1A2CB1 at ON and proceed with step 12. If 1A2CB1 trips to OFF, turn 1A2A3A2R23 fully counterclockwise and repeat this step. If 1A2CB1 trips to OFF, remove interface module 1A2A1, coder-decoder module 1A2A2, and timing module 1A2A4 for their protection. Then ground 1A2A3A2Q4–B and proceed with step 2.
2	1A2CB1 (Set to ON.)	None	Remains at ON	*a.* If normal, prepare for step 6 as follows, and then proceed with step 6: (1) Set 1A2CB1 to OFF. (2) Remove the ground from Q4–B. (3) Connect a 9100-ohm (5-percent, half-watt) resistor between E6 and Q5–B (upper end of R8). *b.* If 1A2CB1 trips to OFF, prepare for step 3 as follows, and then proceed with step 3: (1) Turn off the processor and receiver-transmitter by setting their POWER circuit breakers to OFF. (2) At 28-volt dc power supply, reduce primary power voltage to zero (or minimum). (3) Leave Q4–B grounded. (4) Set 1A2CB1 to ON.
3	1A2A3A2E6	Multimeter (Slowly increases primary power voltage at 28-volt dc power supply, observing voltage at E6 and ammeter reading on 28-volt dc power supply. Stop in-	Voltage at E6 reaches +5 volts before ammeter reading reaches 2.5 amperes, and 1A2CB1 does not trip to OFF.	*a.* If normal, proceed with step 4. *b.* If ammeter reading on 28-volt dc power supply reaches 2.5 amperes, check C1, Q1, and the flywheel circuit associated with Q1.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
		creasing primary power voltage when voltage at E6 reaches +5 volts, or when ammeter reading reaches 2.5 amperes, or when 1A2CB1 trips to OFF, whichever occurs first).		*c.* If 1A2CB1 trips to OFF, check Q3 and associated parts, including VR1.
4	1A2A3A2E8 and 1A2A3A2Q4–C.	Multimeter (Measure voltage between test points).	0.5 volt or less between E8 and Q4–C when Q4–B is grounded.	If abnormal, check Q4. If normal, prepare for step 5 as follows, and then proceed with step 5: *a.* Set 1A2CB1 to OFF. *b.* Disconnect Q1C from E8 by unsoldering the corresponding wire from E8. *c.* Set 1A2CB1 to ON. (Leave Q4–B grounded).
5	1A2A3A2E6 -------	Multimeter --------	Less than 1.0 volt at E6 when Q4–B is grounded.	If normal, check Q1. If abnormal, check Q2 and associated parts.
6	1A2CB1 (Set to ON.)	None ----------	Remains at ON ----------	If normal, proceed with step 7. If 1A2CB1 trips to OFF, check Q5, R7, and R8.
7	1A2A3A2E6 -------	Multimeter --------	+4.5 to +5.0 volts at E6 with suitable value of resistance between E6 and Q5–B.	If normal, proceed with step 8. If less than +4.5 volts, proceed as follows: *a.* Set 1A2CB1 to OFF. *b.* Disconnect the 9100-ohm resistor from E6 and Q5–B, and substitute a 10,000-ohm resistor between the same points. *c.* Set 1A2CB1 to ON. *d.* If voltage at E6 is still less than +4.5 volts, repeat *a*, *b*, and *c* to substitute successively higher (5 percent) values of 11,000 ohms, 12,000 ohms, 13,000 ohms, etc., until +4.5 to +5.0 volts is obtained. Then leave 1A2CB1 at ON and proceed with step 8.
8	1A2A3A2Q6–B -----	Oscilloscope --------	Waveform F, fig. 20–16 ------	If normal, or if waveform can be made normal by ad-

Step No.	Test point	Test equipment	Normal indication	Corrective measures
				justment of R23, check Q6. If abnormal at all settings of R23, proceed with step 9.
9	1A2A3A2Q8–B	Oscilloscope	Waveform H, fig. 20–16	If normal, or if waveform can be made normal by adjustment of R23, check Q6 and associated parts, including CR8. If abnormal at all settings of R23, proceed with step 10.
10	1A2A3A2Q11–B	Multimeter	+3.5 to +4.5 volts, and varies with adjustment of R23.	If normal, proceed with step 11. If abnormal, check Q12 and associated parts.
11	1A2A3A2Q9–C	Oscilloscope	Waveform K, fig. 20–16	If no waveform, check Q9, Q10, and associated parts. If negative-going portions of waveform are too narrow at all settings of R23, check Q8, Q9, CR9, and R11. If the positive-going risetimes are too long, check Q7. If the negative-going portions are too wide, check Q11.
12	1A2A3A2E6	Multimeter	+0.5 ± 0.1 volts	If normal, or if voltage can be made normal by adjustment of R23, proceed with step 19. If abnormal, compare with voltage at E7. If difference is 2 volts or higher, check L1. If difference is less than 2 volts, prepare for step 13 as follows, and then proceed with step 13: *a.* Set 1A2CB1 to OFF. *b.* Turn R23 fully counterclockwise. *c.* Remove interface module 1A2A1, coder-decoder module 1A2A2, and timing module 1A2A4. *d.* Set 1A2CB1 to ON.
13	1A2A3A2E6	Multimeter	+5.0 ± 0.1 volts	If normal, or if voltage can be made normal by adjustment of R23, check Q1. If abnormal at all settings of R23, proceed with step 14.
14	1A2A3A2Q4–C	Multimeter	+3 volts or lower	If normal, check Q2 and associated parts. If abnormal, proceed with step 15.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
15	1A2A3A2Q4–B	Multimeter	+2.5 volts or higher	If normal, check Q4, CR5, CR6, and CR7. If abnormal, note the change in voltage, if any, when Q6–E (or CR5–K) is grounded. If the voltage at Q4–B does not decrease by more than 0.5 volt when Q6–E is grounded, check Q5, R7, R8, and CR6. If voltage does decrease by more than 0.5 volt when Q6–E is grounded, prepare for step 16 as follows, and then proceed with step 16: *a.* Set 1A2CB1 to OFF. *b.* Ground Q6–B (or CR8–A). *c.* Connect a 9100-ohm (5-percent, half watt) resistor between E6 and Q5–B (upper end of R8). *d.* Set 1A2CB1 to ON. If 1A2CB1 trips to OFF, do not contiinue with step 16; check Q5, R7, and R8.
16	1A2A3A2E6	Multimeter	+4.5 to +5.0 volts at E6 with suitable value of resistance between E6 and Q5–B.	If normal, proceed with step 17. If less than +4.5 volts, proceed as follows: *a.* Set 1A2CB1 to OFF. *b.* Disconnect the 9100-ohm resistor from E6 and Q5–B, and substitute a 10,000-ohm resistor between the same points. *c.* Set 1A2CB1 to ON. *d.* If voltage at E6 is still less than +4.5 volts, repeat *a*, *b*, and *c* to substitute successively higher (5 percent) values of 11,000 ohms, 12,000 ohms, 13,000 ohms, etc., until +4.5 to +5.0 volts is obtained. Then leave 1A2CB1 at ON and proceed with step 17. If +4.5 to +5.0 volts cannot be obtained with a resistance of 24,000 ohms or lower, do not continue; check Q6, CR6, CR7, and R10.
17	1A2A3A2Q11–B	Multimeter	+3.5 to +4.5 volts, and varies with adjustment of R23.	If normal, proceed with step 18. If abnormal, check Q12 and associated parts.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
18	1A2A3A2Q9–C	Oscilloscope	Waveform K, fig. 20–16	If normal, or if waveform can be made normal by adjustment of R23, check Q6 and associated parts, including CR8. If negative-going portions of waveform are too narrow at all settings of R23, check Q8, Q9, CR9, and R11. If the positive-going risetimes are too long, check Q7. If the negative-going portions are too wide, check Q11. If no waveform, check Q9, Q10, and associated parts.
19	1A2A3A2E6	Oscilloscope	Waveform A, fig. 20–16	If ripple is excessive, check the flywheel circuit associated with Q1.

20–131. Adjustment

The single potentiometer on the +5-volt regulator card is +5 volt adjustment potentiometer 1A2A3A2R23, which is adjusted for an output of +5 volts. The adjustment procedure is given in paragraphs 18–10 and 18–12.

20–132. Test Procedure

a. The test procedure for the +5-volt regulator card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the +5-volt regulator card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–133. Then prepare a hot mockup as for troubleshooting (paras 20–128 and 20–129) and perform the preliminary procedure given in paragraph 20–130*a*, but do not continue with the troubleshooting chart. Instead, proceed as follows:

(1) Set POWER circuit breaker 1A2CB1 to ON.

(2) Measure the dc voltage at 1A2A3A2E6. The voltage should be +5 ±0.15 volts. While observing this voltage, vary the output voltage of the 28-volt dc power supply throughout the range from 22 to 32 volts. The voltage at 1A2A3A2E6 should remain within tolerance over the entire range.

(3) Readjust the 28-volt dc power supply for an output voltage of 28 volts.

(4) At the synchronizer, use the oscilloscope to observe the ripple waveform at 1A2A3A2E6 (A, fig. 20–16).

(5) Set 1A2CB1 to OFF, and remove interface module 1A2A1, coder-decoder module 1A2A2, timing module 1A2A4, and −12-volt inverter card 1A2A3A3.

(6) Set 1A2CB1 to ON, and note that it does not trip to OFF.

(7) Measure the dc voltage at 1A2A3A2E6. With 1A2A3A3 removed, the voltage should be less than +1.2 volt.

(8) Set 1A2CB1 to OFF, reinstall 1A2A3A3, and set 1A2CB1 back to ON.

(9) Momentarily ground 1A2A3A3J1. This should trip 1A2CB1 to OFF.

(10) With 1A2CB1 at OFF, unground 1A2A3AJ1 and reinstall 1A2A1, 1A2A2, and 1A2A4.

20-133. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating +5-volt regulator card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20-128 and 20-129). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20-130*a*), except that the synchronizer POWER circuit breaker was set to ON.

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 6, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 6, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 6, and the negative probe was touched to each of the listed pins.

b. +5-volt Regulator Card 1A2A3A2 Etched Connector Pin Voltage and Regulator Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	Not used				
2	Not used				
3	0.15	RX100	1800	RX100	1800
4	0.15	RX100	1800	RX100	1800
5	0.0	RX1	0.0	RX1	0.0
6	0.0	RX1	0.0	RX1	0.0
7	0.0	RX1	0.0	RX1	0.0
8	0.0	RX1	0.0	RX1	0.0
9	0.0	RX1	0.0	RX1	0.0
10	0.0	RX1	0.0	RX1	0.0
11	5.1	RX100	1850	RX100	360
12	5.1	RX100	1850	RX100	360
13	5.1	RX100	1850	RX100	360
14	5.1	RX100	1850	RX100	360
15	5.1	RX100	1850	RX100	360
16	5.1	RX100	1850	RX100	360

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
17	Not used				
18	Not used				
19	—12.0	RX100	1100	RX100	2000
20	—12.0	RX100	1100	RX100	2000
21	Not used				
22	Not used				
23	Not used				
24	Not used				
25	Not used				
26	Not used				
27	Not used				
28	Not used				
29	4.9	RX100	1400	RX100	1500
30	4.9	RX100	1400	RX100	1500
31	Not used				
32	Not used				
33	12.5	RX100	2200	RX100	1250
34	12.5	RX100	2200	RX100	1250
35	12.5	RX100	2200	RX100	1250
36	12.5	RX100	2200	RX100	1250
37	Not used				
38	Not used				
39	Not used				
40	Not used				
41	0.0	RX100	850	RX100	900
42	0.0	RX100	850	RX100	900
43	Not used				
44	Not used				

20-134. Waveforms
(fig. 20-16)

Figure 20-16 shows the +5-volt regulator card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-128, 20-129 and 20-130*a*), except that the synchronizer POWER circuit breaker was set to ON.

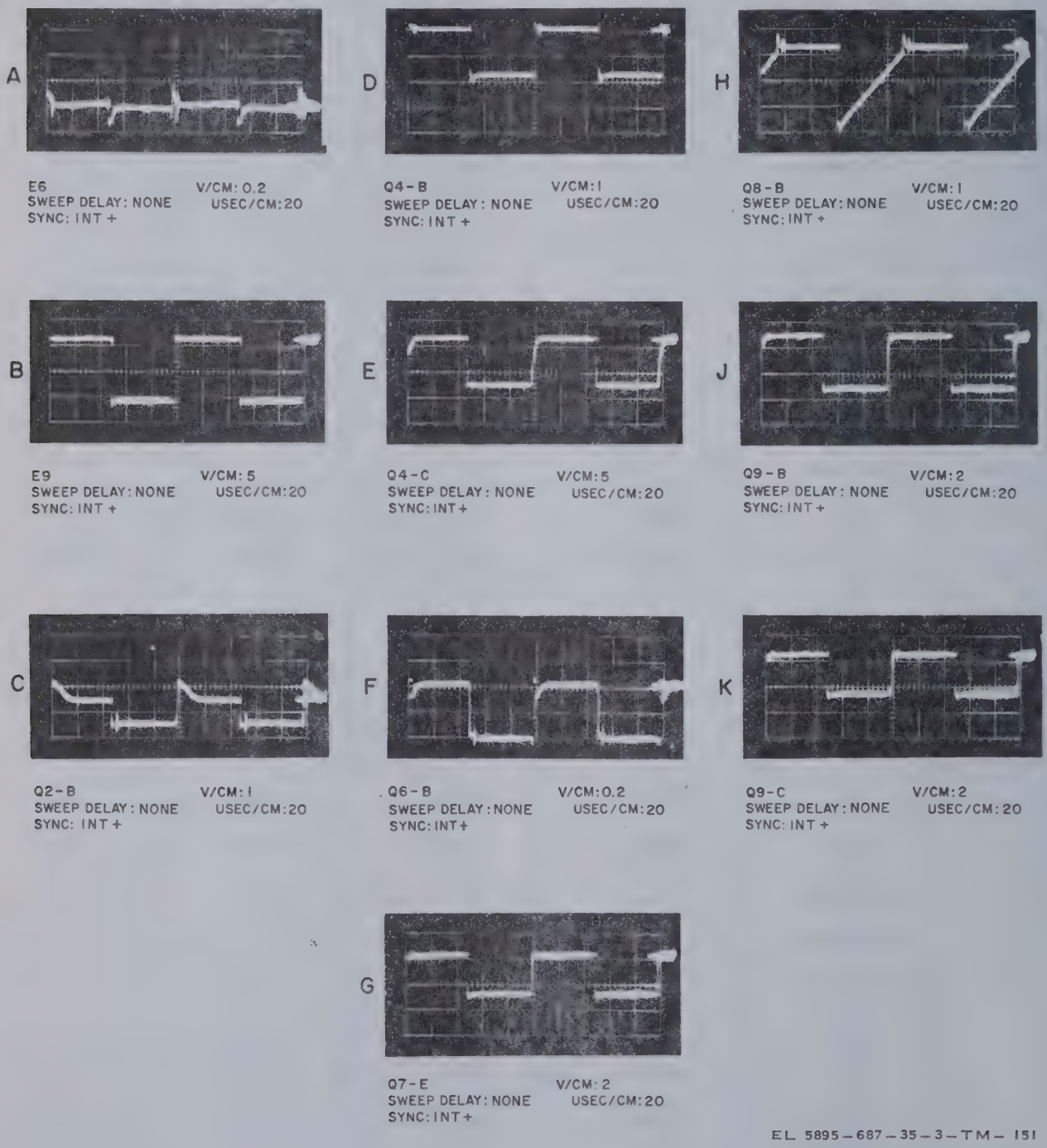


Figure 20-16. +5-volt regulator card 1A2A3A2 waveforms.

Section XIX. −12-VOLT INVERTER CARD 1A2A3A3 TROUBLESHOOTING AND REPAIR

20–135. General

This section presents specific troubleshooting and testing information for −12-volt inverter card 1A2A3A3. For troubleshooting, paragraph 20–136 lists helpful data located in other parts of this manual, and paragraphs 20–137, 20–138 and 20–139 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–141 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–142 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–17 shows the card waveforms which are of significance in troubleshooting and testing.

20–136. Reference Data

The data listed in the following chart will be helpful when troubleshooting the −12-volt inverter card.

Reference	*Data*
Para 9–4 -----	−12-volt inverter functioning.
Fig. 24–38 ---	−12-volt inverter card 1A2A3A3 schematic diagram.

20–137. Test Equipment Required

a. If the −12-volt inverter card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Oscilloscope.

(3) Radar test set (only to supply "0" TRIGGER output to 1J1).

(4) Test facilities set (only for cables W32, W41, W42, and W47).

(5) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–138. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group cause by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output of 28 volts.

20–139. Troubleshooting Chart

a. Preliminary Procedure. With the −12-volt inverter card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–138*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to OFF.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the indications at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. —12-volt Inverter Card 1A2A3A3 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	POWER circuit breaker 1A2CB1 (Set to ON.)	None	Remains at ON	If normal, leave 1A2CB1 at ON and proceed with step 10. If 1A2CB1 trips to OFF, remove interface module 1A2A1 and coder-decoder module 1A2A2 for their protection. Then remove +5-volt regulator card 1A2A3A2 and proceed with step 2.
2	1A2CB1 (Set to ON.)	None	Remains at ON with all cards except 1A2A3A1 and 1A2A3A3 removed.	If normal, leave 1A2CB1 at ON and proceed with step 8. If 1A2CB1 trips to OFF, prepare for step 3 as follows, and then proceed with step 3: *a.* Turn off the processor and the receiver-transmitter by setting their POWER circuit breakers to OFF. *b.* Reduce the primary power voltage from the 28-volt dc power supply to zero (or minimum). *c.* Ground 1A2A3A3J4 with a jumper wire. *d.* Set 1A2CB1 to ON.
3	1A2A3A1E10 and 1A2A3A3J2.	Multimeter (Measure voltage between test points. Slowly increase primary power voltage until one of the following indications is obtained (whichever occurs first): a. Voltage between test points reaches 4.1 volts. b. Current reading on 28-volt dc power supply reaches 2.0 amperes. c. 1A2CB1 trips to OFF.	Primary power voltage reaches 28 volts before voltage between test points reaches 4.1 volts and before the current reading on the 28-volt dc power supply reaches 2.0 amperes, and 1A2CB1 does not trip to OFF.	*a.* If normal, leave primary voltage at 28 volts and proceed with step 6. *b.* If 1A2CB1 trips to OFF, check Q3. *c.* If voltage between test points reaches 4.1 volts, leave the primary power voltage at its existing value and proceed with step 4.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
4	1A2A2A2Q1-C	Oscilloscope	Waveform D, fig. 20-17 (will not be normal in this step; use a lower vernier VOLTS / DIV control setting (higher sensitivity) at the oscilloscope, if necessary.	If a waveform cannot be obtained at all, or if the waveform obtained is similar to the waveform at 1A2A3A3J2, check Q1, Q2, and associated parts, including C1 and T1. If the waveform obtained is greater in amplitude than the waveform at J2, prepare for step 5 as follows, and then proceed with step 5: *a.* Set 1A2CB1 to OFF. *b.* Disconnect CR5 and CR6 from T1 by unsoldering their cathode (upper) leads. *c.* Set 1A2CB1 to ON.
5	Same as for step 3	Same as for step 3	Same as for step 3	*a.* If normal, check CR5, CR6, C2, and C3. *b.* If 1A2CB1 trips to OFF, check Q3. *c.* If voltage between test points reaches 4.1 volts, check Q1, Q2, and associated parts, including C1 and T1.
6	1A2A3A3J3	Multimeter	—12 ± 1 volts	If normal, proceed with step 7. If abnormal, check CR5 and CR6.
7	1A2A3A3-40	Multimeter	+0.5 to +2.0 volts	If normal, check Q3 and associated parts, including C4 and R4. If abnormal, check VR1.
8	1A2A3A3Q1-C	Oscilloscope	Waveform D, fig. 20-17	If abnormal, check Q1, Q2, and associated parts, including T1. If normal, prepare for step 9 as follows, and then proceed with step 9: *a.* Set 1A2CB1 to OFF. *b.* Reinstall 1A2A1 and 1A2A2, but leave 1A2A3A2 removed. *c.* Ground 1A2A3A3J4 with a jumper wire. *d.* Set 1A2CB1 to ON.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
9	1A2A3A3Q1-C	Oscilloscope	Waveform D, fig. 20-17	If normal, check CR5 and CR6. If abnormal, check Q1, Q2, and associated parts, including T1.
10	1A2A3A3J3	Multimeter	−12 ±1 volts	If normal, proceed with step 12. If abnormal, proceed with step 11.
11	1A2A3A3Q1-C	Oscilloscope	Waveform D, fig. 20-17	If normal, check CR5 and CR6. If abnormal, check Q1, Q2 and associated parts including T1.
12	1A2A3A3J3	Oscilloscope	Waveform B, fig. 20-17	If abnormal (excessive ripple), check CR5, CR6, C2, and C3. If normal, proceed with step 13.
13	1A2A3A3J1	Oscilloscope	Waveform A, fig. 20-17 (10-kc triggers).	If abnormal, check Q4 and associated parts.

20-140. Adjustment

The output of the −12-volt inverter card is not independently adjustable, but it varies directly with the output of +12-volt regulator card 1A2A3A1 when +12-volt adjustment potentiometer 1A2A3A1R27 is adjusted. Therefore, if the output of a repaired −12-volt inverter is slightly out of tolerance when the +12-volt adjustment is made as directed in paragraph 18-11, it is usually possible to find a compromise setting of 1A2A3A1R27 at which the +12-volt and −12-volt power supply voltages are both within their respective tolerances.

20-141. Test Procedure

a. The test procedure for the −12-volt inverter card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the 12-volt inverter card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-142. Then prepare a hot mockup as for troubleshooting (paras 20-137 and 20-138) and perform the preliminary procedure given in paragraph 20-139*a*, but do not continue with the troubleshooting chart. Instead, proceed as follows:

(1) Set POWER circuit breaker 1A2CB1 to ON.

(2) Measure the dc voltage at 1A2A3A3J3. The voltage should be −12 ±1.0 volts.

(3) Use the oscilloscope to observe the ripple waveform at 1A2A3A3J3 (B, fig. 20-17).

(4) Use the oscilloscope to observe the 10-kc triggers at 1A2A3A3J1 (A, fig. 20-17).

(5) Use the oscilloscope to check the dc voltage at 1A2A3A3J4. This voltage should be +0.5 to +2.0 volts when not externally loaded.

(6) Set 1A2CB1 to OFF and remove interface module 1A2A1, coder-decoder module 1A2A2, timing module 1A2A4, and +5-volt regulator card 1A2A3A2.

(7) Temporarily ground 1A2A3A3J3 with a jumper wire.

(8) Set 1A2CB1 to ON for not longer than 2 seconds. Within that period of time, it should trip to OFF.

(9) With 1A2CB1 at OFF, unground 1A2A3A3J3 and reinstall 1A2A1, 1A2A2, 1A2A4, and 1A2A3A2.

20–142. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating −12-volt inverter card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20–137 and 20–138). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–139*a*), except that the synchronizer POWER circuit breaker was set to ON.

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 30, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 30, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 30, and the negative probe was touched to each of the listed pins.

b. −12-Volt Inverter Card 1A2A3A3 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	Not used				
2	Not used				
3	Not used				
4	Not used				
5	0.15	RX100	1600	RX100	900
6	0.15	RX100	1600	RX100	900
7	12.0	RX100	600	RX100	700
8	12.0	RX100	600	RX100	700
9	12.0	RX100	600	RX100	700
10	12.0	RX100	600	RX100	700
11	Not used				
12	Not used				
13	Not used				
14	Not used				
15	Not used				
16	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
17	Not used				
18	Not used				
19	Not used				
20	Not used				
21	Not used				
22	Not used				
23	Not used				
24	Not used				
25	Not used				
26	Not used				
27	Not used				
28	Not used				
29	0.0	RX1	0.0	RX1	0.0
30	0.0	RX1	0.0	RX1	0.0
31	0.0	RX1	0.0	RX1	0.0
32	0.0	RX1	0.0	RX1	0.0
33	Not used				
34	Not used				
35	—12.0	RX100	550	RX10,000	3 Mego
36	—12.0	RX100	550	RX10,000	3 Mego
37	—12.0	RX100	550	RX10,000	3 Mego
38	—12.0	RX100	550	RX10,000	3 Mego
39	Not used				
40	1.57	RX10,000	55K	RX10,000	90K
41	0.16	RX1	80	RX1	80
42	Not used				
43	12.5	RX100	5500	RX100	5300
44	Not used				

20-143. Waveforms
(fig. 20-17)

Figure 20-17 shows the −12-volt inverter card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-137, 20-138, and 20-139*a*), except that the synchronizer POWER circuit breaker was set to ON.

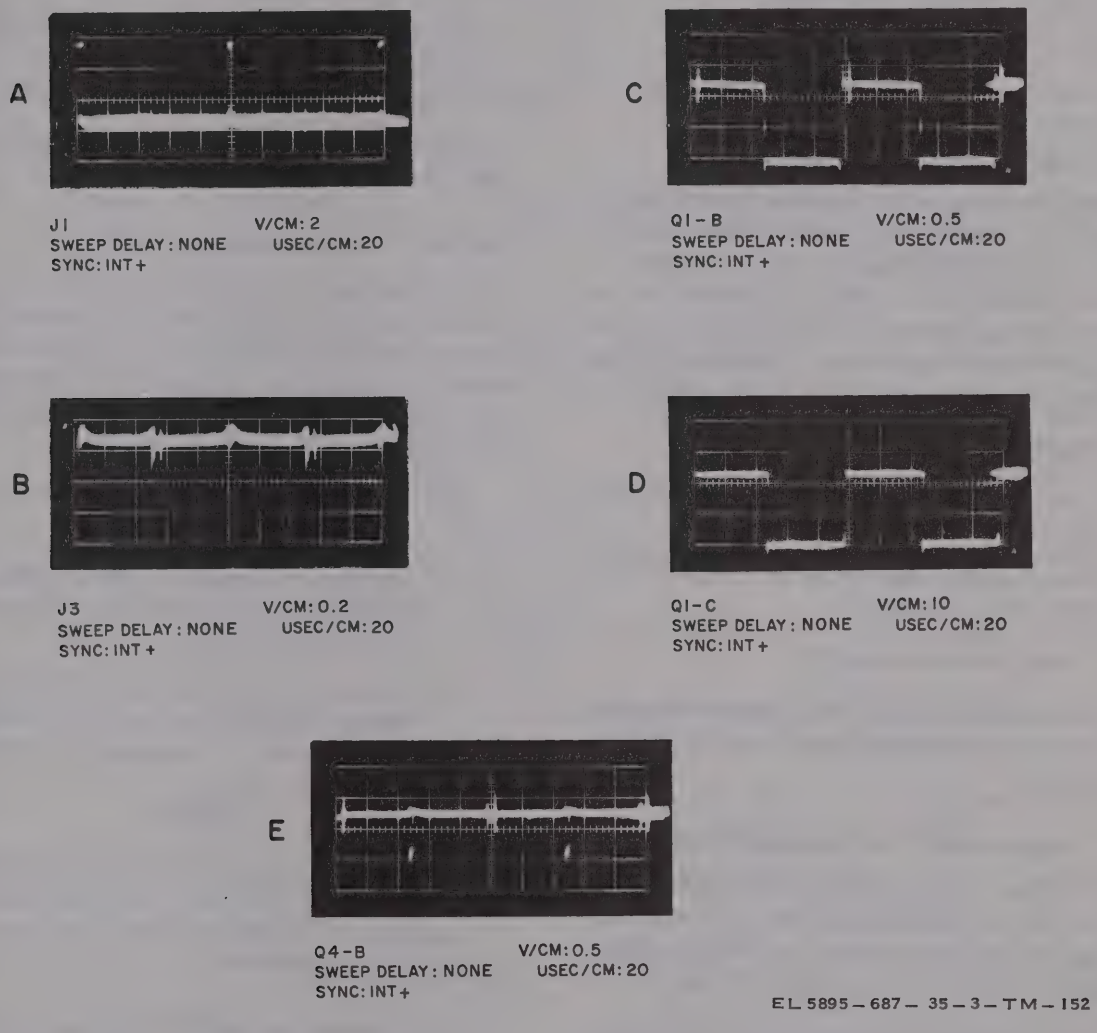


Figure 20-17. —12-volt inverter card 1A2A3A3 waveforms.

Section XX. 10-MC CLOCK AND COUNTER A CARD 1A2A4A1 TROUBLESHOOTING AND REPAIR

20-144. General

This section presents specific troubleshooting and testing information for 10-mc clock and counter A card 1A2A4A1. For troubleshooting, paragraph 20-145 lists helpful data located in other parts of this manual, and paragraphs 20-146, 20-147 and 20-148 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20-149 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20-150 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20-18 shows the card waveforms which are of significance in troubleshooting and testing.

20–145. Reference Data

The data listed in the following chart will be helpful when troubleshooting the 10-mc clock and counter A card:

Reference	*Data*
Para 4–2 ----	Pretrigger generation.
Fig. 24–40 ---	10-mc clock and counter A card 1A2A4A1 schematic diagram.

20–146. Test Equipment Required

a. If the 10-mc clock and counter A card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Oscilloscope.

(2) Radar test set (only to supply "0" TRIGGER output to 1J1).

(3) Test facilities set (only for cables W32, W41, W42, and W47).

(4) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–147. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output voltage of 28 volts.

20–148. Troubleshooting Chart

a. Preliminary Procedure. With the 10-mc clock and counter A card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–174*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. 10-Mc Clock and Counter A Card 1A2A4A1 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 17 ----------	Oscilloscope --------	Processor start pretrigger (J, fig. 20–18).	If normal, proceed with step 21. If abnormal, proceed with step 2.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
2	J1-9	Oscilloscope	2^4 (G, fig. 20-18)	If normal, proceed with step 13. If abnormal, proceed with step 3.
3	J1-3	Oscilloscope	10-mc clock (same as L, fig. 20-18).	If normal, proceed with step 6. If abnormal, proceed with step 4.
4	J1-2	Oscilloscope	$\overline{\text{10-mc clock}}$ (B, fig. 20-18)	If normal, inverter A4A is defective. If abnormal, proceed with step 5.
5	J1-1	Oscilloscope	10-mc oscillator (A, fig. 20-18).	If normal, buffer stage Q2 is defective. If abnormal, oscillator stage Q1 or crystal Y1 is defective.
6	J1-5	Oscilloscope	Reset 2 (same as F, fig. 20-18, except inverted).	At this point, only the leading edge is important. If the leading edge is abnormal, flip-flop A2B is defective. If the leading edge is normal, proceed with step 7.
7	J1-8	Oscilloscope	$\overline{\text{Reset 2}}$ (F, fig. 20-18)	If abnormal, inverter A1A is defective.
8	Pin 37	Oscilloscope	$\overline{\text{Reset 2}}$ (same as F, fig. 20-18).	If abnormal, inverter A1B is defective.
9	J1-7	Oscilloscope	2^0 (E, fig. 20-18)	If abnormal, flip-flop A2A is defective.
10	J1-6	Oscilloscope	2^3 (D, fig. 20-18)	If abnormal, flip-flop A3 is defective.
11	A4-8	Oscilloscope	(Continuously high)	If abnormal, inverter A4C is defective.
12	J1-4	Oscilloscope	2^2 (C, fig. 20-18)	If abnormal, flip-flop A5 is defective. If normal, flip-flop A6 is defective.
13	Pin 41	Oscilloscope	2^1 (same as H, fig. 20-18)	If abnormal, inverter A4D is defective.
14	Pin 32	Oscilloscope	$\overline{2^5}$ (same as F, fig. 20-19 except inverted).	If abnormal, isolate to A8B or A9A.
15	Pin 33	Oscilloscope	$\overline{2^6}$ (same as B, fig. 20-19, except inverted).	If abnormal, isolate to A8B or A9A.
16	Pin 35	Oscilloscope	$\overline{2^7}$ (same as G, fig. 20-19)	If abnormal, isolate to A8B or A9A.
17	Pin 14	Oscilloscope	$\overline{2^9}$ (same as E, fig. 20-19, except inverted).	If abnormal, A7 is defective.
18	Pin 16	Oscilloscope	$\overline{2^{10}}$ (same as D, fig. 20-19, except inverted).	If abnormal, A7 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
19	Pin 18	Oscilloscope	$\overline{2^{11}}$ (same as J, fig. 20-19, except inverted).	If abnormal, A7 is defective.
20	Pin 26	Oscilloscope	$\overline{2^{13}}$ (same as H, fig. 20-19)	If abnormal, isolate to A2B or A7A. If normal, A7A or A9 is defective.
21	Pin 20	Oscilloscope	$\overline{\text{Mode 4 pretrigger}}$ (K, fig. 20-18).	If abnormal, A7B or A8 is defective.
22	Pin 22	Oscilloscope	10-mc clock (L, fig. 20-18)	If abnormal, inverter A4B is defective.
23	Pin 43	Oscilloscope	$\overline{2^{3}}$ (same as D, fig. 20-18, except inverted).	If abnormal, flip-flop A3A is defective.
24	J1-5	Oscilloscope	Reset 2 (same as F, fig. 20-18, except inverted).	At this point, only the trailing edge is important. If abnormal, flip-flop A2B is defective.
			STEPS 25 THROUGH 29 CHECK THE DIRECT RESET CAPABILITIES OF THE FLIP-FLOPS COMPRISING THE COUNTER. IN EACH CASE THE TEST POINT SHOULD GO LOW WHEN J1-8 GOES LOW AND SHOULD STAY LOW AS LONG AS J1-8 STAYS LOW.	
25	J1-7	Oscilloscope	See Note above	If abnormal, flip-flop A2A is defective.
26	J1-10	Oscilloscope	See Note above	If abnormal, flip-flop A3B is defective.
27	J1-6	Oscilloscope	See Note above	If abnormal, flip-flop A3A is defective.
28	J1-4	Oscilloscope	See Note above	If abnormal, flip-flop A5 is defective.
29	J1-9	Oscilloscope	See Note above	If abnormal, flip-flop A6 is defective.

20-149. Test Procedure

a. The test procedure for the 10-mc clock and counter A card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the 10-mc clock and counter A card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph

20–150. Then prepare a hot mockup as for troubleshooting (paras 20–146 and 20–147) and perform the preliminary procedure given in paragraph 20–148*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order:

(1) 1A2A4A1-17, $\overline{\text{processor start pretrigger}}$ (J, fig. 20–18).

(2) 1A2A4A1–20, $\overline{\text{mode 4 pretrigger}}$ (K, fig. 20–18).

(3) 1A2A4A1–22, $\overline{\text{10-mc clock}}$ (L, fig. 20–18).

(4) 1A2A4A1–37, $\overline{\text{reset 2}}$ (same as F, fig. 20–18).

20–150. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating 10-mc clock and counter A card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting (paras 20–146 and 20–147). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–148*a*).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

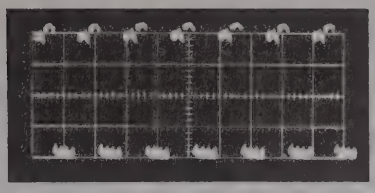
b. 10-Mc Clock and Counter A Card 1A2A4A1 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	940	RX100	350
4	5.0	RX100	940	RX100	350
5	Not used				
6	Not used				
7	Not used				
8	Not used				
9	Not used				
10	Not used				
11	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
12	Not used				
13	Not used				
14	3.3	RX10,000	500K	RX100	3300
15	Not used				
16	3.3	RX10,000	500K	RX100	3300
17	5.0	RX100	3200	RX100	730
18	3.3	RX10,000	44K	RX100	3300
19	3.3	RX10,000	44K	RX100	4000
20	5.0	RX100	3200	RX100	700
21	Not used				
22	1.37	RX10,000	5 Mego	RX100	780
23	Not used				
24	3.8	RX10,000	700K	RX100	1200
25	Not used				
26	0.7	RX10,000	500K	RX100	900
27	Not used				
28	3.4	RX10,000	440K	RX100	700
29	Not used				
30	0.65	RX10,000	440K	RX100	700
31	Not used				
32	3.3	RX10,000	440K	RX100	3000
33	3.3	RX10,000	450K	RX100	3000
34	3.3	RX10,000	440K	RX100	3500
35	0.65	RX10,000	420K	RX100	3000
36	3.3	RX10,000	450K	RX100	700
37	1.22	RX10,000	400K	RX100	800
38	0.65	RX10,000	460K	RX100	700
39	0.65	RX10,000	430K	RX100	700
40	0.65	RX10,000	450K	RX100	3600

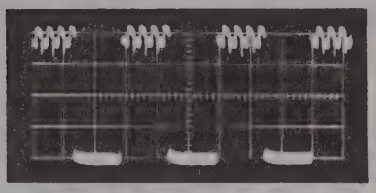
A

J1-1 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.1
SYNC: INT-



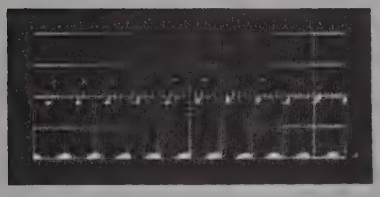
D

J1-6 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT +



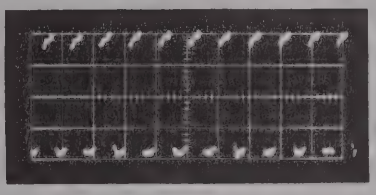
G

J1-9 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 1
SYNC: INT +



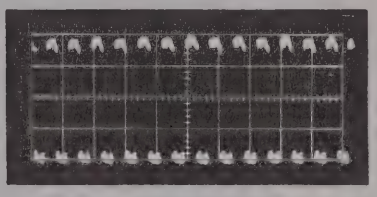
B

J1-2 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.1
SYNC: INT-



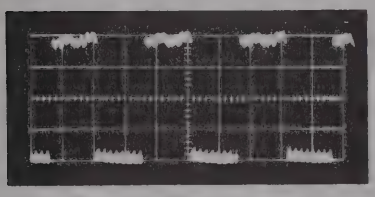
E

J1-7 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.2
SYNC: INT-



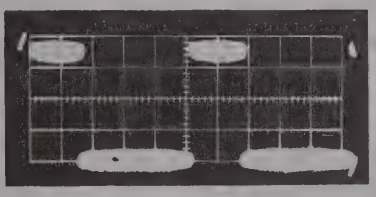
H

J1-10 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT +



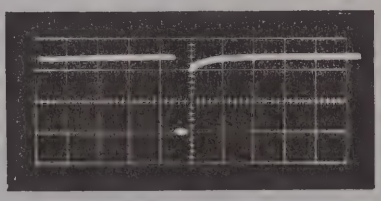
C

J1-4 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.5
SYNC: INT+



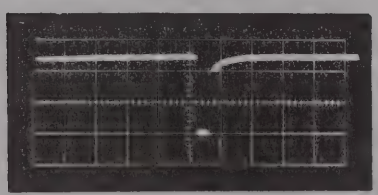
F

J1-8 V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 0.5
SYNC: INT +



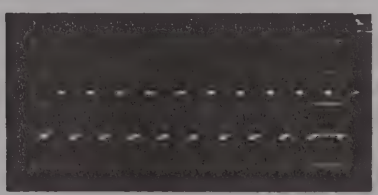
J

PIN 17 V/CM: 2
SWEEP DELAY: 448 USEC USEC/CM: 0.5
SYNC: EXT + (1J1)



K

PIN 20 V/CM: 2
SWEEP DELAY: 11 USEC USEC/CM: 0.5
SYNC: EXT + (1J1)



L

PIN 22 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 0.1
SYNC: INT +

EL 5895 - 687 - 35 - 3 - TM - 153

Figure 20-18. 10-mc clock and counter A card 1A2A4A1 waveforms.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
41	0.65	RX10,000	440K	RX100	750
42	5.0	RX100	940	RX100	350
43	3.4	RX10,000	540K	RX100	700
44	0.0	RX1	0.0	RX1	0.0

20–151. Waveforms
(fig. 20–18)

Figure 20–18 shows the 10-mc clock and counter A card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–146, 20–147 and 20–148*a*).

Section XXI. COUNTER B CARD 1A2A4A2 TROUBLESHOOTING AND REPAIR

20–152. General

This section presents specific troubleshooting and testing information for counter B card 1A2A4A2. For troubleshooting, paragraph 20–153 lists helpful data located in other parts of this manual, and paragraphs 20–154, 20–155 and 20–156 provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–157 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–158 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–19 shows the card waveforms which are of significance in troubleshooting and testing.

20–153. Reference Data

The data listed in the following chart will be helpful when troubleshooting the counter B card:

Reference	*Data*
Para 4–2 ----	Pretrigger generation.
Fig. 24–41 ---	Counter B card 1A2A4A2 schematic diagram.

20–154. Test Equipment Required

a. If the counter B card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Oscilloscope.

(3) Radar test set (only to supply "0" TRIGGER output to 1J1).

(4) Test facilities set (only for cables W32, W41, W42, and W47).

(5) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–155. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-

volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn on the 28-volt dc power supply and adjust it for an output voltage of 28 volts.

20–156. Troubleshooting Chart

a. Preliminary Procedure. With the counter B card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–155*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Counter B Card 1A2A4A2 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 25	Oscilloscope	$\overline{\text{Sif pretrigger}}$ (L, fig. 20–19)	If normal, proceed with step 11. If abnormal, proceed with step 2.
2	Pin 36	Oscilloscope	2^{12} (H, fig. 20–19)	If normal, proceed with step 10. If abnormal, proceed with step 3.
3	P1–A1	Oscilloscope	2^{4} (A, fig. 20–19)	If abnormal, inverter A6C is defective.
4	A6–3	Oscilloscope	(Continuously high)	If abnormal, inverter A6A is defective.
5	P1–A4	Oscilloscope	2^{6} (B, fig. 20–19)	If abnormal, flip-flop A1 is defective.
6	P1–B4	Oscilloscope	2^{7} (G, fig. 20–19)	If abnormal, flip-flop A5 is defective.
7	P1–A26	Oscilloscope	2^{5} (C, fig. 20–19)	If abnormal, flip-flop A9 is defective.
8	P1–2A8	Oscilloscope	2^{10} (D, fig. 20–19)	If abnormal, flip-flop A4 is defective.
9	P1–B30	Oscilloscope	2^{11} (J, fig. 20–19)	If abnormal, flip-flop A8 is defective. If normal, flip-flop A10 is defective.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
10	P1-B28	Oscilloscope	$\overline{2^{12}}$ (same as H, fig. 20-19, except inverted).	If abnormal, flip-flop A10 is defective. If normal, A2 or A7A is defective.
11	Pin 32	Oscilloscope	$\overline{\text{Self-test pretrigger}}$ (M, fig. 20-19).	If normal, proceed with step 14. If abnormal, proceed with step 12.
12	Pin 10	Oscilloscope	$\overline{2^{5}}$ (same as F, fig. 20-19, except inverted).	If abnormal, flip-flop A1A is defective.
13	P1-B29	Oscilloscope	$\overline{2^{9}}$ (same as E, fig. 20-19, except inverted).	If abnormal, flip-flop A4A is defective. If normal, A3 or A7B is defective.
14	Pin 16	Oscilloscope	$\overline{\text{Reshaped radar trigger}}$ (K, fig. 20-19).	If abnormal, inverter A6B is defective.
15	Pin 6	Oscilloscope	$\overline{\text{Reset 2}}$ (same as F, fig. 20-18).	If abnormal, isolate to A1, A4, A5, A8, A9 or A10.
16	Pin 20	Oscilloscope	$\overline{2^{8}}$ (same as C, fig. 20-19, except inverted).	If abnormal, flip-flop A9 is defective.
17	Pin 18	Oscilloscope	$\overline{2^{8}}$ (same as C, fig. 20-19)	If abnormal, inverter A6D is defective.
18	Pin 36	Oscilloscope	$\overline{2^{12}}$ (H, fig. 20-19)	If abnormal, flip-flop A10 is defective.
19	Pin 40	Oscilloscope	$\overline{2^{11}}$ (same as J, fig. 20-19, except inverted).	If abnormal, flip-flop A8 is defective.
20	Pin 38	Oscilloscope	$\overline{2^{10}}$ (same as D, fig. 20-19, except inverted).	If abnormal, flip-flop A4B is defective.
21	Pin 8	Oscilloscope	$\overline{2^{6}}$ (same as B, fig. 20-19, except inverted).	If abnormal, flip-flop A1B is defective.
			STEPS 22 THROUGH 29 CHECK THE DIRECT RESET CAPABILITIES OF THE FLIP-FLOPS COMPRISING THE COUNTER. IN EACH CASE THE TEST POINT SHOULD GO LOW WHEN PIN 6 GOES LOW AND SHOULD STAY LOW AS LONG AS PIN 6 STAYS LOW.	
22	P1-B1	Oscilloscope	See Note above	If abnormal, flip-flop A1A is defective.
23	P1-A4	Oscilloscope	See Note above	If abnormal, flip-flop A1B is defective.
24	P1-B4	Oscilloscope	See Note above	If abnormal, flip-flop A5 is defective.

b. Counter B Card 1A2A4A2 Troubleshooting Chart. (cont)

Step	Test point	Test equipment	Normal indication	Corrective measures
25	P1-A26	Oscilloscope	See Note above	If abnormal, flip-flop A9 is defective.
26	P1-A29	Oscilloscope	See Note above	If abnormal, flip-flop A4A is defective.
27	P1-A28	Oscilloscope	See Note above	If abnormal, flip-flop A4B is defective.
28	P1-B30	Oscilloscope	See Note above	If abnormal, flip-flop A8 is defective.
29	P1-B27	Oscilloscope	See Note above	If abnormal, flip-flop A10 is defective.

20-157. Test Procedure

a. The test procedure for the counter B card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the counter B card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20-158. Then prepare a hot mock-up as for troubleshooting (para 20-154 and 20-155 and perform the preliminary procedure given in paragraph 20-156*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following points in any convenient order.

(1) 1A2A4A2J1-A1, 2^4 (A, fig. 20-19)
(2) 1A2A4A2J1-A4, 2^6 (B, fig. 20-19)
(3) 1A2A4A2J1-A26, 2^8 (C, fig. 20-19)
(4) 1A2A4A2J1-A28, 2^{10} (D, fig. 20-19)
(5) 1A2A4A2J1-A29, 2^9 (E, fig. 20-19)
(6) 1A2A4A2J1-B1, 2^5 (F, fig. 20-19)
(7) 1A2A4A2J1-B4, 2^7 (G, fig. 20-19)
(8) 1A2A4A2J1-B27, 2^{12} (H, fig. 20-19)
(9) 1A2A4A2J1-B30, 2^{11} (J, fig. 20-19)
(10) 1A2A4A2-16, $\overline{\text{reshaped radar trigger}}$ (K, fig. 20-19)
(11) 1A2A4A2-25, $\overline{\text{sif pretrigger}}$ (L, fig 20-19)
(12) 1A2A4A2-32, $\overline{\text{self-test pretrigger}}$ (M, fig. 20-19)

20-158. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating counter B card.

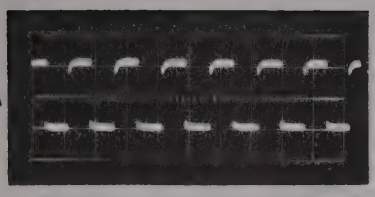
(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mock-up and prepared in the same way as for troubleshooting (para 20-154 and 20-155). The preliminary procedure used to turn on the hot mock-up iff set was also the same as for troubleshooting (para 20-156*a*).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of the multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the

card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

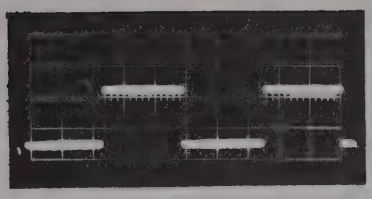
b. Counter B Card 1A2A4A2 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX100	1700	RX100	350
4	5.0	RX100	1700	RX100	350
5	Not used				
6	1.22	RX10,000	520K	RX100	1200
7	Not used				
8	3.3	RX10,000	600K	RX100	700
9	Not used				
10	3.3	RX10,000	600K	RX100	700
11	Not used				
12	0.65	RX10,000	540K	RX100	700
13	Not used				
14	0.1	RX10,000	680K	RX100	1800
15	Not used				
16	3.8	RX10,000	3 Mego	RX100	850
17	Not used				
18	0.65	RX10,000	60K	RX100	850
19	Not used				
20	3.3	RX10,000	600K	RX100	700
21	Not used				
22	3.3	RX10,000	550K	RX100	700
23	0.65	RX10,000	700K	RX100	4000
24	3.4	RX10,000	700K	RX100	1950



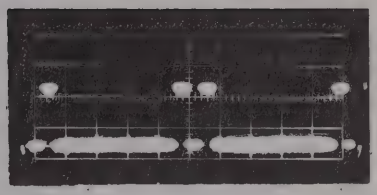
A

P1 - A1 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 2
SYNC: EXT + (IJI)



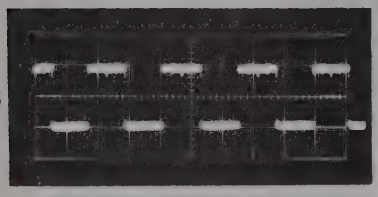
E

P1 - A29 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: EXT + (IJI)



J

P1 - B30 V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 0.5
SYNC: EXT + (IJI)

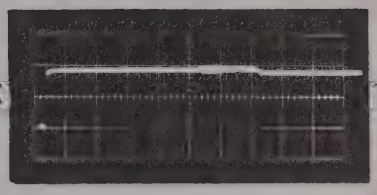


B

P1 - A4 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 5
SYNC: EXT + (IJI)

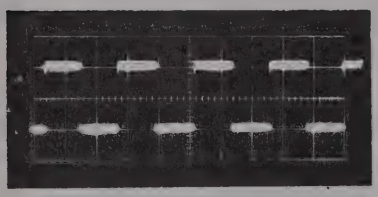
F

P1 - B1 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 5
SYNC: INT -



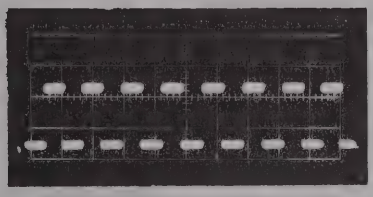
K

PIN 16 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 2
SYNC: INT -



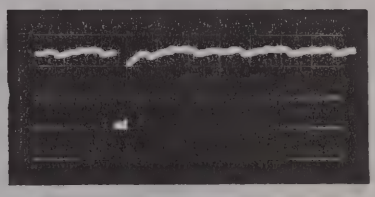
C

P1 - A26 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: EXT + (IJI)



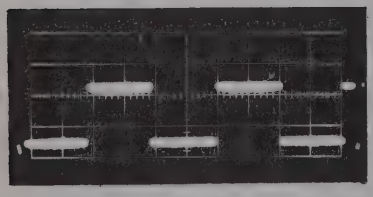
G

P1 - B4 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 20
SYNC: EXT + (IJI)



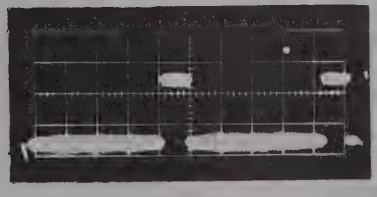
L

PIN 25 V/CM: 2
SWEEP DELAY: 408 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)



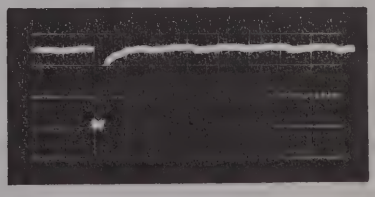
D

P1 - A28 V/CM: 2
SWEEP DELAY: NONE USEC/CM: 50
SYNC: EXT + (IJI)



H

P1 - B27 V/CM: 2
SWEEP DELAY: NONE MSEC/CM: 0.5
SYNC: EXT + (IJI)



M

PIN 32 V/CM: 2
SWEEP DELAY: 353 USEC USEC/CM: 0.5
SYNC: EXT + (IJI)

EL 5895 - 687 - 35 - 3 - TM - 154

Figure 20-19. Counter B card 1A2A4A2 waveforms.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
25	5.0	RX100	4500	RX100	700
26	3.4	RX10,000	650K	RX100	4000
27	0.65	RX10,000	650K	RX100	3200
28	0.65	RX10,000	680K	RX100	3800
29	3.3	RX10,000	680K	RX100	3800
30	0.65	RX10,000	680K	RX100	3800
31	Not used				
32	5.0	RX100	4400	RX100	700
33	Not used				
34	3.3	RX10,000	640K	RX100	700
35	Not used				
36	0.7	RX10,000	550K	RX100	700
37	Not used				
38	3.3	RX10,000	650K	RX100	700
39	Not used				
40	3.3	RX10,000	580K	RX100	700
41	5.0	RX100	1700	RX100	350
42	5.0	RX100	1700	RX100	350
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20–159. Waveforms

(fig. 20–19)

Figure 20–19 shows the counter B card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20–154, 20–155 and 20–156*a*).

Section XXII. TIMING SELF-TEST CARD 1A2A4A3 TROUBLESHOOTING AND REPAIR

20–160. General

This section presents specific troubleshooting and testing information for timing self-test card 1A2A4A3. For troubleshooting, paragraph 20–161 lists helpful data located in other parts of this manual, and paragraphs 20–162, 20–163 and 20–164

provide a troubleshooting procedure which isolates any trouble to a stage or part. For testing after repair, paragraph 20–165 provides a test procedure based on the same test equipment and preparation as for troubleshooting. Paragraph 20–166 provides a list of typical voltage and resistance measurements at the etched connector pins, and figure 20–20 shows the card waveforms which are of significance in troubleshooting and testing.

20–161. Reference Data

The data listed in the following chart will be helpful when troubleshooting the timing self-test card:

Reference	*Data*
Para 4–3	Timing self-test circuit functioning.
Para 4–4	Radar trigger test circuit functioning.
Fig. 24–42	Timing self-test card 1A2A4A3 schematic diagram.

20–162. Test Equipment Required

a. If the timing self-test card can be (or is already) installed in a synchronizer which is connected into the complete hot mockup shown in figure 24–16, there is no need to change the hot mockup. However, the mode 4 word generator and the hybrid attenuator of the test facilities set are not required. The items required are the following:

(1) Multimeter.

(2) Oscilloscope.

(3) Radar test set (only to supply "0" TRIGGER output to 1J1).

(4) Test facilities set (only for cables W32, W41, W42, and W47).

(5) 28-volt dc power supply.

b. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–7.

20–163. Preparation for Troubleshooting

a. At the synchronizer, set the POWER circuit breaker to OFF. If the synchronizer is already connected into the complete hot mockup shown in figure 24–16, disregard step *b* and proceed with step *c*.

b. With the control box connected to the interrogator group case by means of IFF set cable W1, connect the synchronizer, the oscilloscope, the 28-volt dc power supply, and the XTAL MARK & SYNC panel of the radar test set to the interrogator group case as shown in figure 24–16.

c. Set the switches on the control box as directed in paragraph 12–5*c*.

d. At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

e. At the radar test set, set the POWER switch to ON, and set the controls of the XTAL MARK & SYNC panel as directed in paragraph 12–5*e*(3).

f. Turn ON the 28-volt dc power supply and adjust it for an output voltage of 28 volts.

20–164. Troubleshooting Chart

a. Preliminary Procedure. With the timing self-test card installed in an otherwise satisfactory synchronizer, and with the synchronizer connected into either the complete hot mockup shown in figure 24–16 or the partial hot mockup established in paragraph 20–163*b*, proceed as follows:

(1) At the synchronizer, set the POWER circuit breaker to ON.

(2) At the interrogator group case, set the POWER circuit breaker on the power control panel to ON.

(3) At the control box, set the POWER circuit breaker to ON, and check that the CHALLENGE switch is released (to OFF).

NOTE

Troubleshooting may commence immediately. It is not necessary to wait until the receiver-transmitter 60-second warmup delay has ended.

(4) Observe the signals at the test points listed in the following chart, proceeding in step number order unless otherwise directed in the *Corrective measures* column:

b. Timing Self-Test Card 1A2A4A3 Troubleshooting Chart.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
1	Pin 18	Oscilloscope	Reshaped radar trigger (same as J, fig. 20-19, except inverted).	If abnormal, isolate to A2, A3, A4C, or A7C.
2	RADAR TRIG FAULT lamp 1A2DS1.	None	Not lighted	If normal, proceed with step 7. If abnormal, proceed with step 3.
3	J1-9	Oscilloscope	Low prf (continuously high)	If normal, proceed with step 5. If abnormal, proceed with step 4.
4	A7-3	Oscilloscope	(Continuously high)	If abnormal, inverter A7A is defective. If normal, single-shot stage A3 is defective.
5	J1-5	Oscilloscope	High prf (B, fig. 20-20)	If abnormal, single-shot stage A2 is defective.
6	A4-13	Oscilloscope	Radar trigger fault reset (same as K, fig. 20-19).	If abnormal. AND A4C is defective. If normal, flip-flop A8B is defective.
7	TIMING FAULT lamp 1A2DS2.	None	Not lighted	If normal, proceed with step 21. If abnormal, proceed with step 8.
8	J1-2	Oscilloscope	Reshaped radar trigger (same as K, fig. 20-19).	If abnormal, isolate to A5A or A6.
9	J1-3	Oscilloscope	Self-test pretrigger (same as M, fig. 20-19).	If abnormal, isolate to A5B or A7B.
10	J1-4	Oscilloscope	Sif pretrigger (same as L, fig. 20-19).	If abnormal, isolate to A1A or A7B
11	J1-6	Oscilloscope	Processor start pretrigger (same as J, fig. 20-18).	If abnormal, isolate to A1B or A7D.
12	J1-7	Oscilloscope	Mode 4 pretrigger (same as K, fig. 20-18).	If abnormal, isolate to A5A or A7D.
13	J1-10	Oscilloscope	Timing fault accumulator (D, fig. 20-20).	If normal, proceed with step 20. If abnormal, proceed with step 14.
14	J1-8	Oscilloscope	Pretrigger sequence (C, fig. 20-20).	If normal, proceed with step 16. If abnormal, proceed with step 15.
15	J1-1	Oscilloscope	Intermediate pretrigger sequence check (A, fig. 20-20).	If normal, flip-flop A1 is defective. If abnormal, flip-flop A5 is defective.
16	A6-8	Oscilloscope	Self-test and sif pretrigger fault (E, fig. 20-20).	If normal, proceed with step 18. If abnormal, proceed with step 17.

Step No.	Test point	Test equipment	Normal indication	Corrective measures
17	A7–5	Oscilloscope	Self-test or sif pretrigger (G, fig. 20–20).	If normal, flip-flop A6B is defective. If abnormal, OR A7B is defective.
18	A6–13	Oscilloscope	Mode 4 and processor start pretrigger fault (F, fig. 20–20).	If normal, OR A4A is defective. If abnormal, proceed with step 19.
19	A7–14	Oscilloscope	Mode 4 or processor start pretrigger (H, fig. 20–20).	If normal, flip-flop A6A is defective. If abnormal, OR A7D is defective.
20	A2–6	Oscilloscope	High prf (same as B, fig. 20–20, except inverted).	If abnormal, single-shot stage A2 is defective. If normal, flip-flop A8A is defective.
21	RADAR TRIG FAULT lamp 1A2DS1.	None	Lights when PRF control on XTAL MARK & SYNC panel of radar test set is turned fully ccw.	If normal, proceed with step 23. If abnormal, proceed with step 22.
22	J1–9	Oscilloscope	Low prf fault	There should be a square-wave present at this point. It should go high for approximately 5 ms. If abnormal, single-shot stage A3 is defective. If normal, flip-flop A8B is defective.
23	RADAR TRIG FAULT lamp 1A2DS1.	None	Lights when PRF control on XTAL MARK & SYNC panel of radar test set is turned fully cw.	If abnormal, proceed with step 24.
24	J1–5	Oscilloscope	High prf (continuously high)	If abnormal, single-shot stage A2 is defective. If normal, proceed with step 25.
25	A7–8	Oscilloscope	High prf trigger fault (same as K, fig. 20–19).	If normal, flip-flop A8B is defective. If abnormal, AND A7C is defective.

20–165. Test Procedure

a. The test procedure for the timing self-test card is quite similar to the troubleshooting procedure in the preceding paragraphs, except that corrective measures are not applicable. If any abnormal results are obtained, the repaired card is still defective, and the complete troubleshooting procedure must be performed to isolate the defective stage.

b. To test the timing self-test card after repair, first check the card for short circuits that might have been introduced during repair by comparing resistance measurements at its etched connector pins with the values listed in paragraph 20–166. Then prepare a hot mockup as for troubleshooting (paras 20–162 and 20–163) and perform the preliminary procedure given in paragraph 20–164*a*, but do not continue with the troubleshooting chart. Instead, use the oscilloscope to observe the signals at each of the following ponts in any convenient order.

(1) 1A2A4A3J1–1, intermediate pretrigger sequence check (A, fig. 20–20).

(2) 1A2A4A3, 1–5, high prf, (B, fig. 20–20).

(3) 1A2A4A3J1–8, pretrigger sequence (c, fig. 20–20).

(4) 1A2A4A3J1–9, $\overline{\text{low prf}}$ (should be high).

(5) 1A2A4A3J1–10, timing fault accumulator (D, fig. 20–20).

(6) 1A2A4A3–36, timing fault (should be low).

(7) 1A2A4A3–38, radar trigger fault (should be low).

20–166. Etched Connector Pin Voltages and Resistances

a. Conditions of Measurement. The chart below lists the values of dc voltage and resistance that were measured at the etched connector pins of a properly operating timing self-test card.

(1) The dc voltages were measured with respect to chassis ground while the card was extended (installed on an extender card) in a properly operating synchronizer. The synchronizer was connected into a hot mockup and prepared in the same way as for troubleshooting paras 20–162 and 20–163). The preliminary procedure used to turn on the hot mockup IFF set was also the same as for troubleshooting (para 20–164*a*).

(2) The resistances were measured with the card completely removed from the synchronizer. An extender card was used to provide a test point for each pin, so that the measurements could be taken without scratching or otherwise damaging the pins with the probes of multimeter (operated as an ohmmeter). The measurements were taken with respect to pin 2, which normally serves as a ground and signal return pin when the card is installed in a synchronizer. For the forward resistance measurements, the negative ohmmeter probe was connected to pin 2, and the positive probe was touched to each of the listed pins. For the reverse resistance measurements, the positive probe was connected to pin 2, and the negative probe was touched to each of the listed pins.

b. Timing Self-Test Card 1A2A4A3 Etched Connector Pin Voltage and Resistance Measurements.

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
1	0.0	RX1	0.0	RX1	0.0
2	0.0	RX1	0.0	RX1	0.0
3	5.0	RX10,000	1200	RX100	300
4	5.0	RX100	1200	RX100	300
5	Not used				
6	Not used				
7	Not used				
8	Not used				
9	Not used				
10	Not used				
11	Not used				
12	3.8	RX100	6000	RX100	1300
13	Not used				
14	Not used				

Pin No.	Voltage (volts)	Resistance in ohms			
		Meter range	Forward	Meter range	Reverse
15	Not used				
16	Not used				
17	Not used				
18	0.1	RX10,000	220K	RX100	900
19	Not used				
20	5.0	RX10,000	560K	RX100	1000
21	Not used				
22	Not used				
23	Not used				
24	Not used				
25	Not used				
26	5.0	RX10,000	560K	RX100	1000
27	Not used				
28	5.0	RX100	5000	RX100	1000
29	Not used				
30	Not used				
31	Not used				
32	Not used				
33	Not used				
34	5.0	RX100	5000	RX100	1000
35	Not used				
36	0.12	RX10,000	100K	RX100	650
37	Not used				
38	0.12	RX100	6000	RX100	650
39	Not used				
40	4.0	RX10,000	950K	RX100	650
41	5.0	RX100	1200	RX100	300
42	5.0	RX100	1200	RX100	300
43	0.0	RX1	0.0	RX1	0.0
44	0.0	RX1	0.0	RX1	0.0

20-167. Waveforms
(fig. 20-20)

Figure 20-20 shows the timing self-test card waveforms which are significant in troubleshooting or testing. These waveforms were obtained with the card installed in a synchronizer connected to a hot mockup and prepared in the same way as for card troubleshooting (paras 20-162, 20-163 and 20-164*a*).

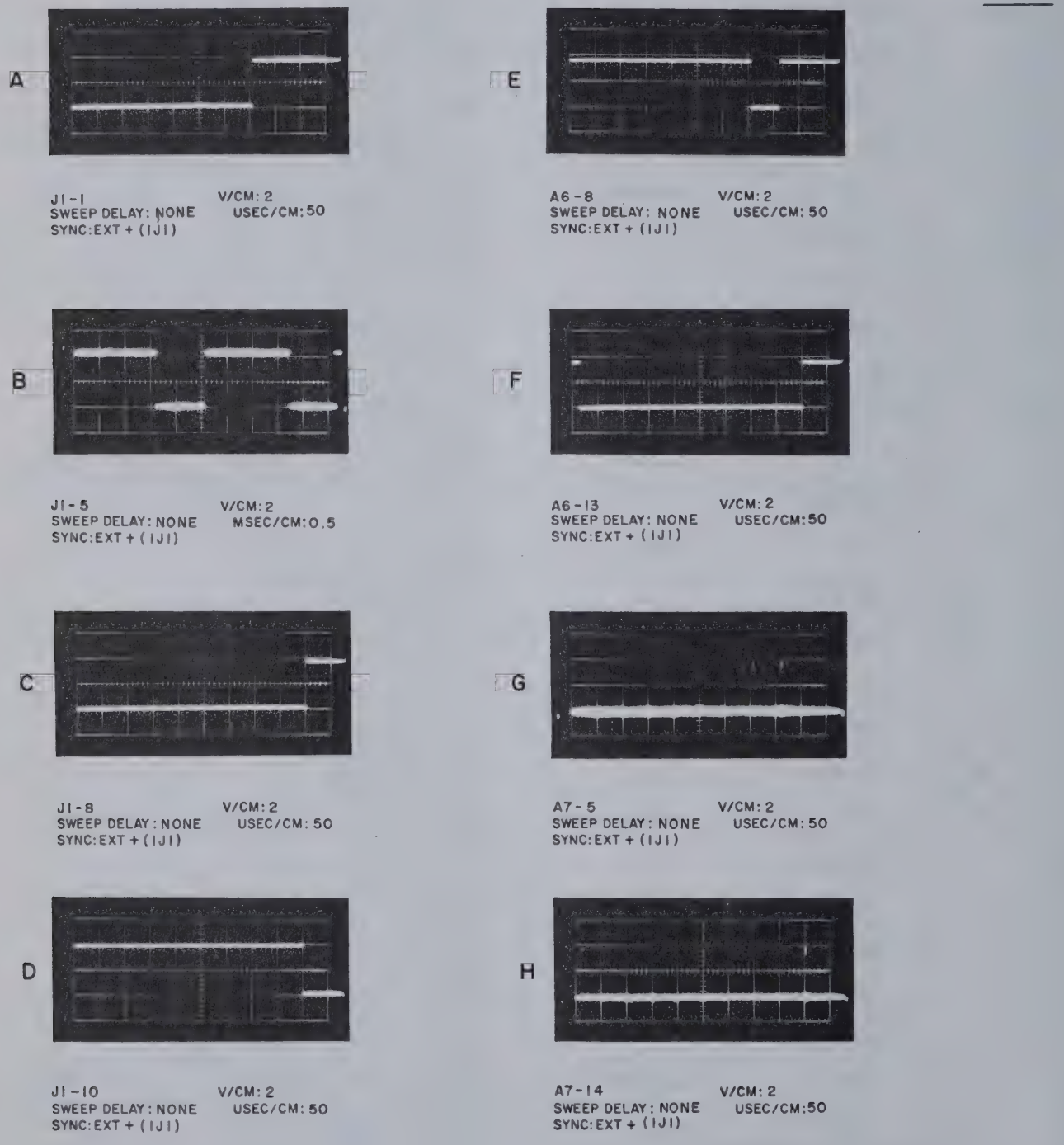


Figure 20-20. Timing self-test card 1A2A4A3 waveforms.

CHAPTER 21

COMPLETE ALIGNMENT AND TESTING OF SYNCHRONIZER

21-1. General

The lists of adjustment and test procedures in this chapter are to be used as a guide for the complete adjustment and/or testing of the synchronizer. Complete adjustment and/or testing are required when the synchronizer either has been out of operation for a prolonged period or has been extensively repaired. Perform the procedures in the order listed, following the step-by-step directions given in the referenced paragraphs.

21-2. Complete Adjustment

The following chart lists the adjustment procedures that should be performed to completely adjust the synchronizer. Step-by-step directions for performing the procedures listed in the *Adjustment* column are provided in the paragraphs listed in the *Procedure* column. To completely adjust the synchronizer, perform the procedures in the order listed below:

Adjustment	*Procedure*
+12-volt adjustment	Paras 18-10 and 18-11
+5-volt adjustment	Paras 18-10 and 18-12
Sif challenge video pulse width adjustment.	Paras 14-10 and 14-11
Mode 4 challenge video pulse width adjustment.	Paras 14-10 and 14-12
Receiver video threshold adjustment.	Paras 15-10 and 15-11
Display gate width adjustment	Paras 16-10 and 16-11
IFF display video adjustments	Paras 16-10 and 16-12

21-3. Complete Testing

A complete step-by-step test procedure for the synchronizer is given in chapter 22. In addition, the following chart lists the test procedures that can be performed to test the six major functional circuits of the synchronizer individually. Step-by-step directions for the major functional circuit tests listed in the *Test* column are provided in the paragraphs listed in the *Procedure* column. Perform the procedures in the order listed below:

Test	*Procedure*
Power supply and power distribution circuit test.	Paras 18-14 and 18-15
Timing circuit test	Paras 13-8 and 13-9
Challenge encoding circuit test	Paras 14-14 and 14-15
Reply decoding circuit test	Paras 15-13 and 15-14
Display video interface circuit test.	Paras 16-14 and 16-15
Fault indication circuit test	Paras 17-8 and 17-9

CHAPTER 23

DEPOT OVERHAUL STANDARDS

23-1. Applicability of Depot Overhaul Standards

Synchronizer, Electrical SN-421/TPX-50 (hereafter referred to as the synchronizer) must be tested thoroughly after rebuild or overhaul to ensure that it meets adequate performance standards for return to stock and reissue. Use the test procedure given in this chapter to measure the performance of a rebuilt or overhauled synchronizer. It is mandatory that each synchronzier to be reissued, or returned to stock for reissue, either as an individual assembly or as part of a complete Interrogator Set AN/TPX-50, meet all of the performance standards given in this chapter.

23-2. Applicable References

a. Repair Standards. Applicable procedures of the Signal Corps depot performing this test, and its general standards for repaired signal equipment, form a part of the requirements for testing this equipment.

b. Technical Publications. The following technical publications are applicable to this equipment:

Equipment and subject	*Publication*
Operator and Organizational Maintenance: Interrogator Set AN/TPX-50.	TM 11-5895-687-12
Organizational Maintenance Repair Parts and Special Tools List: Interrogator Set AN/TPX-50.	TM 11-5895-687-20P
DS, GS, and Depot Maintenance: Interrogator Set AN/TPX-50.	TM 11-5895-687-35-1
Field and Depot Maintenance Repair Parts and Special Tools List: Interrogator Set AN/TPX-50.	TM 11-5895-687-35P-1
Field and Depot Maintenance Repair Parts and Special Tools List: Synchronizer, Electrical SN-421/TPX-50.	TM 11-5895-687-35P-3

c. Modification Work Orders. Perform all applicable modification work orders (MWO's) pertaining to this equipment before making the tests specified. DA Pam 310-7 lists all applicable MWO's.

23-3. Test Facilities Required

The following equipments, or suitable equivalents, will be employed in determining compliance with this specific standard:

a. Test Equipment.

Equipment	Federal stock No.	Qty reqd	Common name	Applicable literature
Counter, Electronic, Digital Readout AN/USM-207A	6625-044-3228	1	Counter	NAVSHIPS 0969-125-0010
Multimeter AN/PSM-6B	6625-957-4374	1	Multimeter	TM 11-6625-475-10
Oscilloscope AN/USM-281A	6625-228-2201	1	Oscilloscope	TM 11-6625-1703-15
Power Supply PP-2953A/U	6130-985-7899	1	28-volt dc power supply	TM 11-6130-233-12
Radar Test Set AN/UPM-98A	6625-912-0429	1	Radar test set	TM 11-6625-403-15-1
Simulator, Test Set AN/APM-245A	6625-169-6551	1	Mode 4 word generator	TM 11-6625-1711-15

Equipment	Federal stock No.	Qty reqd	Common name	Applicable literature
Test Facilities Set AN/TPM-24(V)3.	6625-133-7865	1	Test facilities set	TM 11-6625-2398-15-3

b. Additional Equipment. Interrogator Set AN/TPX-50 (less Synchronizer, Electrical SN-421/TPX-50) and Cable Assembly, Special Purpose, Electrical CX-10876/TPX-50 (7′ 8″) are required to form an electrical test bed (hot mockup) for the synchronizer under test. The assemblies involved are hereafter referred to by common names as follows:

Nomenclature	*Common name*
Interrogator Set Group Cabinet CY-6442/TPX-50.	Interrogator group case.
Signal Processor CP-936/TPX-50_	Processor
Receiver-Transmitter, Radio RT-903/TPX-50.	Receiver-transmitter
Interrogator Set Control C-7651/TPX-50.	Control box
Cable Assembly, Special Purpose, Electrical CX-10876/TPX-50 (7′ 8″).	Cable W1

23-4. General Test Requirements (fig. 23-1)

a. Test Connections. Perform the tests of paragraphs 23-5 through 23-11 with the synchronizer connected to an otherwise complete Interrogator Set AN/TPX-50 (para 23-3*b*) as shown in figure 23-1. To simplify the setup procedures for the successive tests, connect all test equipment initially as shown by unbroken lines in figure 23-1, and then make additional connections or modifications as directed in the individual test procedures. When one or more of the test equipments shown in figure 23-1 are not included in the list of test equipment required for a test, the corresponding connections shown in figure 23-1 are unnecessary but need not be removed; merely disregard them.

b. Applying Test Equipment Power. Connect the test equipments which require power to a source of 115 volts, 60 cps ac. Then turn on the test equipments, observing the following precautions:

(1) Before turning on the 28-volt dc power supply (used in all tests) for the first time, set the POWER circuit breaker on the control box to OFF. Then turn on the 28-volt dc power supply and adjust its output to 28 volts dc. This will insure that the supply voltage is initially within specified limits when the POWER circuit breaker on the control box is set to ON.

(2) Before turning on the mode 4 word generator (used only in the mode 4 tests of paras 23-9 and 23-10) for the first time, set the mode 4 word generator TEST WORD AM. control to its midposition or lower (more counterclockwise than midposition). This will insure against excessive TEST WORD pulse amplitude at the synchronizer when the mode 4 word generator is externally triggered (by the EXT TRIG connection shown as a broken line in fig. 23-1) and W48AT1 and W48P4 of the test facilities set are connected to the TEST WORD receptacle of the mode 4 word generator.

(3) After turning on all test equipment, allow a warmup period of at least 20 minutes before proceeding with any tests other than the power supply and FAULT indicator test of paragraph 23-5. That test is not affected by warmup drift in the test equipment, and may be performed during the 20-minute warmup period.

c. Initial Interrogator Set AN/TPX-50 Control Settings. On the synchronizer under test, set the POWER circuit breaker to OFF and the meter switch to OUT. Then proceed with (1) through

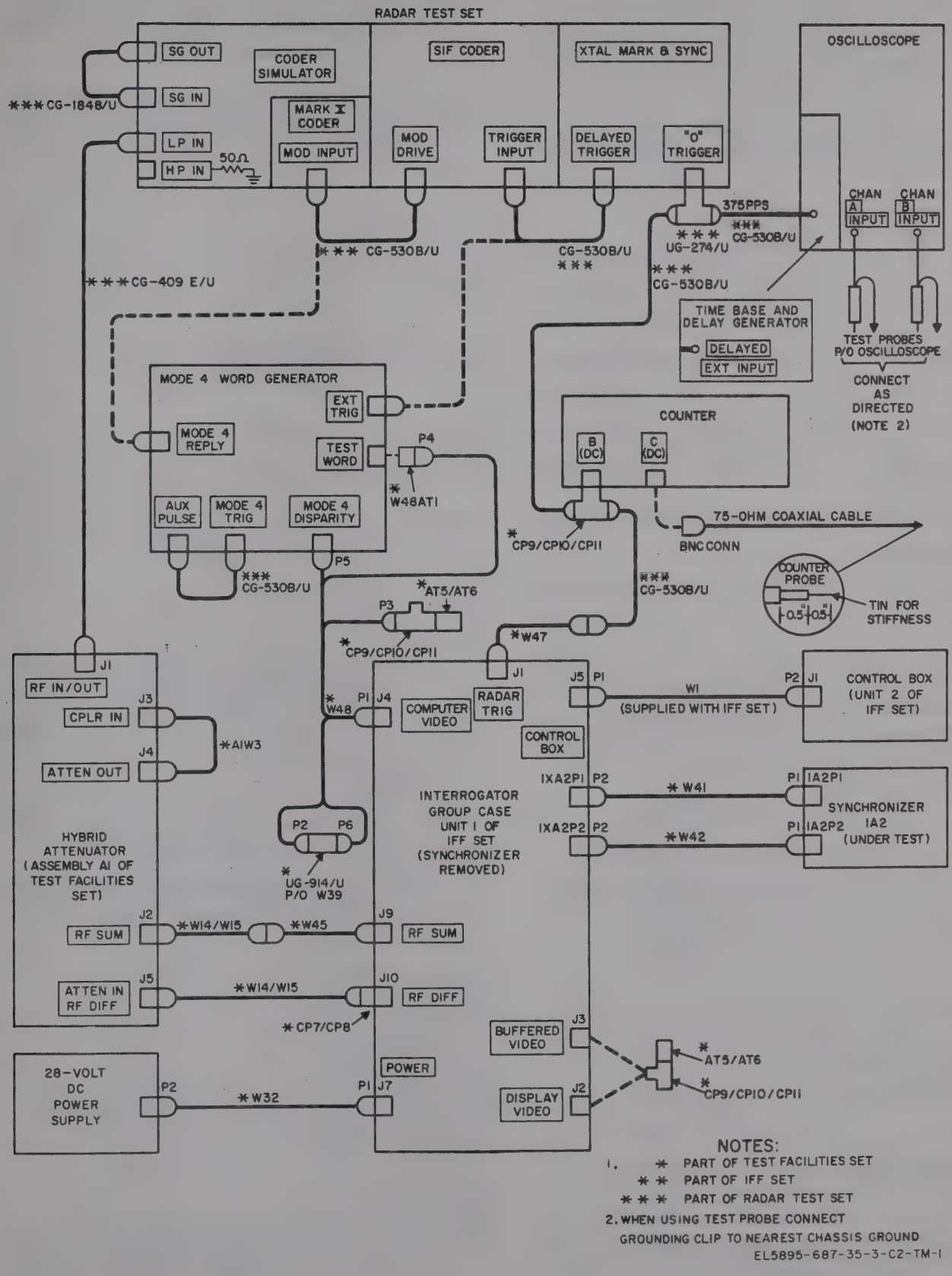


Figure 23-1. Synchronizer test connections.

(4) below, for the initial control settings on the other assemblies of Interrogator Set AN/TPX-50.

(1) On the power control panel of the interrogator group case, set the POWER circuit breaker to ON.

(2) On the processor, set the POWER circuit breaker to ON and the METER switch to OUT.

(3) On the receiver-transmitter, set the POWER circuit breaker to ON, the RF PWR SWITCH to HI, and the (internal) XMTR MOD switch to ON.

(4) On the control box, set the POWER circuit breaker to ON and the switches as follows:

CODE SELECT—MODE 1	73
—MODE 2	7777
—MODE 3/A	7777
CHALLENGE	OFF (released)
GTC	OFF
PANEL	(Immaterial)
PROCESSOR	IN
MODE SELECT	1
SIF REPLIES	CODED (released)
MODE 4	A

d. Test Signals Required. Prepare the test equipment to provide the required test signals as directed in (1) through 6 below. When changes must be made during individual tests, make the changes as directed in the corresponding test procedures.

(1) Adjust the radar test set to provide a "0" TRIGGER output (simulated radar triggers) at a prf of 375 pps as follows:

(*a*) On the radar test set CAL-CONTROL panel, set METER SELECT to 500 PRF, and TRIGGER to INT.

(*b*) On the radar test set XTAL MARK & SYNC panel, set SYNC SELECT to INT, and adjust PRF for a reading of 375 (pps) on CAL-CONTROL panel meter.

(2) Adjust the radar test set to provide a simulated sif code 7777 normal reply with a pulse width of 0.45 μsec as follows:

(*a*) On the radar test set SIF CODER panel, set the following controls to the indicated positions:

CODE (A, B, C, D)	7777
SUB PULSE SELECT	OFF
FUNCTION	N
LEVEL	HI
PULSE WIDTH	(.45)

(*b*) On the radar test set MARK X CODER panel, set FUNCTION to EXT HIGH, and MOD INPUT 75Ω to OUT.

(*c*) On the radar test set CAL-CONTROL panel, set VIDEO OUT to SG MON. This makes the simulated sif reply avail-

able in demodulated form (video pulses) at the VIDEO OUT receptacle for display on the oscilloscope.

(*d*) Connect and adjust the oscilloscope to display the demodulated sif reply, using a sweep speed fast enough to measure the width of any one of the demodulated reply pulses.

(*e*) On the radar test set SIF CODER panel, readjust PULSE WIDTH so that the demodulated reply pulses are 0.45 μsec wide at half-amplitude.

(*f*) Disconnect the oscilloscope from the CAL-CONTROL panel VIDEO OUT receptacle.

(3) Tune the radar test set signal generator to the reply frequency of 1090.0 mc with an attenuation of 40 (dbv) as follows:

(*a*) On the radar test set CODER SIMULATOR, set ATTENUATION to 40.0.

(*b*) On the radar test set CODER SIMULATOR, set WAVEMETER FREQUENCY to the reading corresponding to 1090.0 mc, as given in the associated wavemeter calibration chart.

(*c*) On the radar test set CAL-CONTROL panel, set METER SELECT to WM, and turn WM SENS to midposition.

(*d*) On the radar test set CODER SIMULATOR, set WAVEMETER INPUT to SIG GEN, and tune SG FREQUENCY for best "dip" (downward meter deflection) on the CAL-CONTROL panel meter. Adjust WM SENS on the CAL-CONTROL panel to keep the maximum downward deflection above zero on the meter. If the deflection cannot be kept above zero, temporarily change the CODE (A, B, C, D) settings on the SIF CODER panel from 7777 to 0000 until the best dip has been obtained. Then return the CODE (A, B, C, D) settings to 7777.

(*e*) On the hybrid attenuator of the test facilities set, turn ATTENUATOR to maximum attenuation.

(4) Set up the mode 4 word generator to provide a simulated mode 4 challenge video pulse train beginning 182 μsec (nominal) after the radar test set "0" TRIGGER (simulated radar trigger) and a simulated mode 4 gtc trigger 387 μsec (nominal) after the simulated radar trigger as follows:

(*a*) On the mode 4 word generator, set the following controls to the indicated positions:

TEST WORD switches (all except No. 5)	On (up)
TEST WORD switch No. 5	Off (down)
GO—OFF—NO-GO	OFF
PRF SEL	EXT
AUXILIARY PULSE ON-OFF	OFF
AUXILIARY PULSE AM	(Fully ccw, to minimum).
AUXILIARY PULSE DELAY	(Fully cw, to maximum).
DISPARITY DL1-OFF-DL2	DL2
MKR AM	(Fully ccw, to minimum).

(*b*) On the mode 4 word generator, with TEST WORD AM. at midposition or more counterclockwise, connect W48P4 through 91-ohm series pad W48AT1 to the TEST WORD receptacle.

(*c*) Disconnect the CG-530B/U cable from the TRIGGER INPUT receptacle on the radar test set SIF CODER panel, and connect the cable to the EXT TRIG receptacle on the mode 4 word generator as shown by a broken line in figure 23-1.

(*d*) At the synchronizer, with the POWER circuit breaker at OFF, extend buffer circuit 2 card 1A2A1A7 to observe the TEST WORD (simulated mode 4 challenge video) at pin 34.

(*e*) Connect and adjust the oscilloscope to display the simulated mode 4 challenge video at 1A2A1A7-34, using a sweep externally triggered by the positive-going "0" TRIGGER (simulated radar trigger) input, and fast enough to measure the delay of the first pulse of the simu-

lated mode 4 challenge video. The amplitude of the simulated mode 4 challenge video on the oscilloscope should be 3.0 to 7.0 volts. If not, adjust TEST WORD AM. on the mode 4 word generator for an amplitude of 4.5 volts.

(*f*) On the radar test set XTAL MARK & SYNC panel, set TRIGGER DELAY RANGE to 50–750 and adjust TRIGGER DELAY COARSE and FINE so that the first pulse of the simulated mode 4 challenge video occurs 182 μsec (nominal) after the start of the oscilloscope sweep.

(*g*) Reconnect and adjust the oscilloscope to display the DISPARITY pulse (simulated mode 4 gtc trigger) at 1A2A1A7–36, using a sweep externally triggered by the simulated radar trigger as in (*e*) above, and fast enough to measure the delay of the simulated mode 4 gtc trigger.

(*h*) On the mode 4 word generator, adjust DISPARITY DL2 so that the mode 4 gtc trigger occurs 387 μsec (nominal) after the start of the oscilloscope sweep.

(*i*) Adjust the oscilloscope to measure the pulse width of the simulated gtc trigger at the +2.5-volt amplitude points. Record the pulse width for later reference in the mode 4 challenging test (para 23–9).

(*j*) At the synchronizer, set POWER circuit breaker to OFF and disconnect the oscilloscope and reinstall buffer circuit 2 card 1A2A1A7. Set POWER circuit breaker to ON.

(5) After the mode 4 word generator has been set up to provide simulated mode 4 challenge video and gtc triggers as in (4) above, connect and adjust the mode 4 word generator to provide a simulated mode 4 reply as follows:

(*a*) Disconnect the CG–530B/U cable from the MOD DRIVE receptacle on the radar test set SIF CODER panel, and connect the cable to the MODE 4 REPLY receptacle on the mode 4 word generator as shown by a broken line in figure 23–1.

(*b*) On the radar test set MARK X CODER panel, set MOD INPUT 75Ω to IN.

(*c*) On the mode 4 word generator, set MODE 4 REPLY ON–OFF to ON, and turn MODE 4 REPLY AM. approximately to midposition.

(*d*) On the radar test set CAL–CONTROL panel, set VIDEO OUT to SG MON. This makes the simulated mode 4 reply available as video pulses at the VIDEO OUT receptacle for display on the oscilloscope.

(*e*) Connect and adjust the oscilloscope to display the demodulated mode 4 reply, using a sweep externally triggered by the "0" TRIGGER (simulated radar trigger) input, and fast enough to measure the delay of the first pulse of the reply.

(*f*) On the mode 4 word generator, adjust MODE 4 REPLY DELAY so that the first pulse of the demodulated reply occurs 470 μsec (nominal) after the start of the oscilloscope sweep.

(6) After the mode 4 word generator has been set up as in (4) and (5) above, reconnect the radar test set to provide its simulated sif reply and adjust the reply delay to 500 μsec as follows:

(*a*) Disconnect the CG–530B/U cables from the EXT TRIG and MODE 4 REPLY receptacles on the mode 4 word generator, and reconnect the cables to the TRIGGER INPUT and MOD DRIVE recptacles on the radar test set SIF CODER panel as shown by unbroken lines in figure 23–1.

(*b*) On the radar test set MARK X CODER panel, set MOD INPUT 75Ω to OUT.

(*c*) With the oscilloscope still connected to the VIDEO OUT receptacle of the radar test set CAL–CONTROL panel, the delay of the simulated sif reply can now be observed. On the radar test set XTAL MARK & SYNC panel, readjust TRIGGER DELAY COARSE and FINE so that the first pulse of the simulated sif reply occurs 500 μsec (nominal) after the start of the oscilloscope sweep.

(*d*) Disconnect the oscilloscope from the CAL-CONTROL panel VIDEO OUT receptacle.

23-5. Power Supply and FAULT Indicator Test

(fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN/TPX-50 (para 23-3*b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3*a*.

(1) Radar test set.

(2) Test facilities set.

(3) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) With the synchronizer POWER circuit breaker at OFF, check that the SYN SELF TEST lamp on the control box is lighted.

(2) On the synchronizer, with the POWER circuit breaker at OFF, check that the POWER lamp lights when depressed and goes out when released.

(3) Set the synchronizer POWER circuit breaker to ON, and check that—

(*a*) The SYN SELF TEST lamp on the control box goes out within 1 second.

(*b*) One or more of the four FAULT lamps on the synchronizer may light momentarily, but none remain lighted.

(*c*) The POWER lamp on the synchronizer lights immediately and remains lighted.

(4) On the synchronizer, check that each of the four FAULT lamps lights when depressed and goes out when released.

(5) Set the synchronizer meter switch successively to +5, +12, and −12, allowing the meter reading to settle at each position. The meter reading at each position should settle within the center (solid green) portion of the green band.

(6) Temporarily increase the output of the 28-volt dc power supply to 30 volts, and repeat (5) above.

(7) Temporarily reduce the output of the 28-volt dc power supply to 22.5 volts, and again repeat (5) above.

(8) Return the output of the 28-volt dc power supply to 28 volts.

(9) At the synchronizer, set the POWER circuit breaker to OFF, remove 10-mc clock and counter A card 1A2A4A1 from timing module 1A2A4, and then set the POWER circuit breaker to ON. Check that the synchronizer TIMING FAULT lamp lights.

(10) Check that the SYN SELF TEST lamp on the control box is lighted, and that it remains lighted throughout the remaining steps of this test.

(11) On the radar test set CAL-CONTROL panel, set METER SELECT to 500 PRF.

NOTE

During the subsequent steps the "0" TRIGGER prf is to be varied by means of the PRF control on the radar test set XTAL MARK & SYNC panel. To decrease prf, turn the PRF control counterclockwise. To increase prf to 375 pps, adjust the PRF control until the CAL-CONTROL panel meter reads 375 (pps).

(12) Decrease prf to minimum and check that the synchronizer RADAR TRIG FAULT lamp lights and that the previously lighted TIMING FAULT lamp goes out. Then increase prf to 375 pps.

(13) At the synchronizer, set the POWER circuit breaker to OFF, reinstall 10-mc clock and counter A card 1A2A4A1, remove correct code 1 card 1A2A2A2 from coder-decoder module 1A2A2, and then set the POWER circuit breaker to ON. Check that the synchronizer CODER DECODER FAULT lamp lights.

(14) Decrease prf until the synchronizer RADAR TRIG FAULT lamp lights, and check that the previously lighted CODER DECODER FAULT lamp goes out. Then increase prf to 375 pps.

(15) At the synchronizer, set the POWER circuit breaker to OFF, reinstall correct code 1 card 1A2A2A2, remove interface self-test card 1A2A1A1 from interface module 1A2A1, and then set the POWER circuit breaker to ON. Check that the synchronizer INTERFACE FAULT lamp lights.

(16) Decrease prf until the synchronizer RADAR TRIG FAULT lamp lights, and check that the previously lighted INTERFACE FAULT lamp goes out. Then increase prf to 375 pps.

(17) At the synchronizer, set the POWER circuit breaker to OFF, and reinstall interface self-test card 1A2A1A1.

23-6. Pretrigger Test
(fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN/TPX-50 (para 23-3*b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3*a*.

(1) Counter.

(2) Oscilloscope.

(3) Radar test set.

(4) Test facilities set.

(5) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) At the synchronizer, with the POWER circuit breaker at OFF, extend buffer circuit 2 card 1A2A1A7 for access to the self-test pretrigger on pin 8 and the processor start pretrigger on pin 12. Then set the POWER circuit breaker to ON.

(2) With W48P3 (mode 4 pretrigger) connected to a 75-ohm termination (AT5/AT6) through an adapter tee (CP9/CP10/CP11), connect the oscilloscope to W48P3 through the adapter tee to observe the mode 4 pretrigger across 75 ohms. Adjust the oscilloscope to check that a mode 4 pretrigger is present and to measure its pulse characteristics, which should be as follows:

Polarity	Positive-going.
Amplitude	1.5 to 5.0 volts.
Pulse width	0.5 to 10.0 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.2 μsec maximum.

(3) Disconnect the oscilloscope from the adapter tee on W48P3 and connect W48P3 through the adapter tee to the C (DC) receptacle on the counter, leaving the 75-ohm termination connected to the adapter tee.

(4) On the counter, set the following controls to the indicated positions:

FUNCTION	TIME B C
Time base (outer)	CLOCK FREQ (CPS)-10^7.
DISPLAY	00 (fully counterclockwise).
Mode selector	SEP
B TRIGGER VOLTS (inner)	+4
B MULTIPLIER (outer)	3
B SLOPE	+
C TRIGGER VOLTS (inner)	+2
C MULTIPLIER (outer)	1
C SLOPE	+

(5) On the counter, depress and release RESET to obtain a reading of mode 4 pretrigger delay with respect to the "0" TRIGGER (simulated radar trigger) at the B (DC) receptacle of the counter, which should be 14.5 ± 0.2 μsec.

(6) Connect the oscilloscope to 1A2A1A7-8 (self-test pretrigger) and adjust the oscilloscope to check that a self-test pretrigger is present and to measure its pulse characteristics, which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0 ± 0.5 volt during pulse width.
Pulse width	0.2 ± 0.05 μsec.

Risetime ..... 0.1 μsec maximum.
Falltime ..... 0.1 μsec maximum.

(7) Disconnect the oscilloscope from 1A2A1A7-8.

(8) Reconnect and prepare the counter to measure pretrigger time delays with respect to the mode 4 pretrigger as follows:

(a) Disconnect the "0" TRIGGER from the B (DC) receptacle by disconnecting the adapter tee (CP9 / CP10 / CP11 with two CG-530B / U cables attached) from the B (DC) receptacle. Leave the two CG-530B / U cables connected through the adapter tee.

(b) Disconnect the assembly of W48P3, adapter tee, and 75-ohm termination from the C (DC) receptacle, and connect the assembly to the B (DC) receptacle.

(c) Connect a counter probe such as the one shown in figure 23-1 to the C (DC) receptacle.

(d) Set the following controls to the indicated positions:

B TRIGGER VOLTS (inner) ..... +2
B MULTIPLIER (outer) 1
C SLOPE ..... — (Minus)

(9) Connect the counter probe to 1A2A1A7-8. Then depress and release the RESET button on the counter to obtain a reading of self-test pretrigger delay, which should be 340.0 ± 0.2 μsec.

(10) Disconnect the counter probe from 1A2A1A7-8.

(11) Connect the oscilloscope to 1A2A1A7-12 (processor start pretrigger) and adjust the oscilloscope to check that a processor start pretrigger is present and to measure its pulse characteristics, which should be the same as those given for the self-test pretrigger in (6) above.

(12) Disconnect the oscilloscope from 1A2A1A7-12.

(13) Connect the counter probe to 1A2A1A7-12. Then depress and release the RESET button on the counter to obtain a reading of processor start pretrigger delay, which should be 436.0 ± 0.2 μsec.

(14) Disconnect the counter probe from 1A2A1A7-12.

(15) At the synchronizer, set the POWER circuit breaker to OFF and reinstall buffer circuit 2 card 1A2A1A7.

23-7. Mode 1, 2, and 3 / A (Sif) Challenging Test

(fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN / TPX-50 (para 23-3 *b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3 *a*.

(1) Oscilloscope.
(2) Radar test set.
(3) Test facilities set.
(4) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) At the synchronizer, with the POWER circuit breaker at OFF, extend low level line driver card 1A2A1A6 for access to challenge video on pin 27, isls gate on pin 33, and gtc trigger on pin 21. Then set the POWER circuit breaker to ON.

(2) On the control box, with MODE SELECT at 1, hold CHALLENGE at ON to challenge in mode 1.

(3) Connect the oscilloscope channel A probe to 1A2A1A6-27 (challenge video), and adjust the oscilloscope to check that three mode 1 challenge video pulses are present and to measure their pulse characteristics and spacings, which should be as follows:

Polarity ..... Positive-going.
Amplitude ..... 3.0 to 7.0 volts.
Pulse width ..... 0.80 ± 0.05 μsec.
Risetime ..... 0.1 μsec maximum.
Falltime ..... 0.2 μsec maximum.
Leading edge spacing,
P1 to P2 ..... 2.0 ± 0.15 μsec.
Leading edge spacing,
P1 to P2 ..... 3.0 ± 0.1 μsec.

(4) Connect the oscilloscope channel B probe to 1A2A1A6-33 (isls gate). Then adjust the oscilloscope to check that a mode 1 isls gate is present and to measure its pulse characteristics and the delay of its leading edge from the leading edge of P1 (on the channel A sweep), which should be as follows:

Polarity ..... Positive-going.
Amplitude ..... 3.0 to 5.0 volts.
Pulse width ..... 1.4 ± 0.05 μsec.
Risetime ..... 0.1 μsec maximum.
Falltime ..... 0.15 μsec maximum.
Delay from leading edge
of P1 ..... 1.3 ± 0.05 μsec.

(5) Disconnect the oscilloscope channel B probe from 1A2A1A6-33, connect it to 1A2A1A6-21 (gtc trigger). Then adjust the oscilloscope to check that a gtc trigger is present and to measure its pulse characteristics and its timing with respect to P3 (on the channel A sweep), which should be as follows:

Polarity ..... Positive-going.
Amplitude ..... 3.0 to 7.0 volts.
Pulse width ..... 0.5 to 1.0 μsec.
Risetime ..... 0.1 μsec maximum.
Falltime ..... 0.2 μsec maximum.
Leading edge
timing ..... coincident with leading edge of P3 within ±0.1 μsec.

(6) On the control box, release CHALLENGE (to OFF) and set MODE SELECT to 2. Then hold CHALLENGE at ON to challenge in mode 2.

(7) Adjust the oscilloscope to check that three mode 2 challenge video pulses are present on the channel A sweep and to measure their pulse characteristics and spacings, which should be the same as given in (3) above, except for the following:

Leading edge spacing,
P1 to P3 ..... 5.0 ± 0.1 μsec.

(8) Adjust the oscilloscope to check that a gtc trigger is present on the channel B sweep and to measure its pulse characteristics and its timing with respect to P3 (on the channel A sweep), which should be the same as given in (5) above.

(9) Disconnect the oscilloscope channel B probe from 1A2A1A6-21 and connect it to 1A2A1A6-33 (isls gate). Then adjust the oscilloscope to check that a mode 2 isls gate is present and to measure its pulse characteristics and the delay of its leading edge from the leading edge of P1 (on the channel A sweep), which should be the same as given in (4) above.

(10) On the control box, release CHALLENGE (to OFF) and set MODE SELECT to 3/A. Then hold CHALLENGE at ON to challenge in mode 3/A.

(11) Adjust the oscilloscope to check that three mode 3/A challenge video pulses are present on the channel A sweep and to measure their pulse characteristics and spacings, which should be the same as given in (3) above, except for the following:

Leading edge spacing,
P1 to P3 ..... 8.0 ± 0.1 μsec.

(12) Adjust the oscilloscope to check that a mode 3/A isls gate is present on the channel B sweep and to measure its pulse characteristics and the delay of its leading edge from the leading edge of P1 (on the channel A sweep), which should be the same as given in (4) above.

(13) Disconnect the oscilloscope channel B probe from 1A2A1A6-33 and connect it to 1A2A1A6-21 (gtc trigger). Then adjust the oscilloscope to check that a gtc grigger is present and to measure its pulse characteristics and its timing with respect to P3 (on the channel A sweep), which should be the same as given in (5) above.

(14) Adjust the oscilloscope so that all three challenge video pulses are visible on the channel A sweep.

(15) Set the receiver-transmitter POWER circuit breaker to OFF, loosen the eight front panel retaining screws which secure the receiver-transmitter to the interrogator group case, and pull the receiver-transmitter outward far enough (approximately 1 inch) to disconnect it. This will provide the synchronizer with the equivalent of a high isls pulse inhibit input.

(16) Check that the P2 pulse is no longer present in the oscilloscope display. Disregard the distortion, if any, of the remaining P1 and P3 pulses.

(17) On the control box, release CHALLENGE (to OFF) and set MODE SELECT to 1.

(18) Slide the receiver-transmitter fully into the interrogator group case, tighten its eight front panel retaining screws, and set its POWER circuit breaker to ON.

(19) At the synchronizer, disconnect the oscilloscope probes, set the POWER circuit breaker to OFF, and reinstall low level line driver card 1A2A1A6.

23-8. Mode 1, 2, and 3/A (Sif) Reply Decoding and Processing Test
(fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator set AN/TPX-50 (para 23-3 *b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3 *a*.

(1) Multimeter (not shown in fig. 23-1).
(2) Oscilloscope.
(3) Radar test set.
(4) Test facilities set.
(5) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) At the synchronizer, with the POWER circuit breaker at OFF, extend target video card 1A2A1A4 for access to $\overline{\text{decoded reply video}}$ on pin 35 and $\overline{\text{mode 4/ test target enable}}$ on pin 12. Then set the POWER circuit breaker to ON.

(2) On the control box, with MODE SELECT at 1, hold CHALLENGE at ON to challenge in mode 1. This causes the synchronizer to supply the receiver-transmitter with gtc triggers, and thus

enable the receiver-transmitter to receive the simulated 14-pulse (code 7777) sif reply and to supply the synchronizer with the corresponding receiver video.

(3) Connect the oscilloscope channel B to BUFFERED VIDEO receptacle 1J3 on the interrogator group case, using an adapter tee (CP9 / CP10 / CP11) and a 75-ohm termination (AT5 / AT6) to terminate 1J3 in 75 ohms. Adjust the oscilloscope to check that a 14-pulse train of buffered receiver video pulses is present at 1J3 and to measure the pulse characteristics of at least one of the buffered receiver video pulses, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 to 5.0 volts.
Pulse width	0.45 ± 0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The 14-pulse buffered receiver video pulse train is delayed from the "0" TRIGGER (simulated radar trigger) by slightly more than the 500-μsec delay established in paragraph 23-4 *d* (6) *(c)*.

(4) On the radar test set SIF CODER panel, change the CODE (A, B, C, D) settings from 7777 to 7300 to agree with the MODE 1 CODE SELECT settings on the control box. This removes seven pulses from the buffered receiver video pulse train on the oscilloscope channel B sweep.

(5) Connect the oscilloscope channel A probe to pin 35 (decoded reply video) of target video card 1A2A1A4, and adjust the oscilloscope to check that a decoded reply video pulse is present and to measure its pulse characteristics which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0±0.5 volt during pulse width.
Pulse width	0.4±0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The decoded reply video pulse occurs approximately in coincidence with the last (F2) pulse of the buffered receiver video pulse train on the oscilloscope CHANNEL B sweep.

(6) Disconnect the assembly of the oscilloscope channel B, adapter tee, and 75-ohm termination from BUFFERED VIDEO receptacle 1J3 and connect the assembly to DISPLAY VIDEO receptacle 1J2 to observe the IFF display video pulse at 1J2 across 75 ohms. Adjust the oscilloscope to check that an IFF display video pulse is present at 1J2 and to measure its pulse characteristics, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 ± 0.5 volts.
Pulse width	0.9 to 3.0 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The IFF display video pulse occurs approximately 5 μsec after the decoded reply video pulse on the oscilloscope channel A sweep.

(7) Adjust the oscilloscope so that the decoded reply video pulse on the channel A sweep and the IFF display video pulse on the channel B sweep are both visible.

(8) On the control box, change the MODE 1 CODE SELECT settings from 73 to any other code, such as 00, and check that the IFF display video pulse disappears, but the decoded reply video pulse remains.

(9) On the control box, hold SIF REPLIES at ALL, and check that the IFF display video pulse reappears. Then release SIF REPLIES (to CODED), and change the MODE 1 CODE SELECT settings back to 73.

(10) On the radar test set SIF CODER panel, set FUNCTION to ID to change the simulated normal reply to a simulated i / p reply.

(11) Adjust the oscilloscope to check that now the decoded reply video pulse on the channel A sweep and the IFF display video pulse on the channel B sweep are each followed by one additional pulse having the characteristics given in (5) and (6) above, respectively. Check that the two pulses on each sweep are spaced 24.6 μsec, nominal.

(12) On the radar test set SIF CODER panel, set FUNCTION to EMER to change the simulated i / p reply to a simulated emergency reply.

(13) Adjust the oscilloscope to check that now the decoded reply video pulse on the channel A sweep and the IFF display video pulse on the channel B sweep are each followed by three additional pulses having the characteristics given in (5) and (6) above, respectively. Check that the four pulses on each sweep are spaced at intervals of 24.6 μsec, nominal.

(14) On the radar test set SIF CODER panel, set CODE (A, B, C, D) to 7777 and FUNCTION to N for a simulated code 7777 normal reply.

(15) On the control box, release CHALLENGE (to OFF), and set MODE

SELECT to 2. Then hold CHALLENGE at ON to challenge in mode 2.

(16) Adjust the oscilloscope to check that the decoded reply video pulse on the channel A sweep has the same pulse characteristics as given in (5) above.

(17) Adjust the oscilloscope to check that the IFF display video pulse on the channel B sweep has the same pulse characteristics as given in (6) above.

(18) Adjust the oscilloscope so that the decoded reply video pulse and the IFF display video pulse are both visible.

(19) On the control box, change the MODE 2 CODE SELECT settings from 7777 to any other code, such as 0000, and check that the IFF display video pulse disappears, but the decoded reply video pulse remains.

(20) On the control box, hold SIF REPLIES at ALL, and check that the IFF display video pulse reappears. Then release SIF REPLIES (to CODED), and change the MODE 2 CODE SELECT settings back to 7777.

(21) On the radar test set SIF CODER panel set FUNCTION to ID.

(22) Adjust the oscilloscope to check that now the IFF display video pulse on the channel B sweep is followed by one additional pulse having the characteristics given in (6) above. Check that the two pulses on the channel B sweep are spaced 24.6 μsec, nominal. Disregard the additional pulse on the channel A sweep.

(23) On the radar test set SIF CODER panel, set FUNCTION to EMER and at the control box, set MODE 2 CODE SELECT switches to 7700.

(24) Repeat (13) above.

(25) On the radar test set SIF CODER panel, set FUNCTION to N.

(26) On the control box, release CHALLENGE (to OFF), and set MODE SELECT to 3/A. Then hold CHALLENGE at ON to challenge in mode 3/A.

(27) Repeat (16) through (25) above, except change the MODE 3/A CODE SELECT settings on the control box, rather than the MODE 2 CODE SELECT settings.

(28) Set the processor POWER circuit breaker to OFF, loosen the eight front panel retaining screws which secure the processor to the interrogator group case, and pull the processor outward far enough (approximately 1 inch) to disconnect it. On the control box, set MODE 3/A CODE SELECT switches to 7777.

(29) Check that the IFF display video pulse has disappeared from the oscilloscope channel B sweep, but that the decoded reply video pulse is present on the channel A sweep.

(30) On the control box, set PROCESSOR to BYPASS, and check that the IFF display video pulse reappears. Then set PROCESSOR to IN and release CHALLENGE to OFF.

(31) Slide the processor fully into the interrogator group case, tighten its eight front panel retaining screws, and set its POWER circuit breaker to ON.

(32) Connect the multimeter to measure the dc level of the mode 4/test target enable at pin 12 of target video card 1A2A1A4, which should be +3.0 to +5.0 volts.

(33) At the synchronizer, disconnect the multimeter and oscilloscope channel A probe, set the POWER circuit breaker to OFF, and reinstall target video card 1A2A1A4. Then extend buffer circuit 2 card 1A2A1A7 for access to the processor start pretrigger on pin 12, and set the POWER circuit breaker to ON and on the control box, hold CHALLENGE to ON.

(34) Connect the oscilloscope channel A probe to 1A2A1A7-12 and adjust the oscilloscope so that the processor start pretrigger and an interval of at least 188 μsec immediately following the processor start pretrigger can be examined. The relative position of the IFF display video pulse on the channel B sweep, approximately 75 μsec later than the processor start pretrigger, depend on the delay of the simulated reply.

(35) On the control box, set PROCESSOR to BYPASS.

(36) On the radar test set XTAL MARK & SYNC panel, slowly turn TRIGGER DELAY COARSE counterclockwise and check that the IFF display video pulse, sliding leftward on the oscilloscope channel B sweep, disappears within 10 μsec of coincidence with the processor start pretrigger. Next, slowly turn TRIGGER DELAY COARSE clockwise until the IFF display video pulse, sliding rightward, just disappears. Then carefully adjust TRIGGER DELAY FINE until the IFF display video pulse just reappears, readjusting TRIGGER DELAY COARSE if TRIGGER DELAY FINE has insufficient margin of adjustment.

(37) On the oscilloscope, check that the difference in delay between the leading edge of the processor start pretrigger on the channel A sweep and the leading edge of the IFF display video pulse on the channel B sweep is 188 μsec, nominal.

(38) Disconnect the oscilloscope channel B from the adapter tee at 1J2 and on the control box, hold CHALLENGE to OFF.

(39) At the synchronizer, disconnect the oscilloscope channel A probe, set the POWER circuit breaker to OFF, and reinstall buffer circuit 2 card 1A2A1A7.

23-9. Mode 4 Challenging Test (fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN/TPX-50 (para 23-3 *b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3 *a*.

(1) Mode 4 word generator.
(2) Oscilloscope.
(3) Radar test set.
(4) Test facilities set.
(5) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) Connect the mode 4 word generator and adjust the radar test set trigger delay to provide simulated mode 4 challenge video and mode 4 gtc triggers as directed in paragraph 23-4 *d* (4) (*c*) through *(f)* and *(j)*.

(2) At the synchronizer, with the POWER circuit breaker at OFF, extended low level line driver card 1A2A1A6 for access to challenge video on pin 27 isls gate on pin 33, and gtc trigger on pin 21. Then set the POWER circuit breaker to ON.

(3) On the control box, set MODE SELECT to 4, and hold CHALLENGE at ON to challenge in mode 4.

(4) Connect the oscilloscope channel A probe to 1A2A1A6-27 (challenge video), and adjust the oscilloscope to check that a 37-pulse train of challenge video pulses is present, to measure the pulse characteristics within the train, and to measure the spacing between the leading edges of the fourth and fifth pulses, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 to 7.0 volts.
Pulse width	0.5 ±0.1 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.2 μsec maximum.
Leading edge spacing between fourth and fifth pulse	2.0 ±0.15 μsec.

NOTE

The challenge video is delayed from the "0" TRIGGER (simulated radar trigger) by the 182-μsec delay established in paragraph 23-4 *d* (4).

(5) Connect the oscilloscope channel B probe to 1A2A1A6-33 (isls gate), and adjust the oscilloscope to check that a mode 4 isls gate is present and to measure its pulse characteristics and the delay of its leading edge from the leading edge of the fourth challenge video pulse (on the channel A sweep), which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 to 5.0 volts.
Pulse width	1.4 ±0.05 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.2 μsec maximum.
Delay from leading edge of fourth challenge video pulse	1.3 ±0.05 μsec.

(6) Disconnect the oscilloscope channel B probe from 1A2A1A6-33 and connect the probe to 1A2A1A6-21 (gtc trigger). Then adjust the oscilloscope to check that a mode 4 gtc trigger is present and to measure its pulse characteristics, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 to 7.0 volts.
Pulse width	equal, within ±0.1 μsec, to the width recorded in paragraph 23-4 *d* (4) *(i)*.
Risetime	0.1 μ sec maximum.
Falltime	0.2 μ sec maximum.

NOTE

The mode 4 gtc trigger is delayed from the "0" TRIGGER (simulated radar trigger) by 387-μsec delay established in paragraph 23-4 *d* (4) *(h)*.

(7) Adjust the oscilloscope so that the first five (or more) challenge video pulses are visible on the channel A sweep.

(8) On the control box, release CHALLENGE (to OFF).

(9) Set the receiver-transmitter POWER circuit breaker to OFF, loosen the eight front panel retaining screws which secure the receiver-transmitter to the interrogator group case, and pull the receiver-transmitter outward far enough (approximately 1 inch) to disconnect it. This will provide the synchronizer with the equivalent of a high isls pulse inhibit input.

(10) Use adapter tee (CP9/CP10/CP11) and 75-ohm termination (AT5/AT6) to terminate channel A scope input in 75 ohms.

(11) On the control box, hold CHALLENGE at ON and check that the fifth challenge video pulse is no longer present in the oscilloscope display. Disregard the distortion, if any, of the remaining challenge video pulses.

(12) On the control box, release CHALLENGE (to OFF).

(13) Slide the receiver-transmitter into the interrogator group case, tighten its eight front panel

retaining screws, and set its POWER circuit breaker to ON.

(14) At the synchronizer, disconnect the oscilloscope probes, set the POWER circuit breaker to OFF, and, unless the next test is to be performed, reinstall low level line driver card 1A2A1A6.

(15) Retain the existing mode 4 word generator EXT TRIG connection and radar test set trigger delay setting for the mode 4 reply decoding and processing test (para 23-10).

23-10. Mode 4 Reply Decoding and Processing Test (fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN/TPX-50 (para 23-3b) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3 *a*.

(1) Mode 4 word generator.
(2) Multimeter (not shown in fig. 23-1).
(3) Oscilloscope.
(4) Radar test set.
(5) Test facilities set.
(6) 28-volt dc power supply.

b. Test Procedure. With the mode 4 word generator set up to provide simulated mode 4 challenge video and gtc triggers as at the end of the preceding test, and with the synchronizer and the remainder of the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

(1) Connect the mode 4 word generator to provide a simulated mode 4 reply, in addition to simulated mode 4 challenge video and gtc triggers, as directed in paragraph 23-4 *d* (5) *(a)* and *(b)*.

(2) At the synchronizer, with the POWER circuit breaker at OFF, extend low level line driver card 1A2A1A6 for access to triple pulse decoded video on pin 39. On the radar test set MARK X CODER panel set FUNCTION switch to MOD EXT LOW. Then set the POWER circuit breaker to ON.

(3) On the control box, with MODE SELECT at 4, hold CHALLENGE at ON to challenge in mode 4.

(4) Connect the oscilloscope channel B probe to 1A2A2A6-39 (triple pulse decoded video), and adjust the oscilloscope to check that a triple pulse decoded video pulse is present and to measure its pulse characteristics, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 to 5.0 volts.
Pulse width	0.5 + 0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The triple pulse decoded video pulse is delayed from the "0" TRIGGER (simulated radar trigger) by approximately 5 μsec more than the 470-μsec reply delay established in paragraph 23-4 *d* (5) *(f)*.

(5) At the synchronizer, disconnect the oscilloscope channel B probe, set the POWER circuit breaker to OFF, and reinstall low level line driver card 1A2A1A6. Extend buffer circuit 1 card 1A2A1A8 and target video card 1A2A1A4 for access to spoof counter video on 1A2A1A8-13, decoded reply video on 1A2A1A4-35, and mode 4 / test target enable on 1A2A1A4-12. Then set the POWER circuit breaker to ON.

(6) Connect the oscilloscope channel B probe to 1A2A1A8-13 (spoof counter video), and adjust the oscilloscope to check that a spoof counter video pulse is present and to measure its pulse characteristics, which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0±0.5 volt during pulse width.
Pulse width	0.5±0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The spoof counter video pulse is approximately coincident in time with the triple pulse decoded video pulse check in (4) above.

(7) Connect the oscilloscope channel A probe to 1A2A1A4-35 (decoded reply video), and adjust the oscilloscope to check that a decoded reply video pulse is present and to measure its pulse characteristics, which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0±0.5 volt during pulse width.
Pulse width	0.4±0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

NOTE

The decoded reply video pulse is approximately coincident with the spoof counter video pulse on the channel B sweep.

(8) Disconnect the oscilloscope channel B probe from 1A2A1A8-13, and connect the probe to DISPLAY VIDEO receptacle 1J2 on the in-

terrogator group case, using an adapter tee (CP9/CP10/CP11) and a 75-ohm termination (AT5/AT6) to terminate 1J2 in 75 ohms. Adjust the oscilloscope to check that an IFF display video pulse is present at 1J2 and to measure its pulse characteristics, which should be as follows:

Polarity	Positive-going.
Amplitude	5.0 ± 0.5 volts.
Pulse width	5 ± 0.5 μsec.
Risetime	0.4 μsec maximum.
Falltime	1.0 μsec maximum.

NOTE

The IFF display video pulse occurs approximately 5μ sec later than the decoded reply video pulse on the channel A sweep.

(9) Set the processor POWER circuit breaker to OFF, loosen the eight front panel retaining screws which secure the processor to the interrogator group case, and pull the processor outward far enough (approximately 1 inch) to disconnect it.

(10) Check that the IFF display video pulse has disappeared from the oscilloscope channel B sweep, but that the decoded reply video pulse is present on the channel A sweep.

(11) On the control box, set PROCESSOR to BYPASS, and check that the IFF display video pulse reappears, now with reduced amplitude and pulse width.

(12) Adjust the oscilloscope to measure the new pulse characteristics of the IFF display video pulse, which should be as follows:

Polarity	Positive-going.
Amplitude	3.0 ± 0.5 volts.
Pulse width	0.9 to 3.0 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.2μsec maximum.

(13) On the control box, set PROCESSOR to IN.

(14) Slide the processor fully into the interrogator group case, tighten its eight front panel retaining screws, and set its POWER circuit breaker to ON.

(15) Connect the multimeter to measure the dc level of the mode 4/test target enable at 1A2A1A4-12, which should be 0.0 ± 0.5 volt.

(16) Adjust the oscilloscope to position the IFF display video pulse on a 50 μsec/cm sweep approximately 1 cm (50 μsec) from the beginning of the sweep.

(17) On the radar test XTAL MARK & SYNC panel, slowly turn TRIGGER DELAY COARSE: first counterclockwise to check that the IFF display video pulse, sliding leftward, disappears before reaching the beginning of the sweep; then clockwise until the IFF display video pulse reappears and is again positioned as in (16) above.

(18) Disconnect the oscilloscope channel B probe from the adapter tee at 1J2.

(19) On the control box, release CHALLENGE (to OFF).

NOTE

At this point, the conditions and connections at the synchronizer are suitable for the test target mode test (para 23-11). If there is no reason to postpone the test, disregard (20), below, and proceed as directed in paragraph 23-11 *b* (2).

(20) At the synchronizer, disconnect the multimeter and oscilloscope channel A probe, set the POWER circuit breaker to OFF, and reinstall target video card 1A2A1A4 and buffer circuit 1 card 1A2A1A8.

23-11. Test Target Mode Test
(fig. 23-1)

a. Test Equipment Required. The following equipments, or suitable equivalents, and Interrogator Set AN/TPX-50 (para 23-3 *b*) are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 23-3 *a*.

(1) Multimeter (not shown in fig. 23-1).
(2) Oscilloscope.
(3) Radar test set.
(4) Test facilities set.
(5) 28-volt dc power supply.

b. Test Procedure. With the synchronizer and the required test equipment connected as shown in figure 23-1 and prepared as directed in paragraph 23-4, proceed as follows:

NOTE

If the conditions and connections at the synchronizer are those existing at step (19) of the mode 4 reply decoding and processing test (para 23-10 *b*), disregard (1) below, and proceed directly with (2).

(1) At the synchronizer, with the POWER circuit breaker at OFF, extend buffer circuit 1 card 1A2A1A8 and target video card 1A2A1A4 for access to processor self-test gate on 1A2A1A8-31, spoof counter video on 1A2A1A8-13, decoded reply video on 1A2A1A4-35, and mode 4/test target enable on 1A2A1A4-12. Then connect the oscilloscope channel A probe to 1A2A1A4-35, and connect the multimeter to measure the dc level at 1A2A1A4-12. Set POWER circuit breaker to ON.

(2) On the control box, hold CHALLENGE at TEST to enable the test target mode.

(3) Check that the dc level of the mode 4/test

target enable on 1A2A1A4-12 is 0.0 ±0.5 volt. Then disconnect the multimeter from the synchronizer.

(4) Connect the oscilloscope channel B probe to 1A2A1A8-31 (processor self-test gate), and adjust the oscilloscope to check that a processor self-test gate is present. Then position the leading edge of the processor self-test gate near the end of a 20-μsec / cm sweep, so that an interval of at least 188 μsec immediately preceding the processor self-test gate can be examined. Note the oscilloscope settings for later use in (7) and (10) below.

(5) Check that a train of decoded reply video pulses is sliding smoothly rightward across the channel A sweep. Each pulse should appear approximately 188μsec before the leading edge of the processor self-test gate, and then disappear when it becomes coincident with the leading edge of the processor self-test gate, so that there are never less than two nor more than three pulses visible on the channel A sweep at any one time.

(6) Adjust the oscilloscope to measure the pulse characteristics and leading edge spacings of the sliding decoded reply video pulses, which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0±0.5 volt during pulse width.
Pulse width	0.4±0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

(7) Disconnect the oscilloscope channel B probe from 1A2A1A8-31, connect the probe to 1A2A1A8-13 (spoof counter video), and restore the oscilloscope settings noted in (4) above.
settings noted in (4) above.

(8) Check that the sliding decoded reply video pulses in the channel A sweep are matched by sliding spoof counter video pulses on the channel B sweep.

(9) Adjust the oscilloscope to measure the pulse characteristics of the sliding spoof counter video pulses, which should be as follows:

Polarity	Negative-going from quiescent level.
Quiescent level	+3.0 to +5.0 volts.
Pulse level	0.0±0.5 volts during pulse width.
Pulse width	0.5±0.2 μsec.
Risetime	0.1 μsec maximum.
Falltime	0.1 μsec maximum.

(10) Disconnect the oscilloscope channel B probe from 1A2A1A8-13, and connect the probe to DISPLAY VIDEO receptacle 1J2 on the interrogator group case, using an adapter tee (CP9 / CP10 / CP11) and a 75-ohm termination (AT5 / AT6) to terminate 1J2 in 75 ohms. Then restore the oscilloscope settings noted in (4) above.

(11) Check that the sliding decoded reply video pulses on the channel A sweep are matched by sliding IFF display video pulses on the channel B sweep except where the decoded reply video pulses disappear near the end of the sweep.

NOTE

The IFF display video pulses occur approximately 5 μsec later than the corresponding decoded reply video pulses.

(12) Adjust the oscilloscope to examine one of the IFF display video pulses in detail, and check that it is a superimposed combination of two different pulse shapes: the friend pulse shape, whose characteristics have already been measured, in paragraph 23-10(8); and the target present pulse shape, whose characteristics also have already been measured, in paragraph 23-10 (12).

(13) On the control box, release CHALLENGE (to OFF), and set POWER to OFF.

(14) Disconnect the oscilloscope channel B probe from the adapter tee at 1J2.

(15) At the synchronizer, disconnect the oscilloscope channel A probe, set the POWER circuit breaker to OFF, and reinstall target video card 1A2A1A4 and buffer circuit 1 card 1A2A1A8.

(16) Turn off all test equipment.

CHAPTER 24

FOLDOUT DRAWINGS

24-1. General

This portion of the manual contains the foldout-size illustrations which have been referenced in other chapters. The first illustration, figure 24-1, shows and explains the color code markings for MIL-STD inductors, resistors, and capacitors. The next group of illustrations, figures 24-2 through 24-16, are the functional block diagrams, logic diagrams, and timing diagrams referenced in chapters 3 through 9, and the complete hot mockup drawing referenced in chapters 3 through 9, and the complete hot mockup drawing referenced in chapters 12 through 20. These illustrations are presented in the order referenced, as follows:

Figure No.	*Content*
24-2	Synchronizer overall block diagram.
24-3	Challenge and reply timing relationships.
24-4	Timing circuit logic diagram.
24-5	Challenge encoding circuit functional block diagram.
24-6	Challenge encoding circuit logic diagram.
24-7	Challenge encoding circuit timing diagrams.
24-8	Reply decoding circuit functional block diagram.
24-9	Reply decoding circuit logic diagram.
24-10	Reply decoding circuit timing diagrams.
24-11	Display video interface circuit functional block diagram.
24-12	Display video interface circuit logic diagram.
24-13	Display video interface circuit timing diagrams.
24-14	Fault indication circuit logic diagram.
24-15	Power supply and power distribution circuit logical block diagram.
24-16	Synchronizer test equipment and connections (hot mockup).

24-2. Schematic Diagrams

The complete schematic diagam of the synchronizer is presented as a set of separate schematic diagrams of its physically separable (plug-in) subassemblies in figures 24-17 through 24-42. These schematic diagrams are arranged in the order of the reference designations assigned to the plug-in parts, except for delay line module 1A2A5. The delay line module schematic diagram is included in the overall synchronizer (chassis) schematic diagram, figure 24-17. The following chart lists the schematic diagrams and gives the reference designations of the subassemblies:

Figure No.	*Reference designation*	*Subassembly name*
24-17	1A2	Synchronizer chassis (includes delay line module 1A2A5 and component board 1A2A7).
24-18	1A2A1	Interface module
24-19	1A2A1A1	Interface self-test card
24-20	1A2A1A2	Level shifter card (also applies to identical level shifter card 1A2A2A1).
24-21	1A2A1A3	Test target generator card
24-22	1A2A1A4	Target video card
24-23	1A2A1A5	Display video card
24-24	1A2A1A6	Low level line driver card
24-25	1A2A1A7	Buffer circuit 2 card
24-26	1A2A1A8	Buffer circuit 1 card
24-27	1A2A2	Coder-decoder module
24-20	1A2A2A1	Level shifter card
24-28	1A2A2A2	Correct code 1 card
24-29	1A2A2A3	Correct code 2 card
24-30	1A2A2A4	Coder card
24-31	1A2A2A5	Challenge video card
24-32	1A2A2A6	Reply video card

Figure No.	*Reference designation*	*Subassembly name*
24-33	1A2A2A7	I/p and emergency code card.
24-34	1A2A2A8	Coder-decoder self-test card
24-35	1A2A3	Power supply module
24-36	1A2A3A1	+12-volt regulator card
24-37	1A2A3A2	+5-volt regulator card
24-38	1A2A3A3	−12-volt inverter card
24-39	1A2A4	Timing module
24-40	1A2A4A1	10-mc clock and counter A card.
24-41	1A2A4A2	Counter B card
24-42	1A2A4A3	Timing self-test card
(24-17)	1A2A5	Delay line module
(24-17)	1A2A6	28-volt line filter (sealed subassembly).
(24-17)	1A2A7	Component board (meter multiplier parts).

COLOR CODE TABLES

N, CY and CB

CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
		± 20%	± 20%		A				−55° to +70°C	10–55 cps
				B	E		B			
± 2%		± 2%	± 2%	C		C			−55° to +85°C	
	± 30%			D			D	300		
				E					−55° to +125°C	10–2,000 cps
± 5%				F				500		
									−55° to +150°C	
		± 5%	± 5%							
± 10%	± 10%	± 10%	± 10%							

pose, Style CK

LIER[1]	CAPACITANCE TOLERANCE	MIL ID
1	± 20%	
0	± 10%	
0		
0		
0		CK

TABLE III – For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	−30	1	1	10	± 1%		
RED	−80	2	2	100	± 2%	± 0.25uuf	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5%	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

ignificant (SIG) figures are multiplied to obtain the capacitance in uuf.

applicable specifications: MIL–C–5, MIL–C–91, MIL–C–11272, and MIL–C–10950 respectively.

ge-temperature limits designated in MIL–C–11015.

degree centigrade.

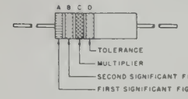
STD–C2

Figure 24–1. Color code markings for MIL–STD inductors, resistors, and capacitors.

Figure No.	*Reference designation*	*Subassembly name*
24–33	1A2A2A7	I/p and emergency code card.
24–34	1A2A2A8	Coder-decoder self-test card
24–35	1A2A3	Power supply module
24–36	1A2A3A1	+12-volt regulator card
24–37	1A2A3A2	+5-volt regulator card
24–38	1A2A3A3	−12-volt inverter card
24–39	1A2A4	Timing module
24–40	1A2A4A1	10-mc clock and counter A card.
24–41	1A2A4A2	Counter B card
24–42	1A2A4A3	Timing self-test card
(24–17)	1A2A5	Delay line module
(24–17)	1A2A6	28-volt line filter (sealed subassembly).
(24–17)	1A2A7	Component board (meter multiplier parts).

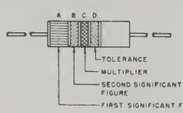
COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS

COMPOSITION-TYPE RESISTORS



BAND A— Equal Width Band Signifies Composition-Type

WIREWOUND-TYPE RESISTORS

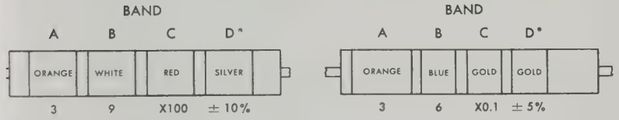


BAND A— Double Width Signifies Wire-wound Resistor

COLOR CODE TABLE

BAND A		BAND B		BAND C		BAND D*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1		
BROWN	1	BROWN	1	BROWN	10		
RED	2	RED	2	RED	100		
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	± 10
GREEN	5	GREEN	5	GREEN	100,000	GOLD	± 5
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	SILVER	0.01		
WHITE	9	WHITE	9	GOLD	0.1		

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 Ohms 3.6 Ohms

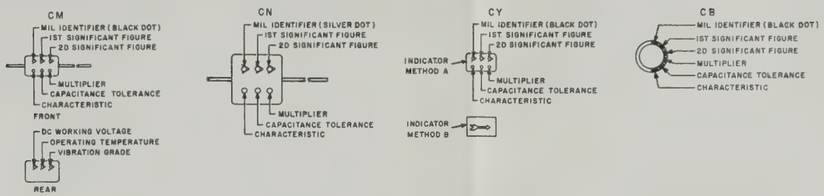
RESISTANCE TOLERANCE ± 10 percent ± 5 percent

STD-R2

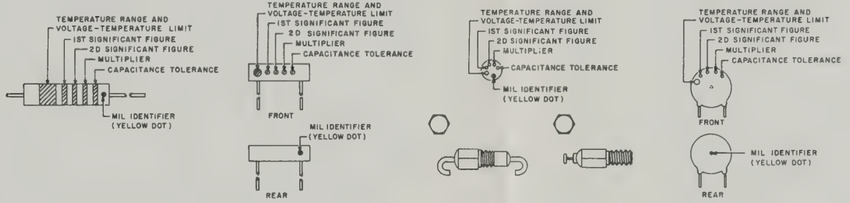
*If Band D is omitted, the resistor tolerance is ±20%, and the resistor is not Mil-Std.

COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

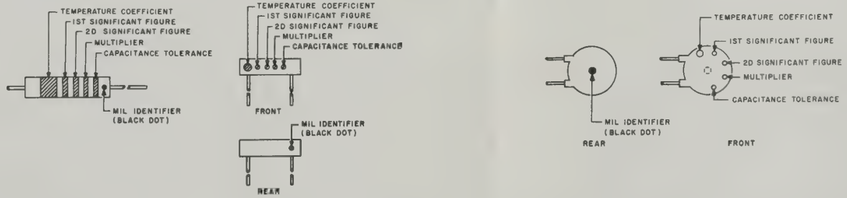
GROUP I Capacitors, Fixed, Various-Dielectrics, Styles CM, CN, CY, and CB



GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK



GROUP III Capacitors, Fixed, Ceramic-Dieletric (Temperature Compensating) Style CC



COLOR CODE TABLES

TABLE I – For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM, CY CB	0	0	1			± 20%	± 20%		A				−55° to +70°C	10–55 cps
BROWN		1	1	10					B	E		B			
RED		2	2	100	± 2%		± 2%	± 2%	C		C			−55° to +85°C	
ORANGE		3	3	1,000		± 30%			D			D	300		
YELLOW		4	4	10,000					E					−55° to +125°C	10–2,000 cps
GREEN		5	5		± 5%				F				500		
BLUE		6	6											−55° to +150°C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

TABLE II – For use with Group II, General Purpose, Style CK

COLOR	TEMP. RANGE AND VOLTAGE – TEMP. LIMITS[3]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20%	
BROWN	AW	1	1	10	± 10%	
RED	AX	2	2	100		
ORANGE	BX	3	3	1,000		
YELLOW	AV	4	4	10,000		CK
GREEN	CZ	5	5			
BLUE	BV	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III – For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	30	1	1	10	± 1%		
RED	80	2	2	100	± 2%	± 0.25uuf	
ORANGE	150	3	3	1,000			
YELLOW	220	4	4				
GREEN	330	5	5		± 5%	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	−100					± 1.0uuf	
SILVER							

1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.
2. Letters indicate the Characteristics designated in applicable specifications: MIL–C–5, MIL–C–91, MIL–C–11272, and MIL–C–10950 respectively.
3. Letters indicate the temperature range and voltage-temperature limits designated in MIL–C–11015.
4. Temperature coefficient in parts per million per degree centigrade.

STD-C2

Figure 24-1. Color code markings for MIL-STD inductors, resistors, and capacitors.

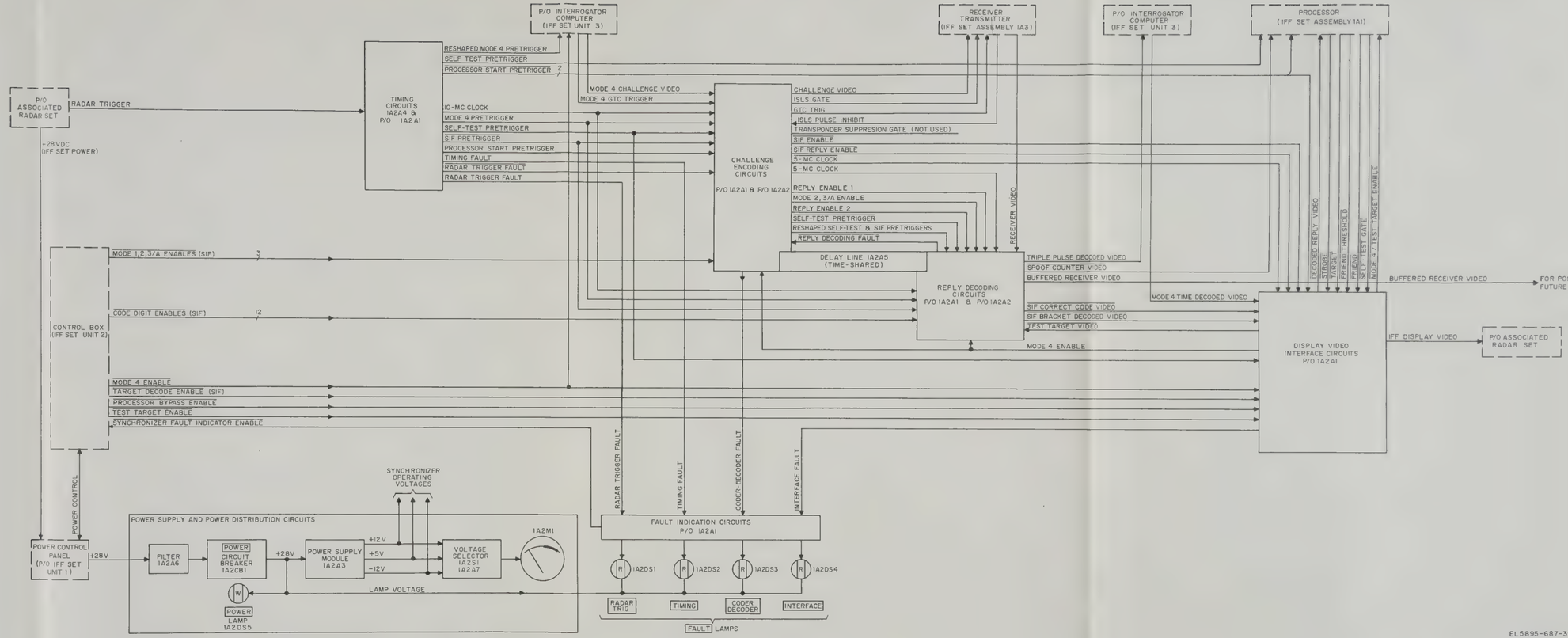
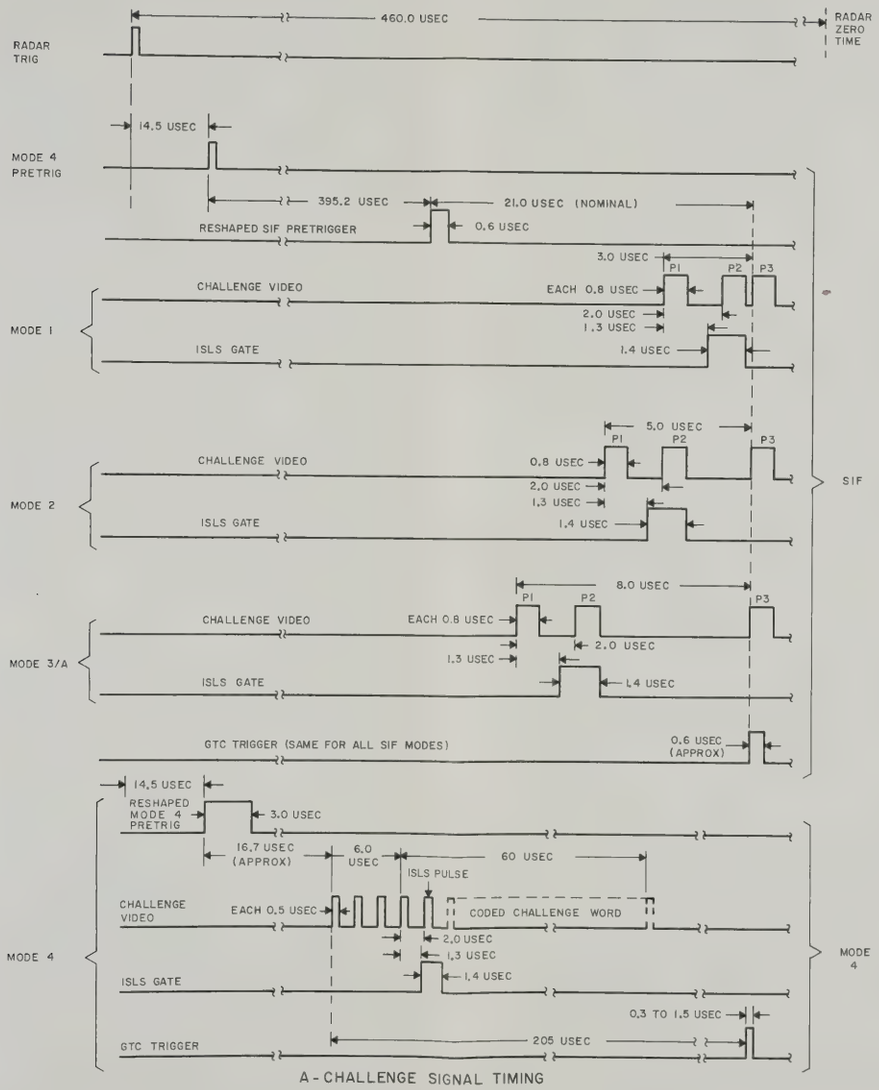
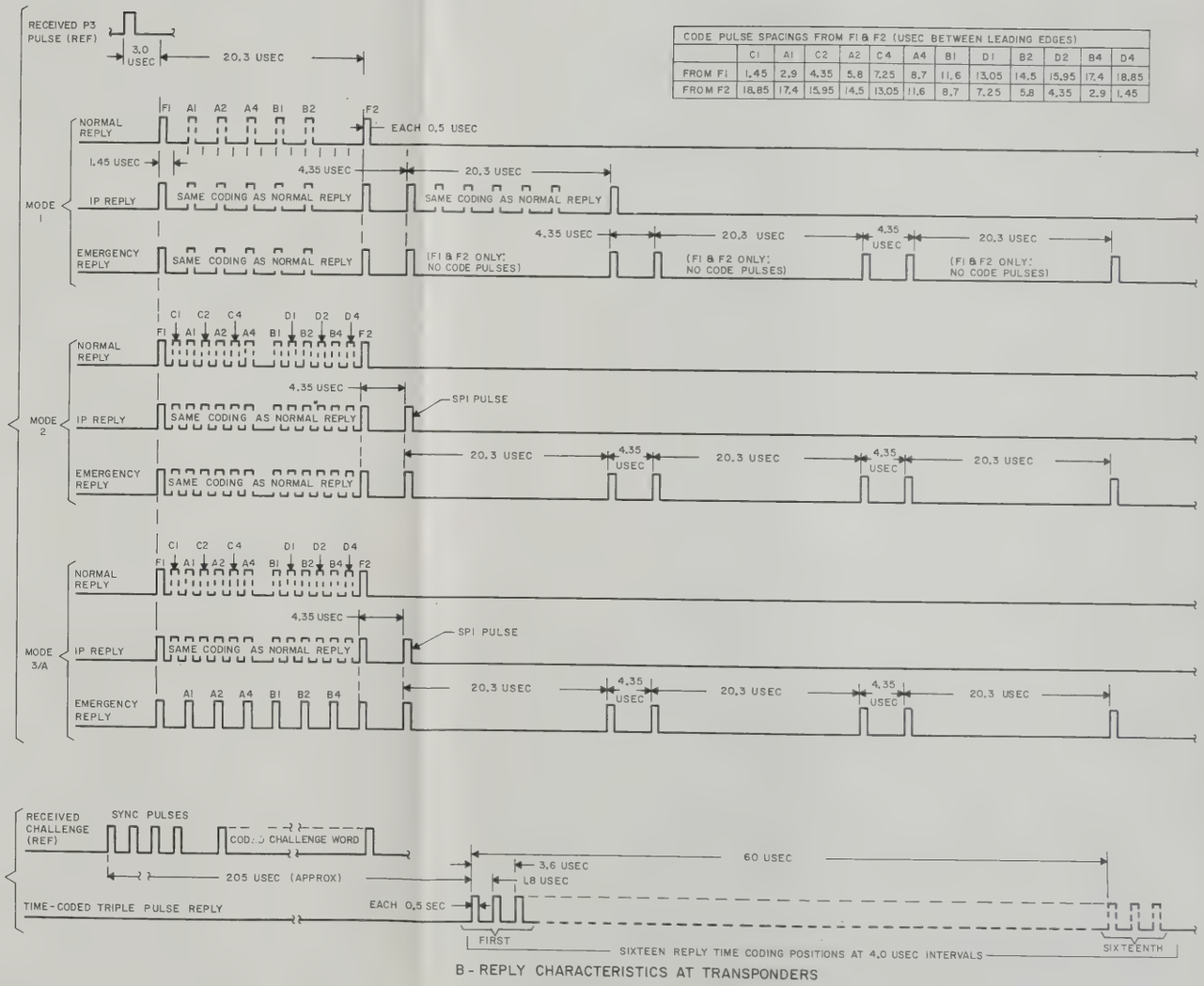


Figure 24-2. Synchronizer overall block diagram.



A - CHALLENGE SIGNAL TIMING

CODE PULSE SPACINGS FROM F1 & F2 (USEC BETWEEN LEADING EDGES)												
	C1	A1	C2	A2	C4	A4	B1	D1	B2	D2	B4	D4
FROM F1	1.45	2.9	4.35	5.8	7.25	8.7	11.6	13.05	14.5	15.95	17.4	18.85
FROM F2	18.85	17.4	15.95	14.5	13.05	11.6	8.7	7.25	5.8	4.35	2.9	1.45



B - REPLY CHARACTERISTICS AT TRANSPONDERS

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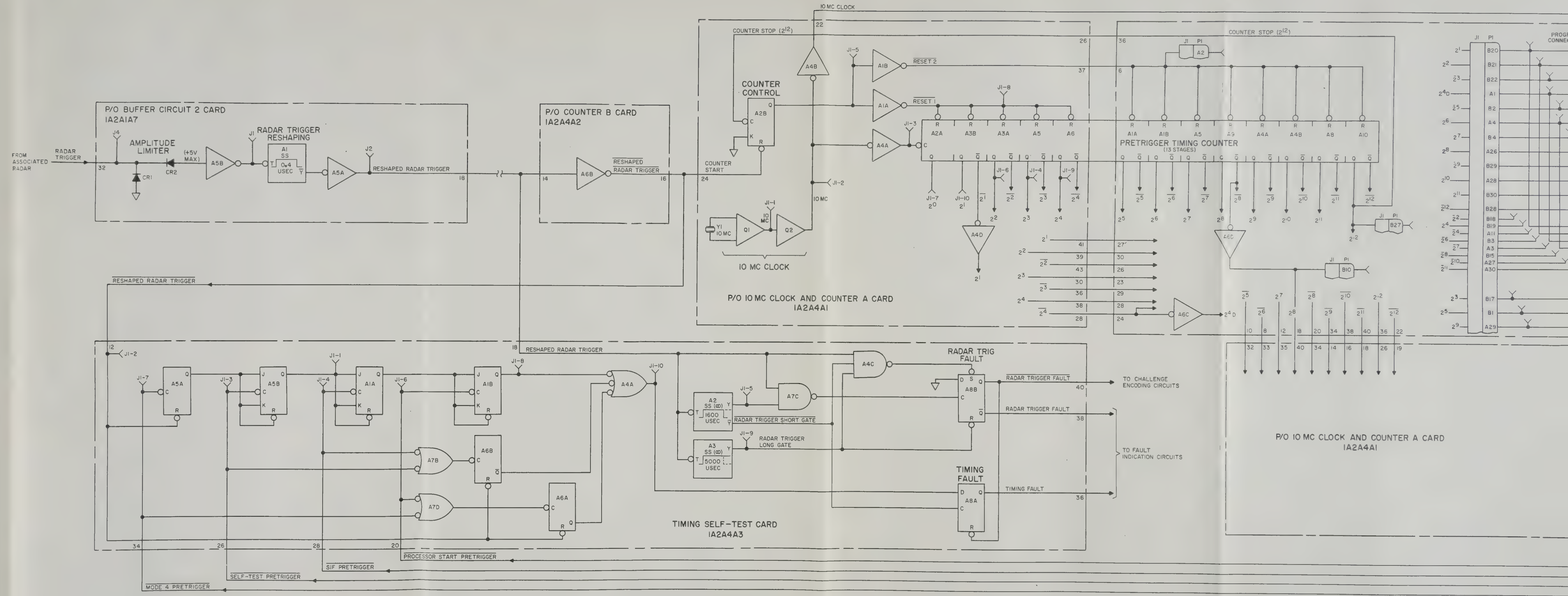
Figure 24-3. Challenge and reply timing relationships.


P/O BUFFER CIRCUIT 2 CARD
IA2AIA7
FROM ASSOCIATED RADAR
RADAR TRIGGER
AMPLITUDE LIMITER
(+5V MAX)
CR1
CR2
A5B
RADAR TRIGGER RESHAPING
AI SS 0.4 USEC
A5A
RESHAPED RADAR TRIGGER
P/O COUNTER B CARD
IA2A4A2
A6B
RESHAPED RADAR TRIGGER
10 MC CLOCK
COUNTER STOP (2^12)
COUNTER CONTROL
A2B
A4B
A1B
RESET 2
A1A
RESET 1
A4A
COUNTER START
Y1 10 MC
Q1
Q2
10 MC CLOCK
A4D
P/O 10 MC CLOCK AND COUNTER A CARD
IA2A4AI
PRETRIGGER TIMING COUNTER
(13 STAGES)
A6C
A6D
PROGR CONNEC
RESHAPED RADAR TRIGGER
A5A
A5B
A1A
A1B
A6B
A7B
A7D
A6A
A4A
A2 SS (∞) 1600 USEC
RADAR TRIGGER SHORT GATE
A3 SS (∞) 5000 USEC
RADAR TRIGGER LONG GATE
A7C
A4C
RADAR TRIG FAULT
A8B
RADAR TRIGGER FAULT
TO CHALLENGE ENCODING CIRCUITS
RADAR TRIGGER FAULT
TO FAULT INDICATION CIRCUITS
TIMING FAULT
A8A
TIMING FAULT
TIMING SELF-TEST CARD
IA2A4A3
PROCESSOR START PRETRIGGER
SIF PRETRIGGER
SELF-TEST PRETRIGGER
MODE 4 PRETRIGGER
P/O 10 MC CLOCK AND COUNTER A CARD
IA2A4AI

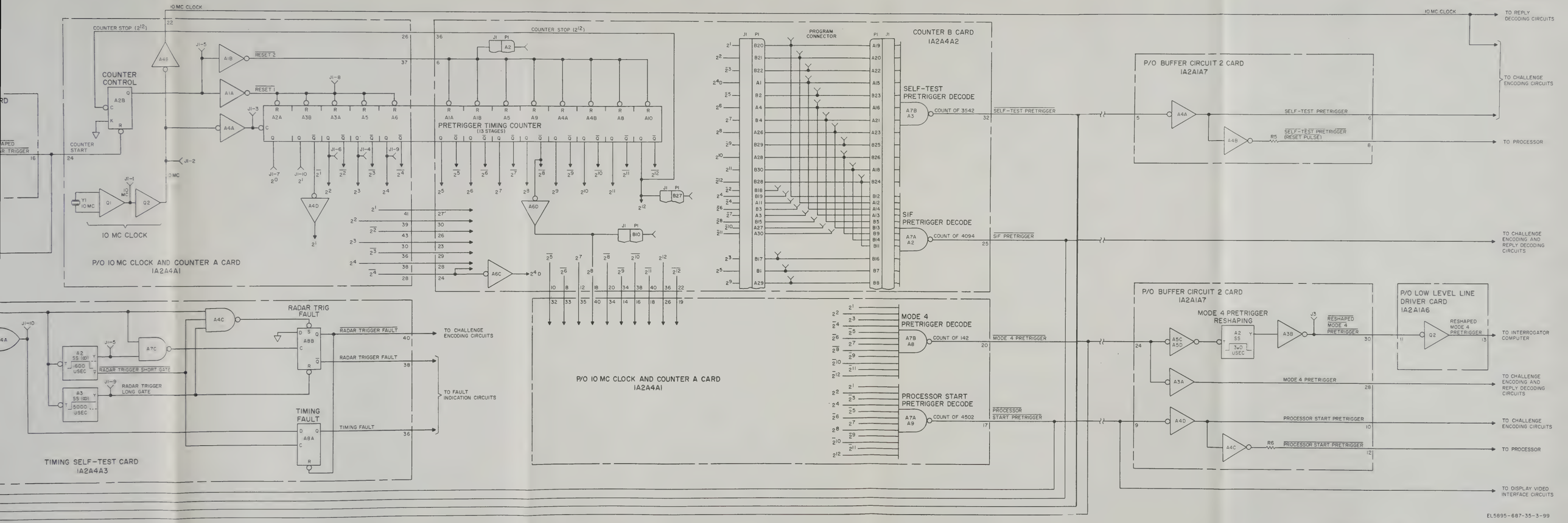


Figure 24-4. Timing circuit logic diagram.

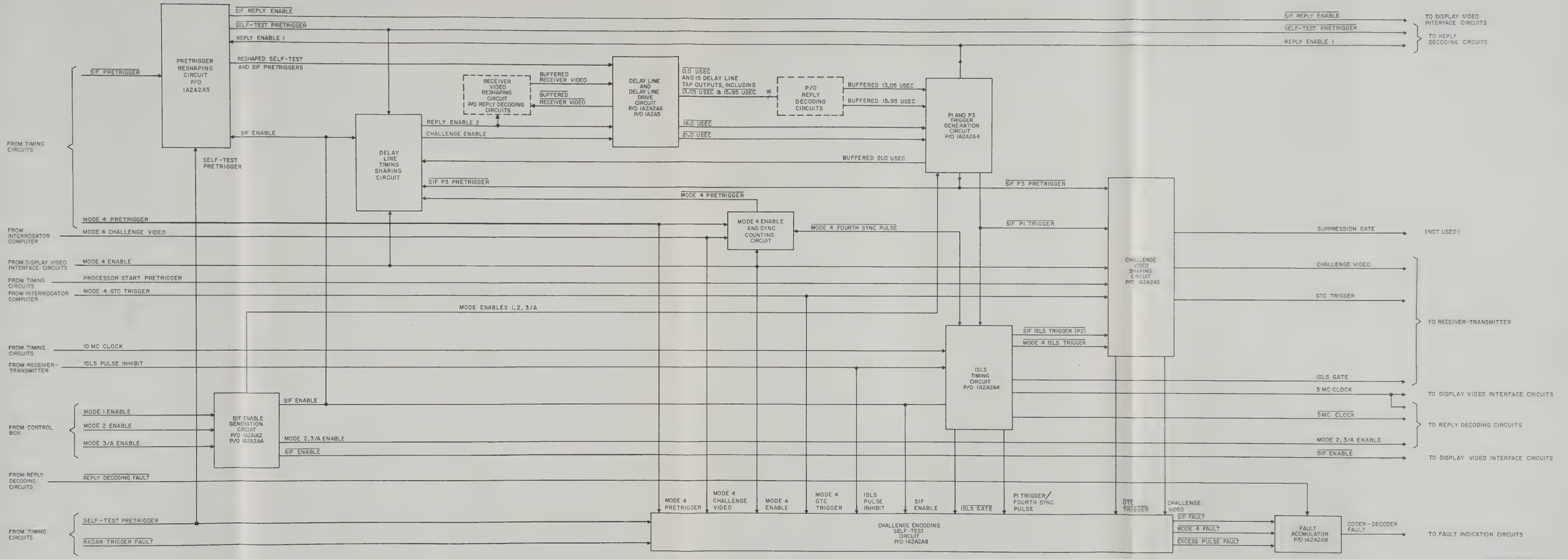


Figure 24-5. Challenge encoding circuit functional block diagram.

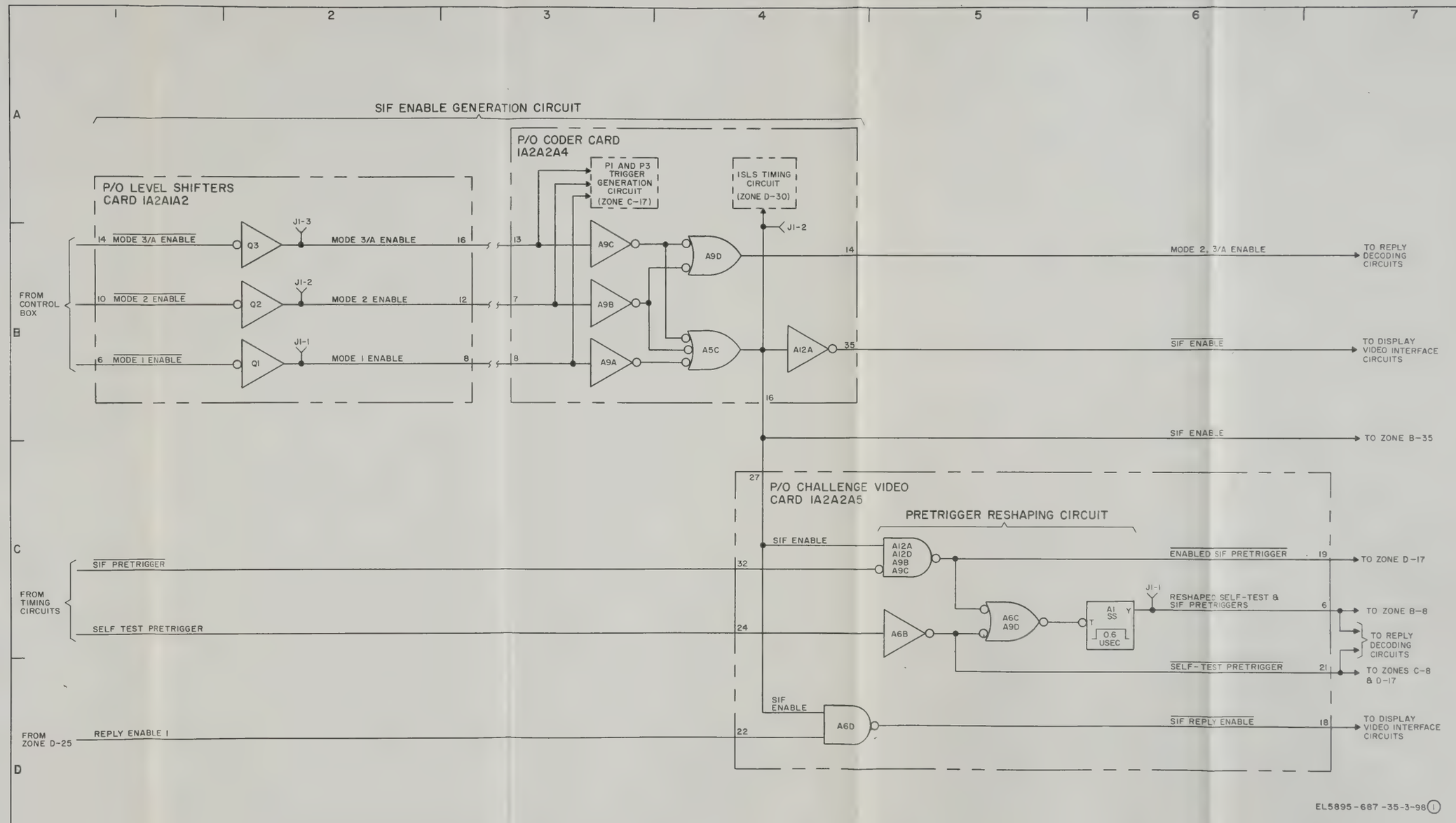


Figure 24-6(1). Challenge encoding circuit logic diagram (sheet 1 of 5).

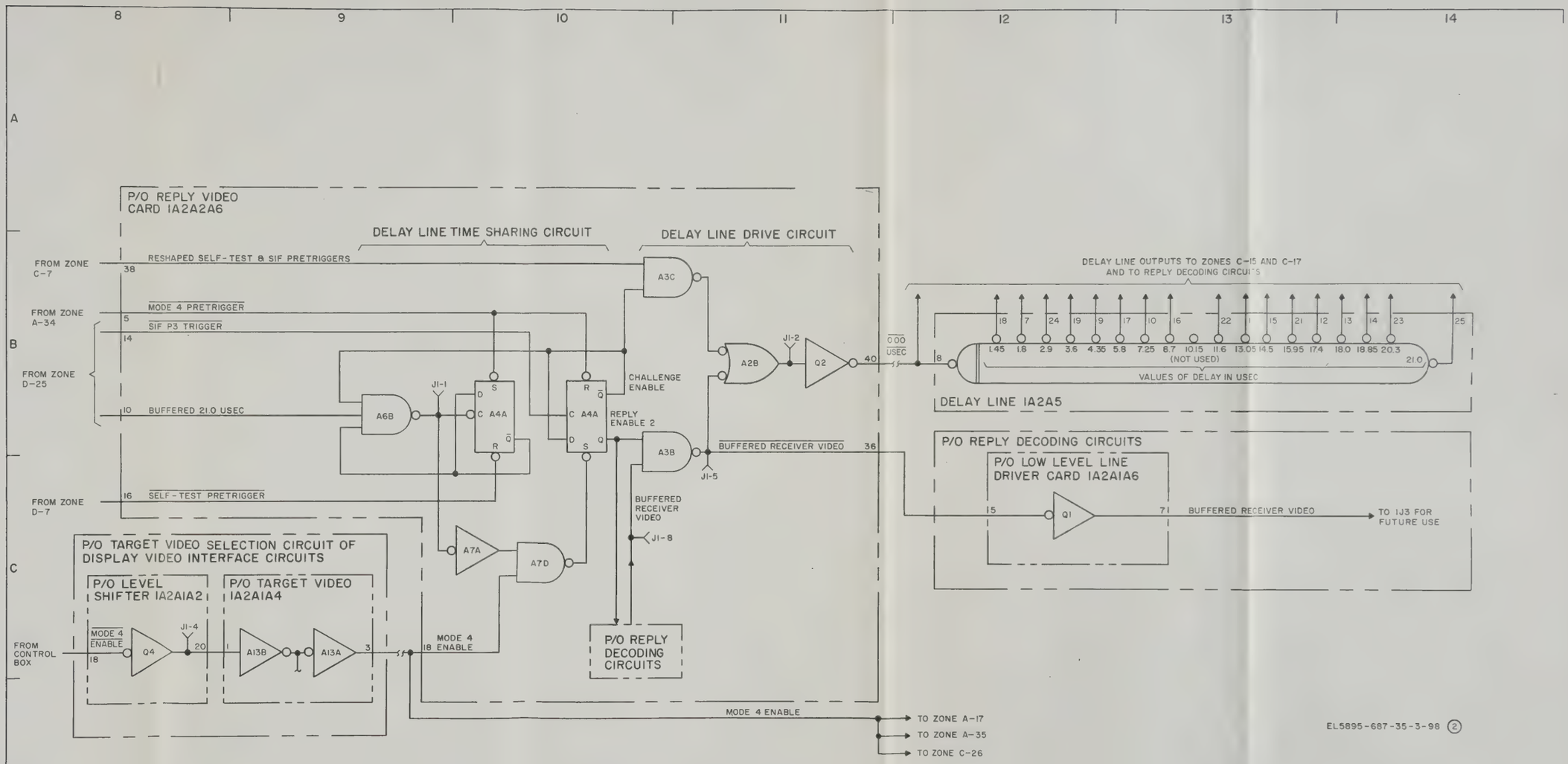


Figure 24-6③. Challenge encoding circuit logic diagram (sheet 2 of 5).

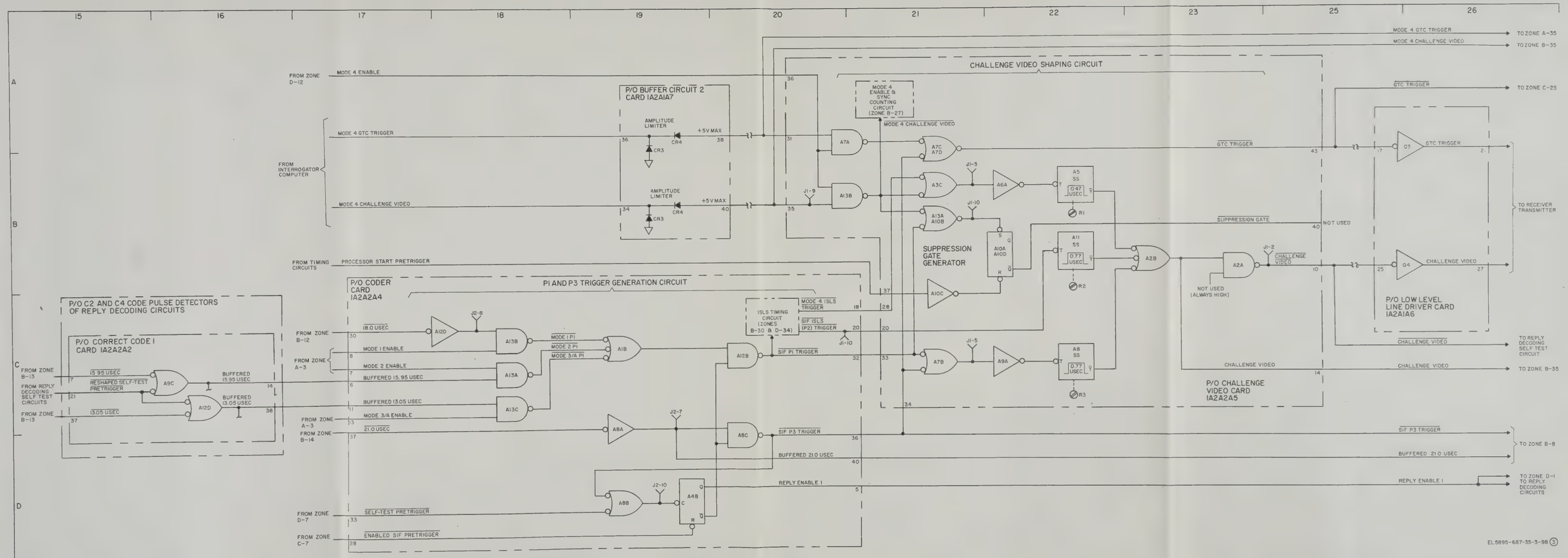


Figure 24-6③. Challenge encoding circuit logic diagram (sheet 3 of 5).

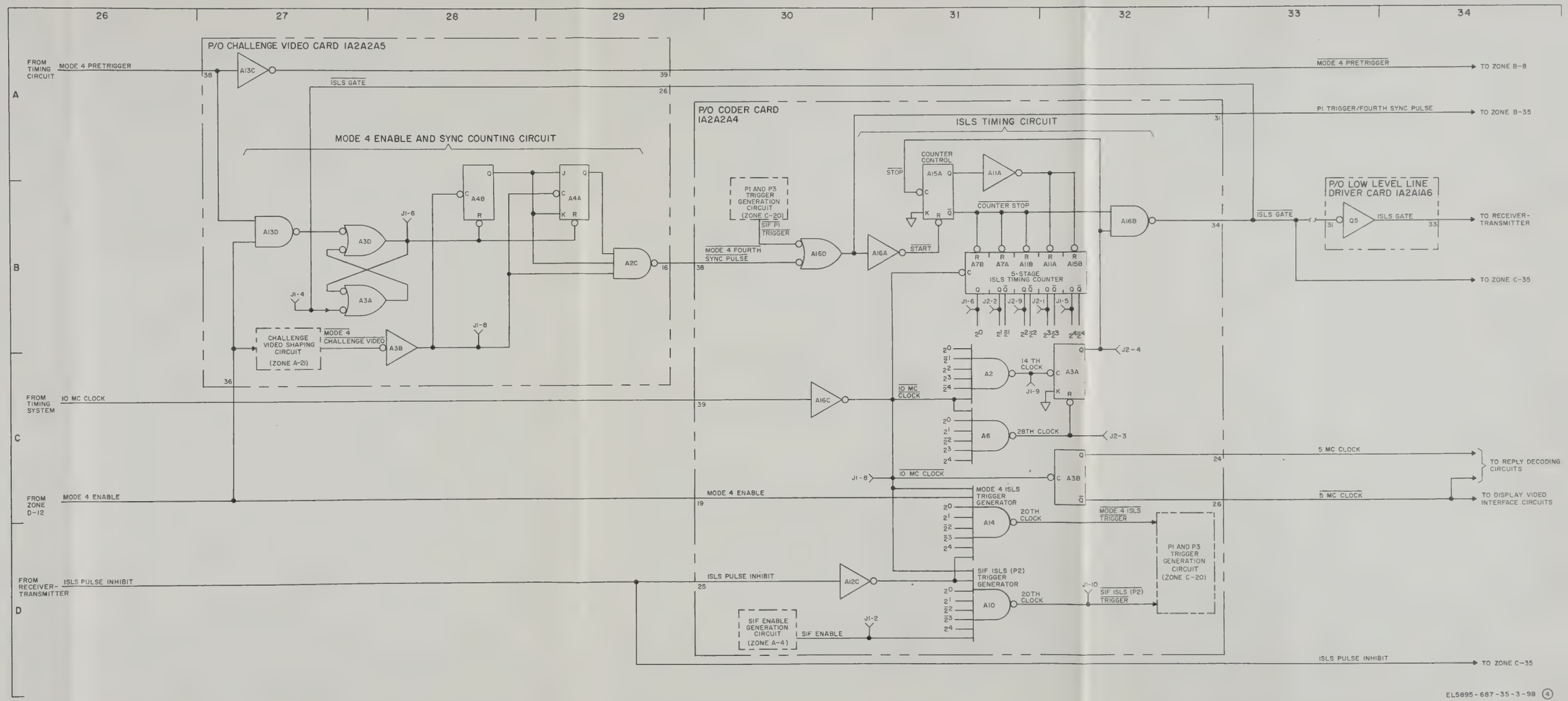


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Figure 24-6④. Challenge encoding circuit logic diagram (sheet 4 of 5).

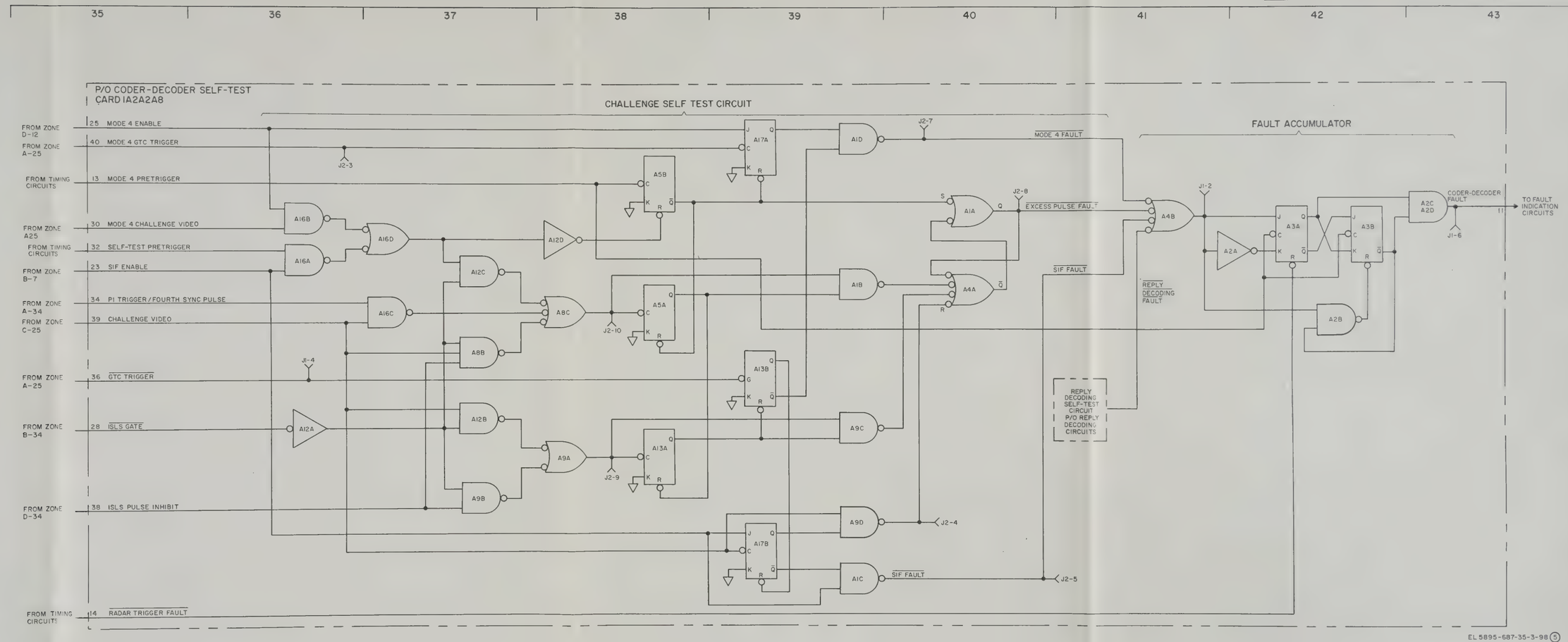
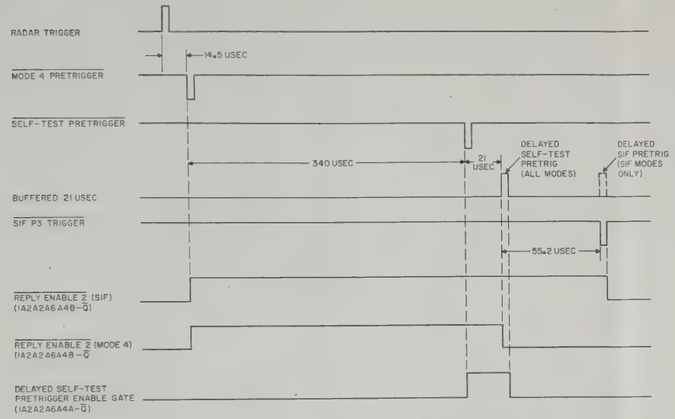
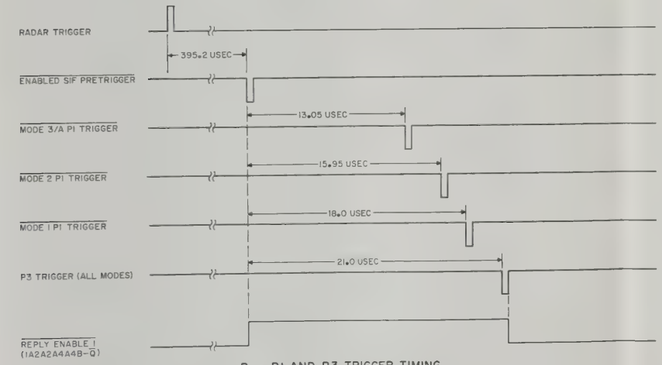


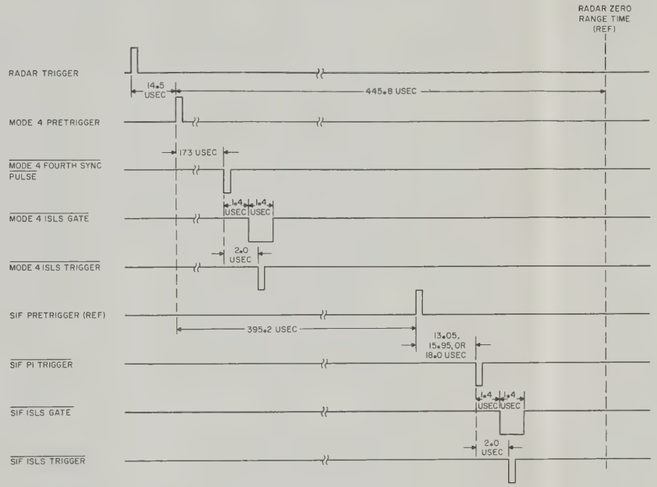
Figure 24-6(5). Challenge encoding circuit logic diagram (sheet 5 of 5).



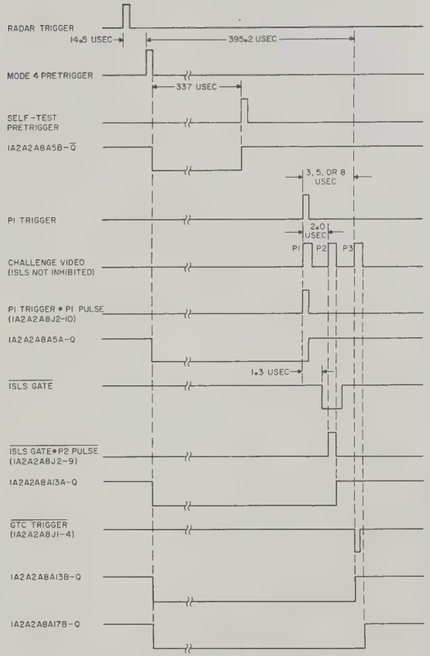
A — DELAY LINE TIME-SHARING



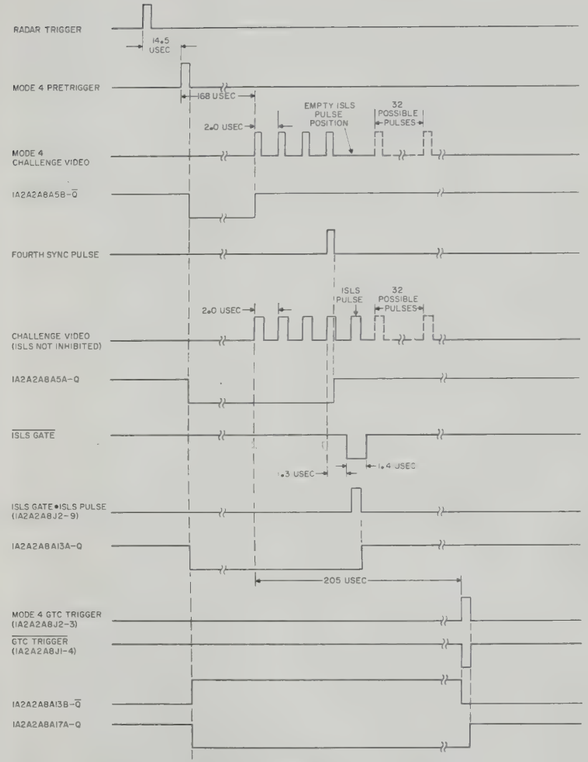
B — P1 AND P3 TRIGGER TIMING



C — ISLS TIMING



D — SIF CHALLENGE SELF-TEST TIMING



E — MODE 4 CHALLENGE SELF-TEST TIMING

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Figure 24-7. Challenge encoding circuit timing diagrams.

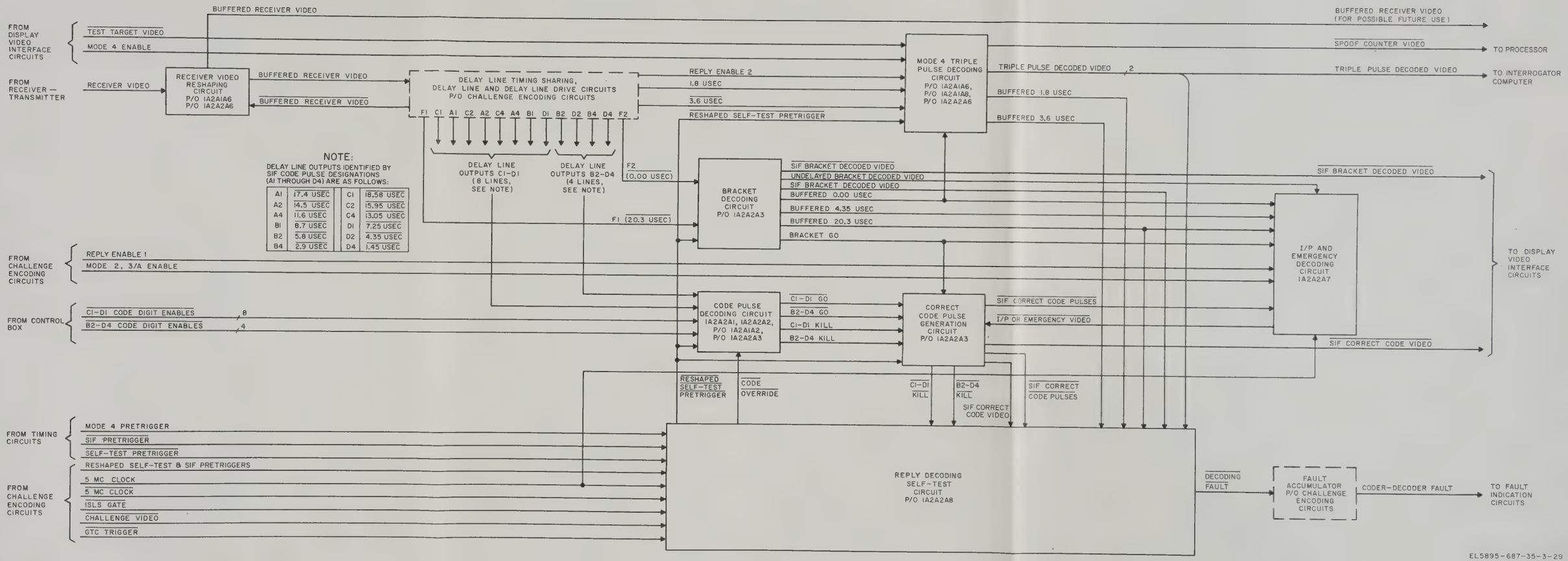


Figure 24-8. Reply decoding circuit functional block diagram.

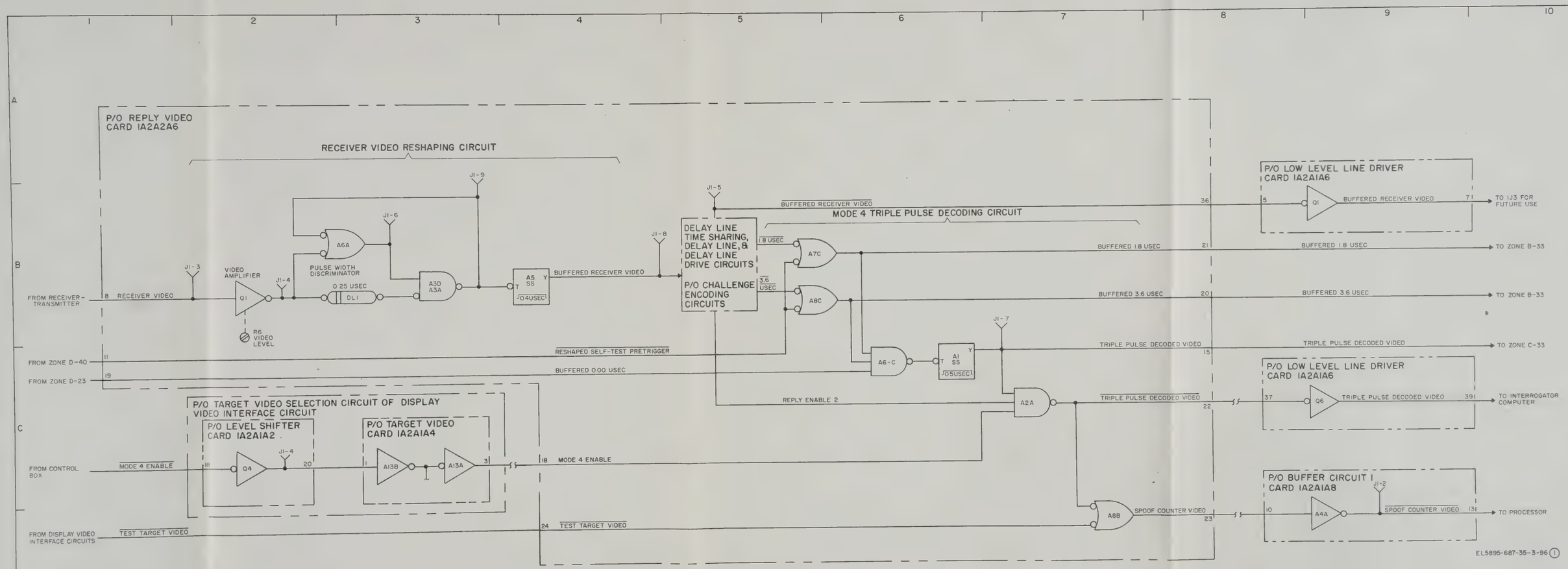


Figure 24-9(1). Reply decoding circuit logic diagram (sheet 1 of 4).

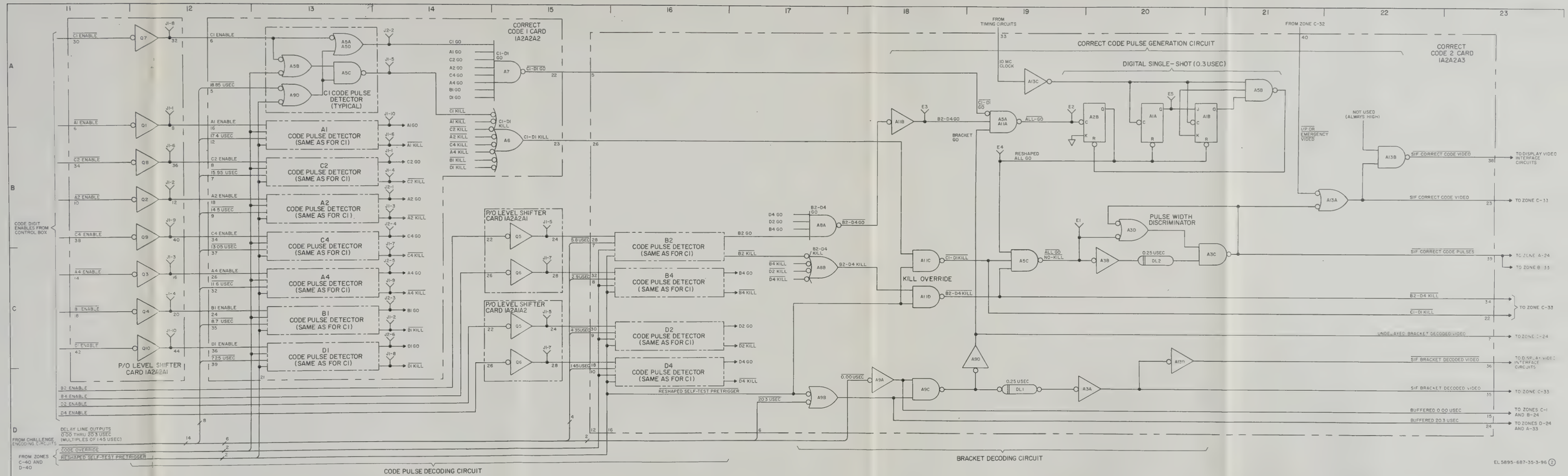


Figure 2-9①. Reply decoding circuit logic diagram (sheet 2 of 4).

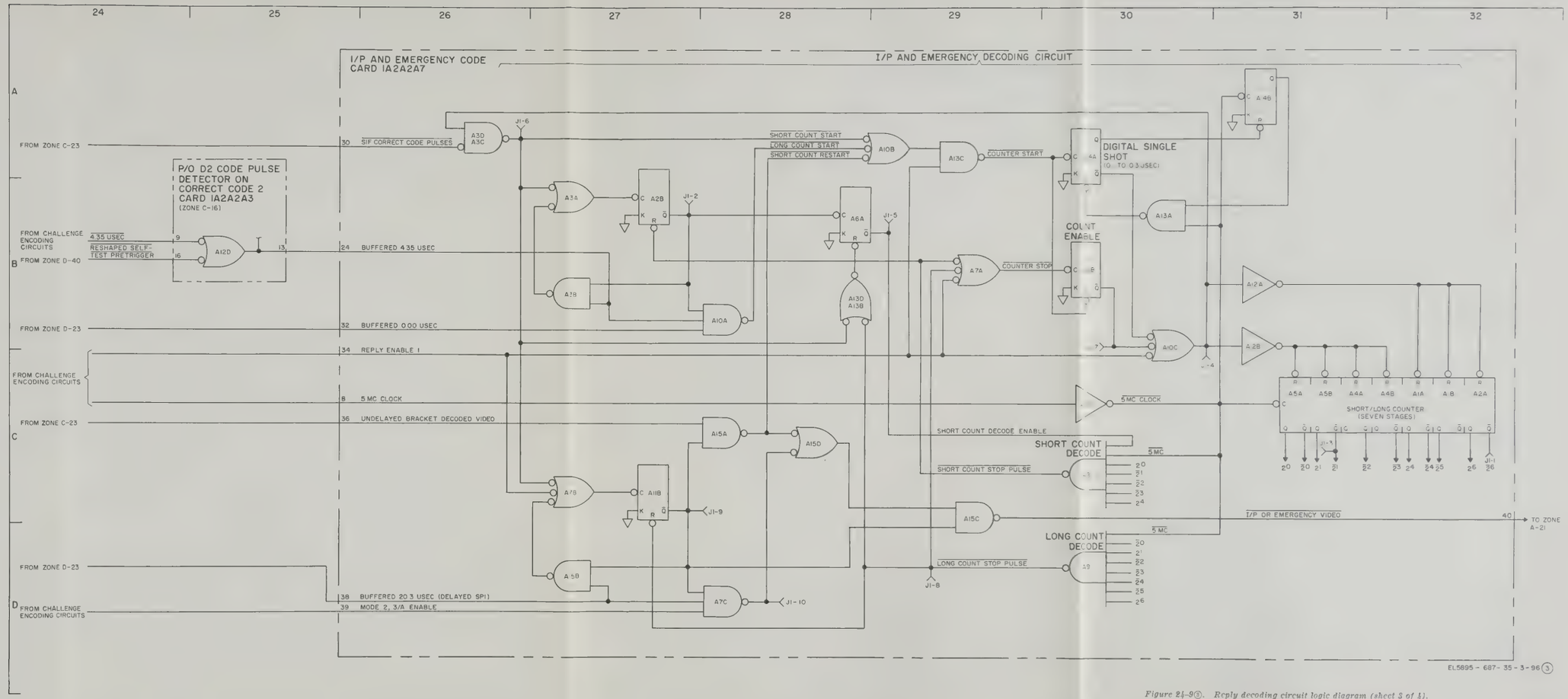


Figure 24-9③. Reply decoding circuit logic diagram (sheet 3 of 4).

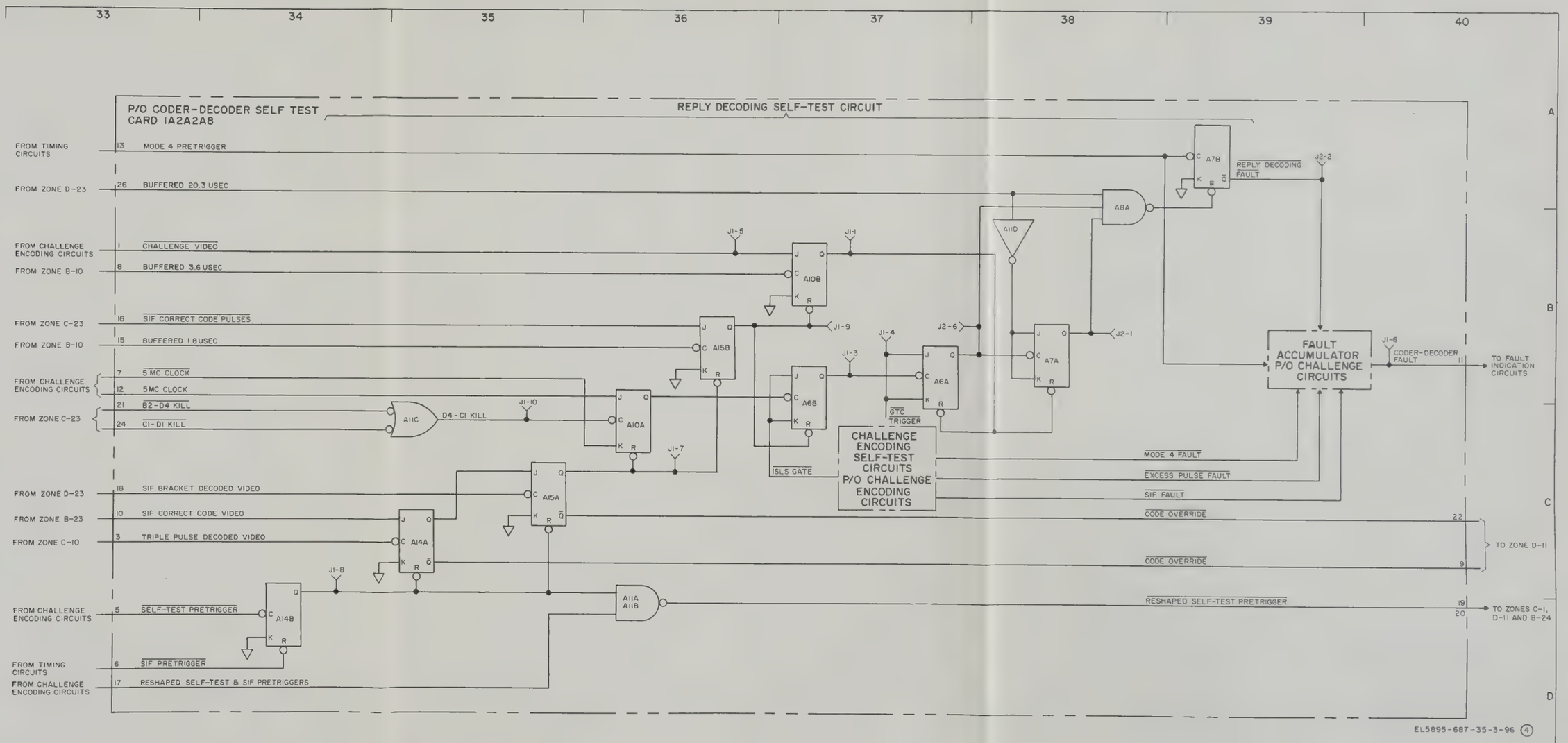
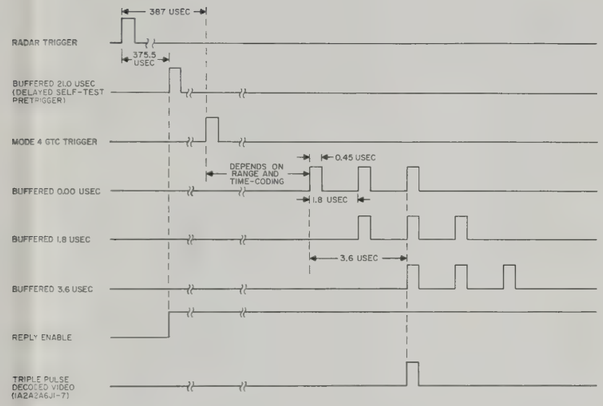
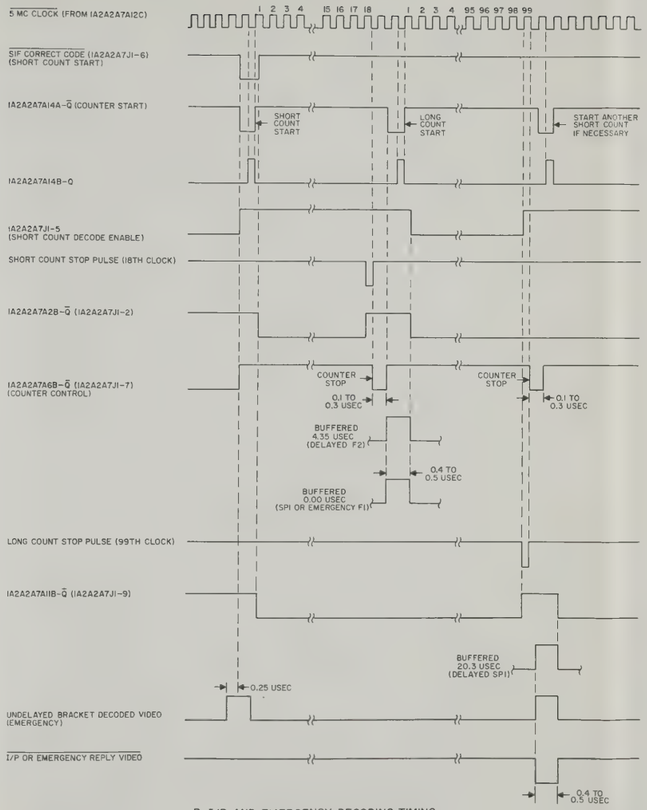


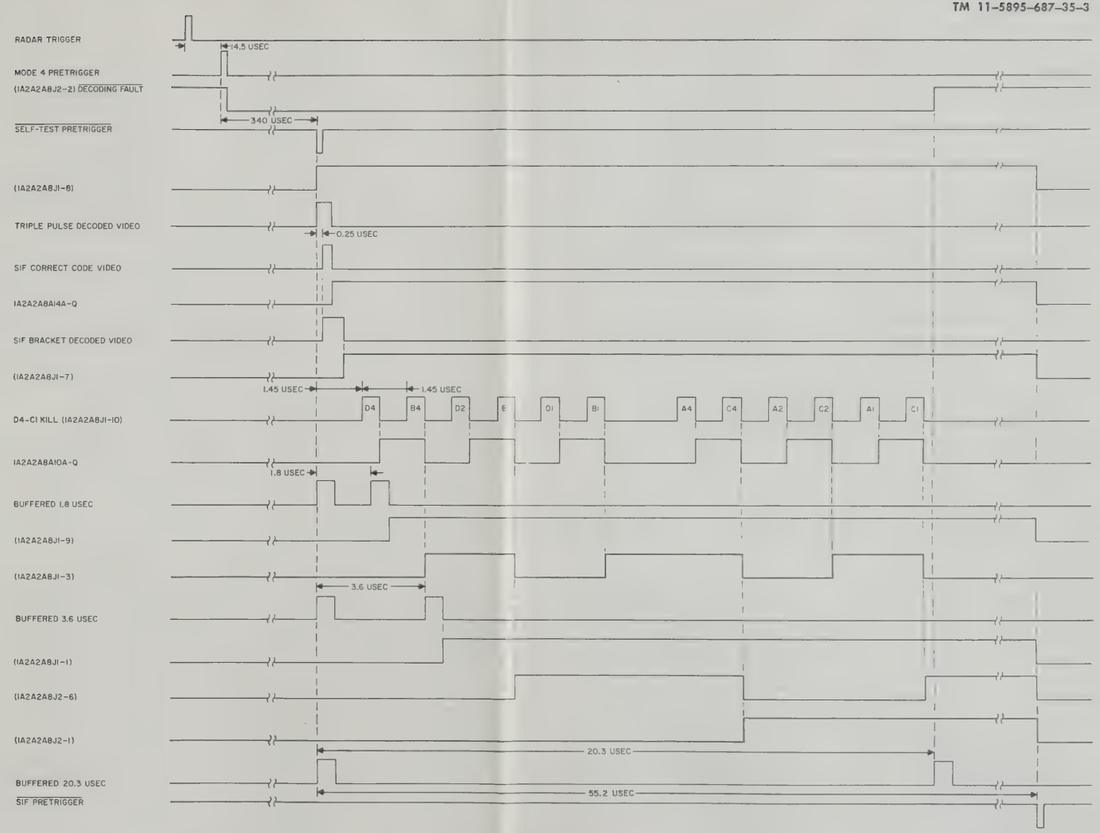
Figure 24-9④. Reply decoding circuit logic diagram (sheet 4 of 4).



A-TRIPLE PULSE DECODING TIMING



B-I/P AND EMERGENCY DECODING TIMING



C-REPLY DECODING SELF-TEST TIMING

EL5895-687-35-3-31

Figure 24-10. Reply decoding circuit timing diagrams.

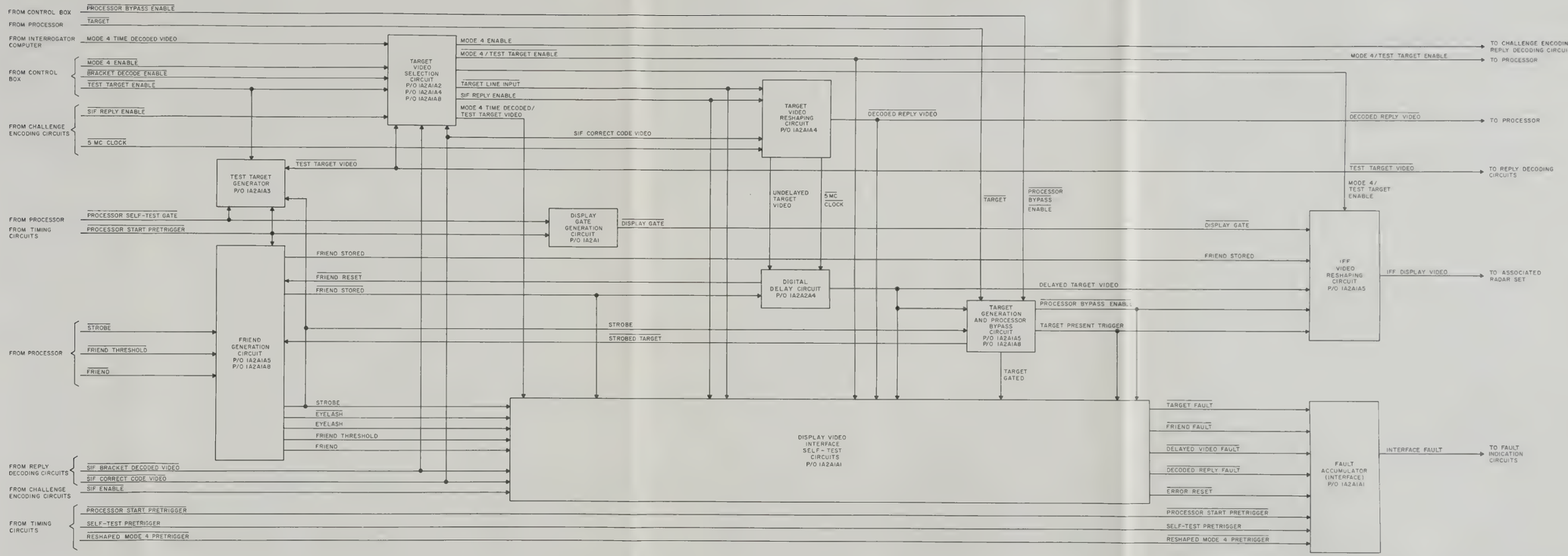


Figure 24-11. Display video interface circuit functional block diagram.

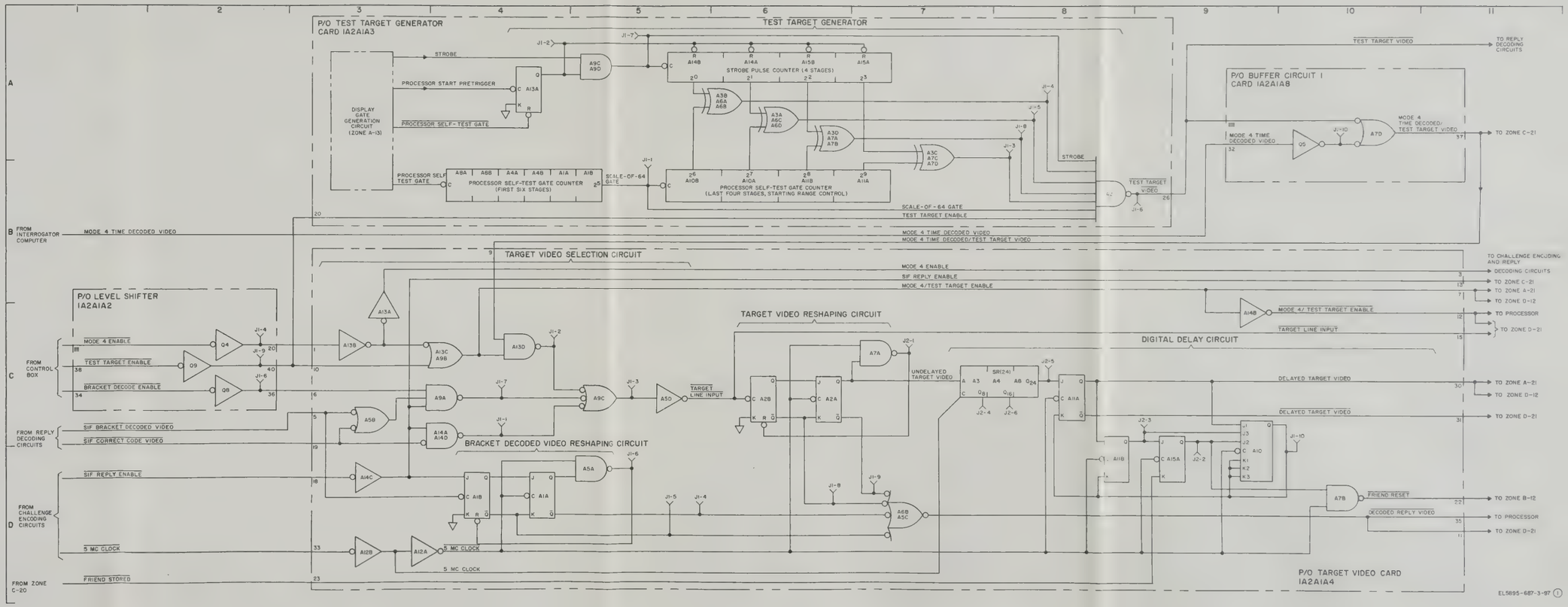


Figure 24-12①. Display video interface circuit logic diagram (sheet 1 of 3).

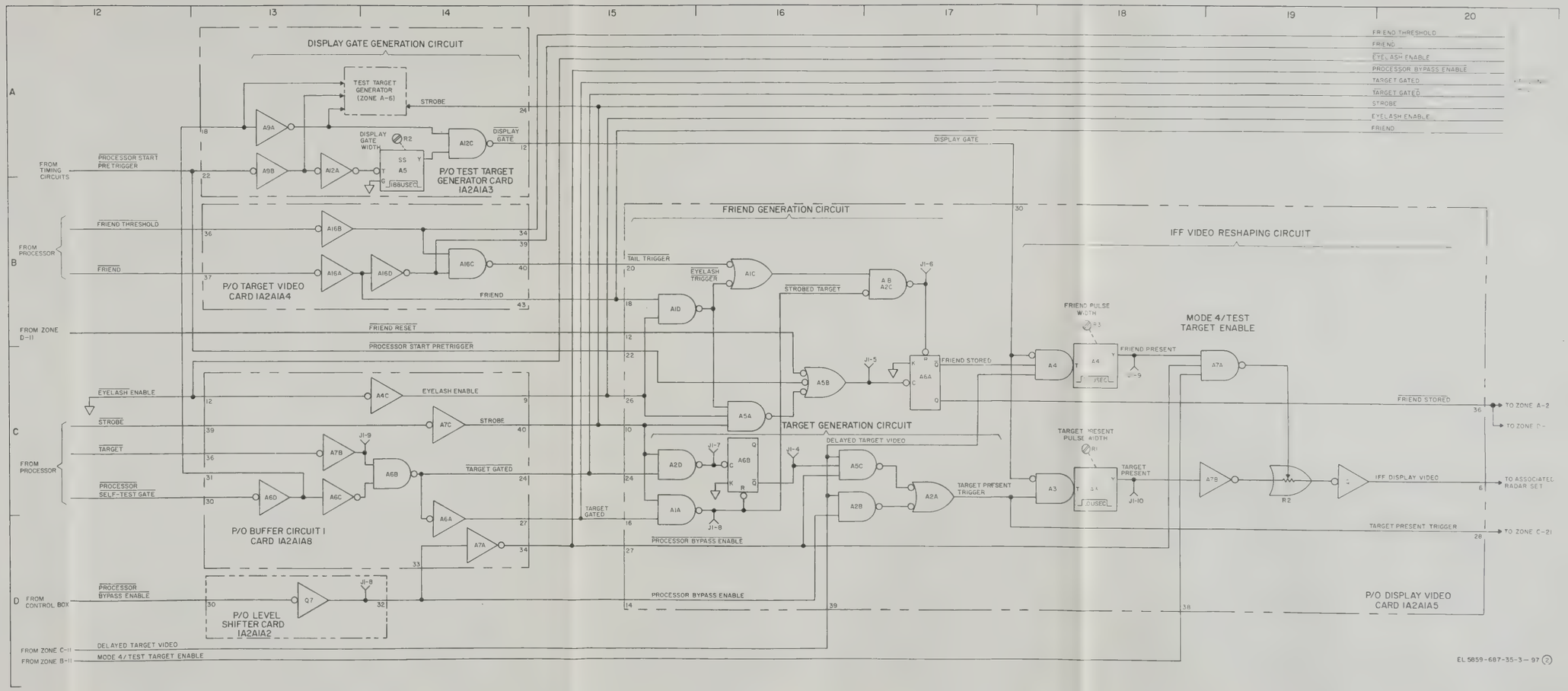


Figure 24-12 (2). Display video interface circuit logic diagrams (sheet 2 of 31).

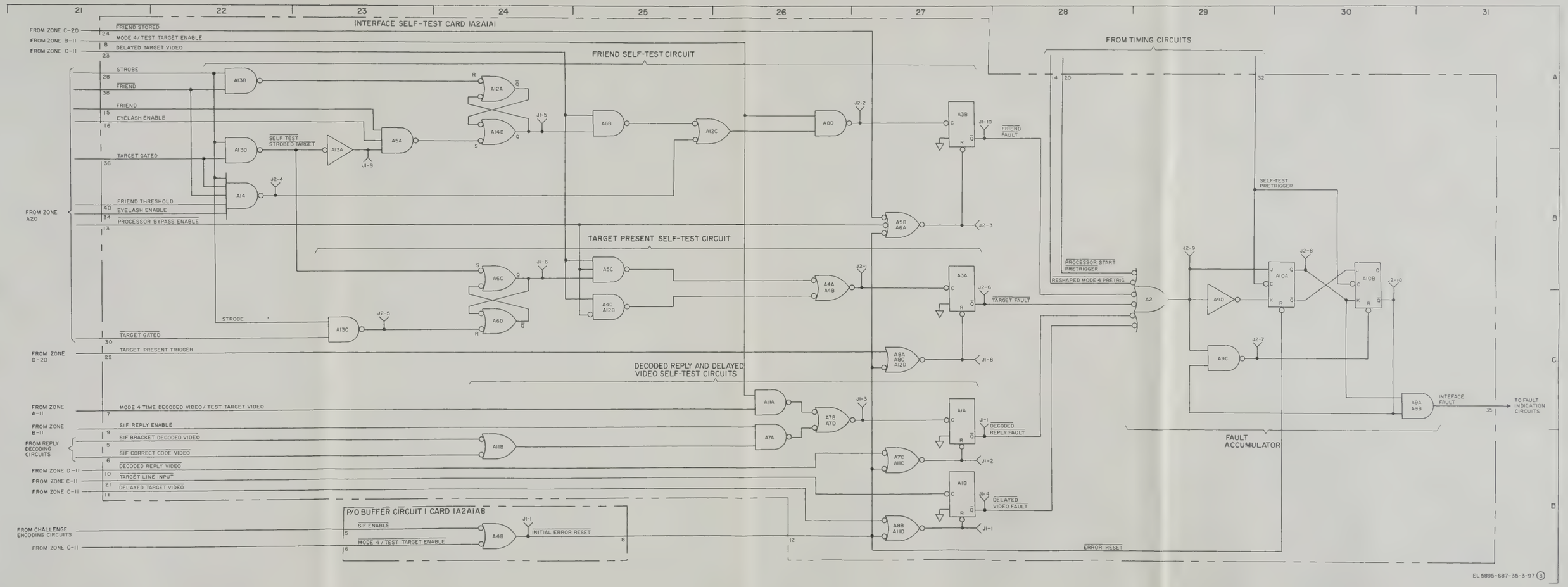


Figure 24-12③. Display video interface circuit logic diagram (sheet 3 of 3).

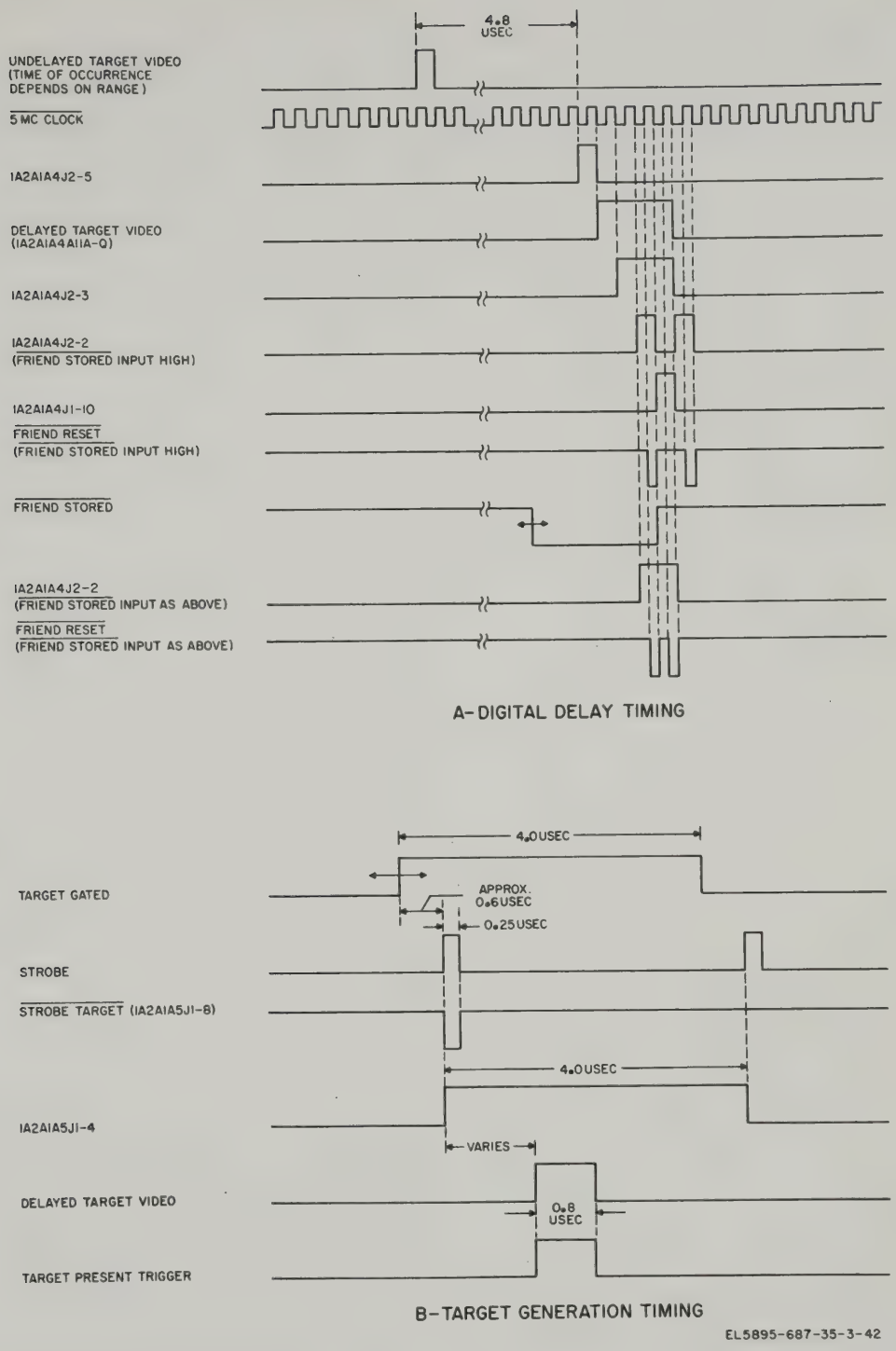


Figure 24-13. Display video interface circuit timing diagrams.

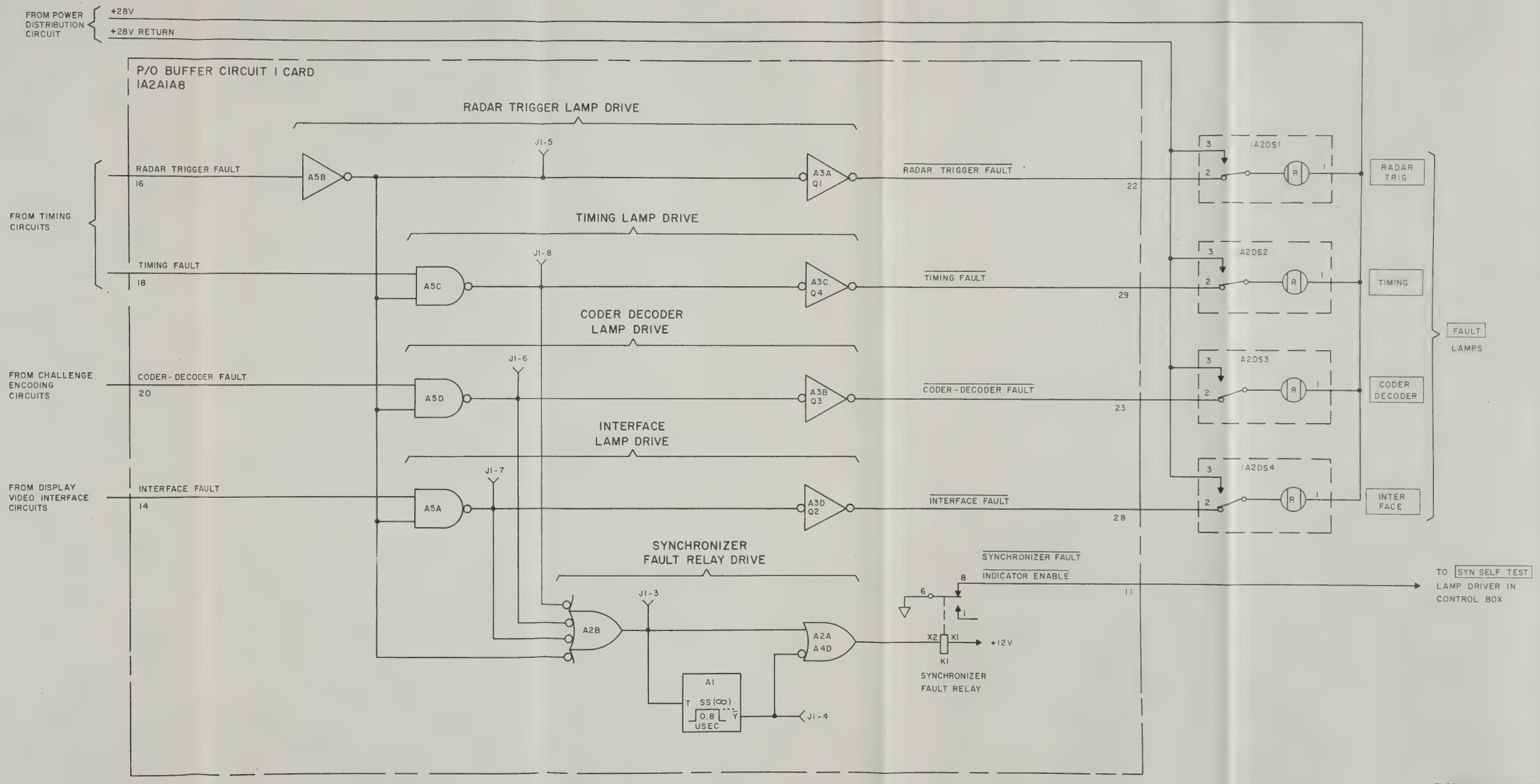


Figure 24-14. Fault indication circuit logic diagram.

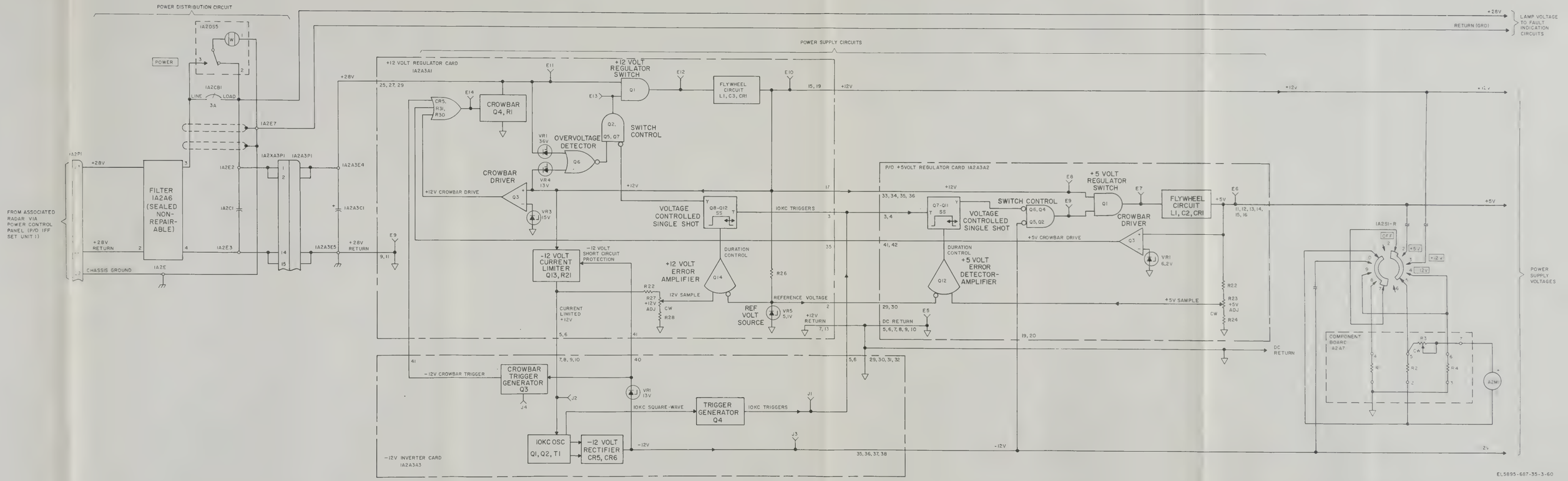
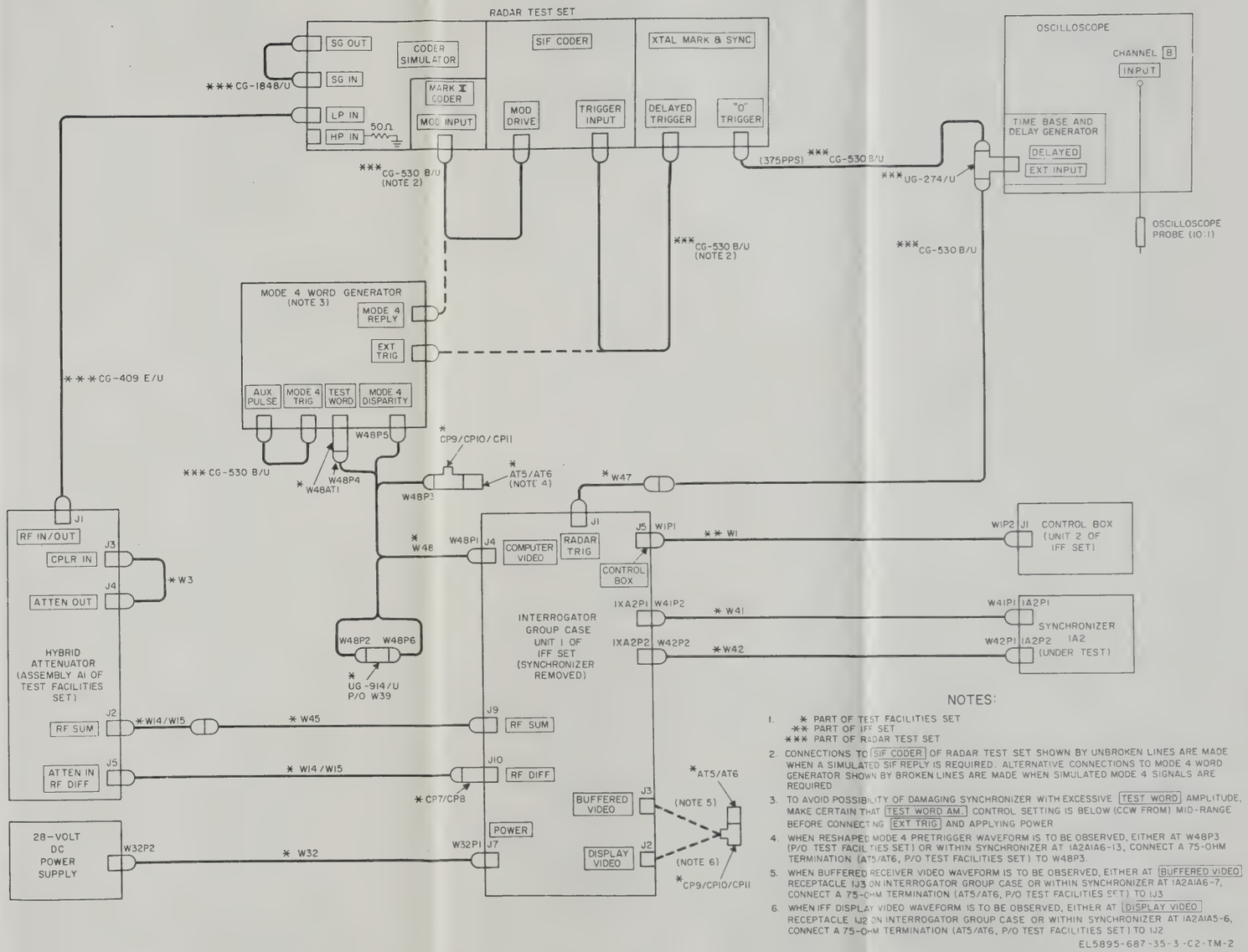


Figure 24-15. Power supply and power distribution circuit logical block diagram.



NOTES:

1. * PART OF TEST FACILITIES SET
   ** PART OF IFF SET
   *** PART OF RADAR TEST SET
2. CONNECTIONS TO SIF CODER OF RADAR TEST SET SHOWN BY UNBROKEN LINES ARE MADE WHEN A SIMULATED SIF REPLY IS REQUIRED. ALTERNATIVE CONNECTIONS TO MODE 4 WORD GENERATOR SHOWN BY BROKEN LINES ARE MADE WHEN SIMULATED MODE 4 SIGNALS ARE REQUIRED.
3. TO AVOID POSSIBILITY OF DAMAGING SYNCHRONIZER WITH EXCESSIVE TEST WORD AMPLITUDE, MAKE CERTAIN THAT TEST WORD AM. CONTROL SETTING IS BELOW (CCW FROM) MID-RANGE BEFORE CONNECTING EXT TRIG AND APPLYING POWER.
4. WHEN RESHAPED MODE 4 PRETRIGGER WAVEFORM IS TO BE OBSERVED, EITHER AT W48P3 (P/O TEST FACILITIES SET) OR WITHIN SYNCHRONIZER AT 1A2A1A6-13, CONNECT A 75-OHM TERMINATION (AT5/AT6, P/O TEST FACILITIES SET) TO W48P3.
5. WHEN BUFFERED RECEIVER VIDEO WAVEFORM IS TO BE OBSERVED, EITHER AT BUFFERED VIDEO RECEPTACLE J3 ON INTERROGATOR GROUP CASE OR WITHIN SYNCHRONIZER AT 1A2A1A6-7, CONNECT A 75-OHM TERMINATION (AT5/AT6, P/O TEST FACILITIES SET) TO J3.
6. WHEN IFF DISPLAY VIDEO WAVEFORM IS TO BE OBSERVED, EITHER AT DISPLAY VIDEO RECEPTACLE J2 ON INTERROGATOR GROUP CASE OR WITHIN SYNCHRONIZER AT 1A2A1A5-6, CONNECT A 75-OHM TERMINATION (AT5/AT6, P/O TEST FACILITIES SET) TO J2.

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Figure 24-16. Synchronizer test equipment and connections.

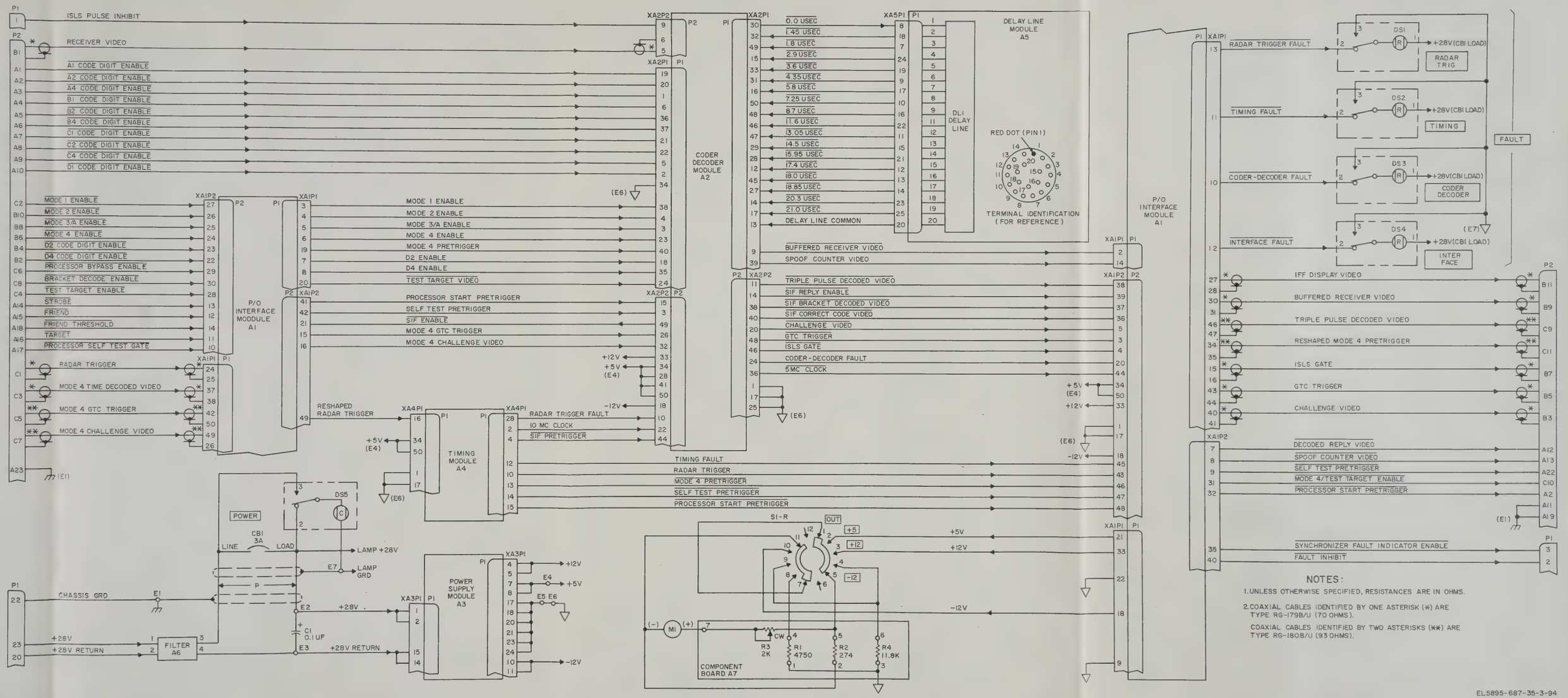


Figure 24-17. Synchronizer 1A2 schematic diagram.

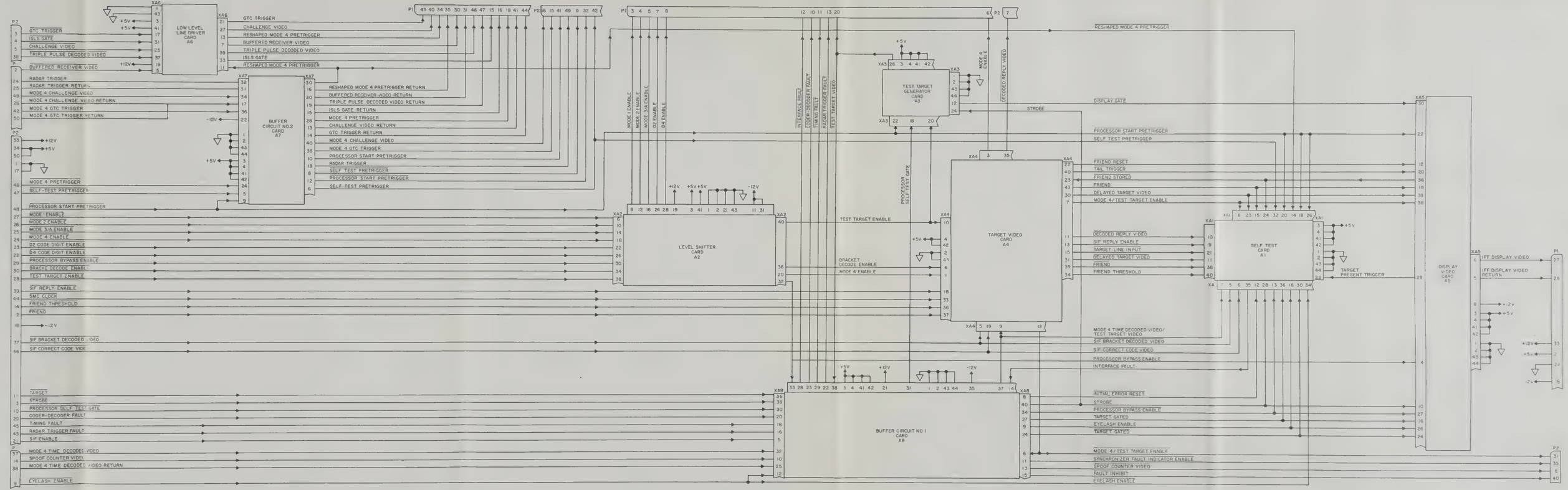
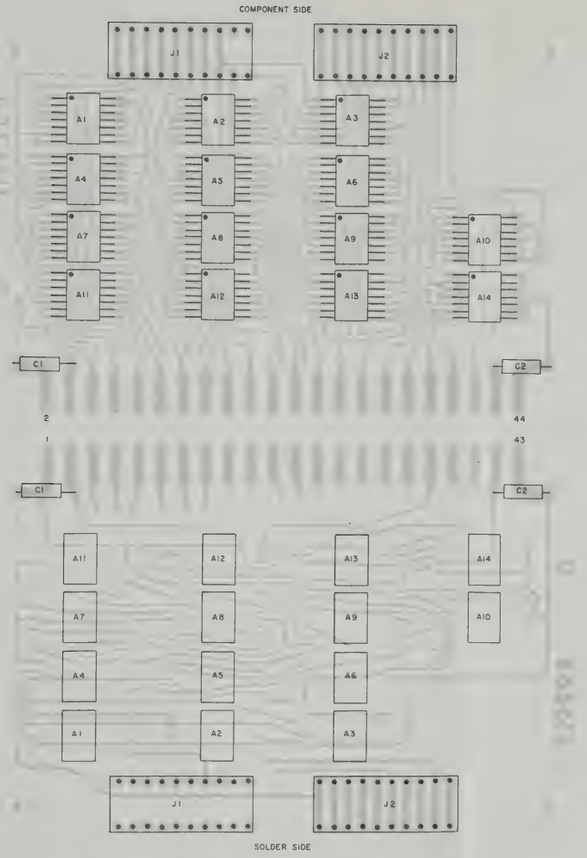
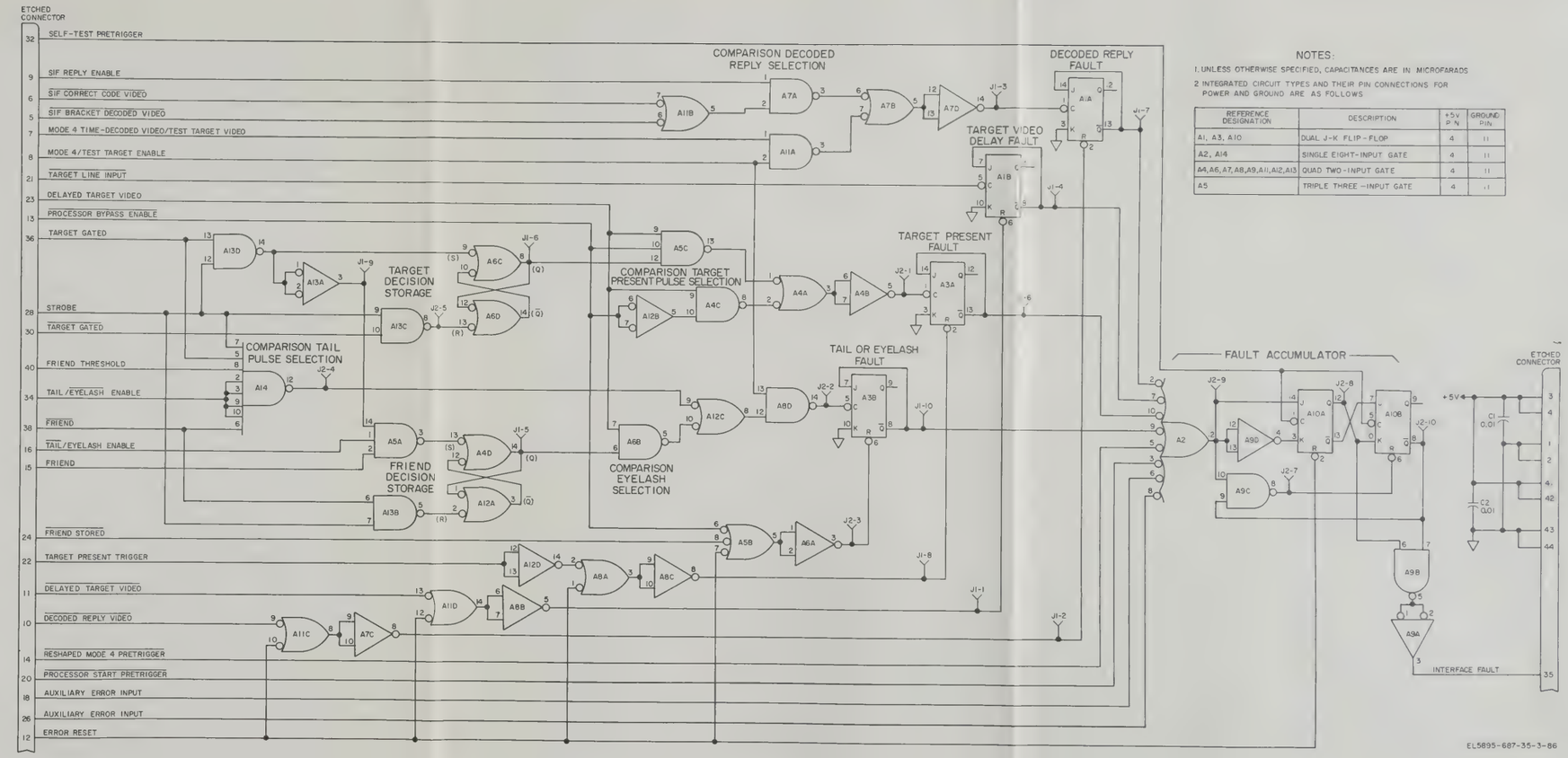


Figure 24-18. Interface module 1A2A1 schematic diagram.



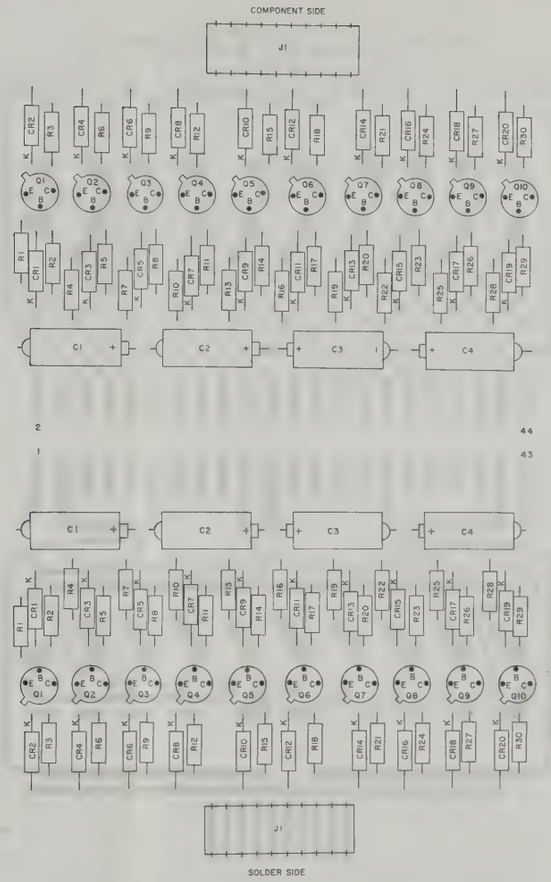


NOTES:

1. UNLESS OTHERWISE SPECIFIED, CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V P/N	GROUND PIN
A1, A3, A10	DUAL J-K FLIP-FLOP	4	11
A2, A14	SINGLE EIGHT-INPUT GATE	4	11
A4, A6, A7, A8, A9, A11, A12, A13	QUAD TWO-INPUT GATE	4	11
A5	TRIPLE THREE-INPUT GATE	4	14

Figure 24-19. Interface self-test card 1A2A1A1 schematic diagram.



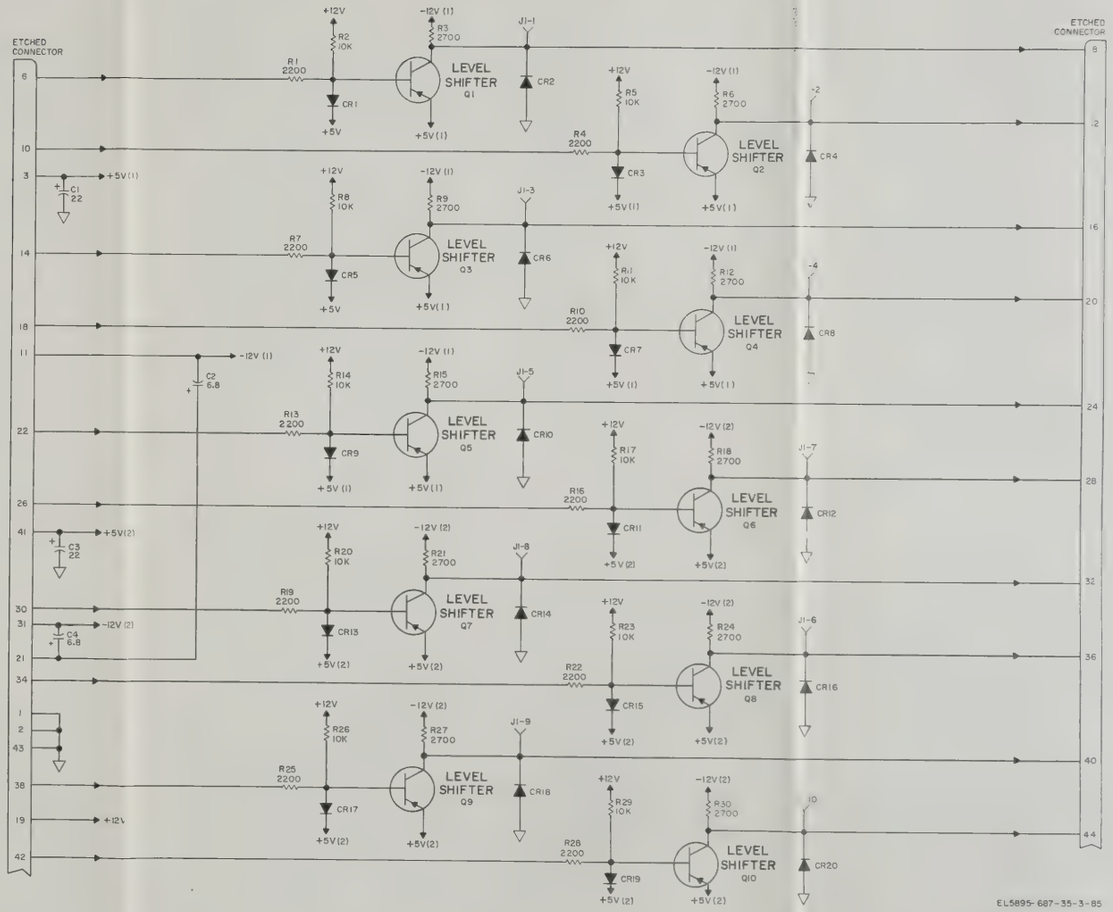


Figure 24-20. Level shifter card 1A2A1A2 or 1A2A2A1 schematic diagram.

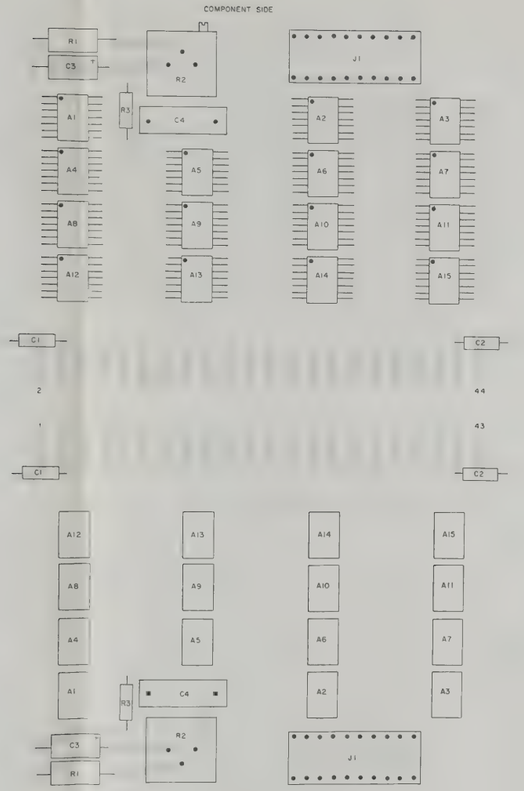
NOTES:

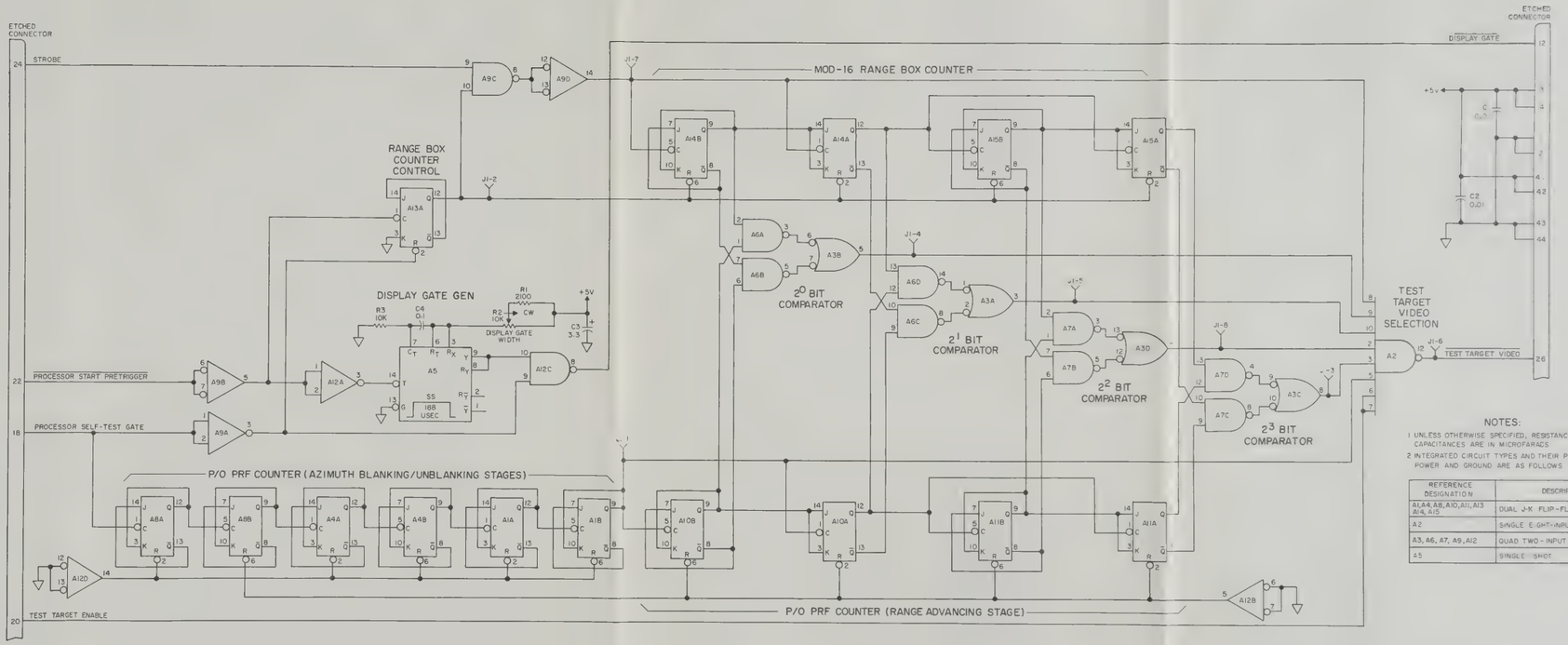
1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN UF
2. ALL TRANSISTORS ARE TYPE 2N2907
3. ALL DIODES ARE TYPE IN914
4. SIGNAL NAMES FOR 1A2A2A1 CARD ARE AS FOLLOWS

SIGNAL	PINS
A1 CODE DIGIT ENABLE	6 TO 8
A2 CODE DIGIT ENABLE	10 TO 12
A4 CODE DIGIT ENABLE	14 TO 16
B1 CODE DIGIT ENABLE	18 TO 20
B2 CODE DIGIT ENABLE	22 TO 24
B4 CODE DIGIT ENABLE	26 TO 28
C1 CODE DIGIT ENABLE	30 TO 32
C2 CODE DIGIT ENABLE	34 TO 36
C4 CODE DIGIT ENABLE	38 TO 40
D1 CODE DIGIT ENABLE	42TO44

5. SIGNAL NAMES FOR 1A2A1A2 CARD ARE AS FOLLOWS

SIGNAL	PINS
MODE 1 ENABLE	6 TO 8
MODE 2 ENABLE	10 TO 12
MODE 3/A ENABLE	14 TO 16
MODE 4 ENABLE	18 TO 20
D2 CODE DIGIT ENABLE	22TO 24
D4 CODE DIGIT ENABLE	26TO 28
PROCESSOR BYPASS ENABLE	30 TO 32
BRACKET DECODE ENABLE	34 TO 36
TEST TARGET ENABLE	38TO 40
NOT USED	42TO44





NOTES:
1 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS
2 INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V P.N.	GROUND P.N.
A1,A4,A8,A10,A11,A13 A14, A15	DUAL J-K FLIP-FLOP	4	11
A2	SINGLE EIGHT-INPUT GATE	8	
A3, A6, A7, A9, A12	QUAD TWO-INPUT GATE	4	
A5	SINGLE ONE-SHOT	4	

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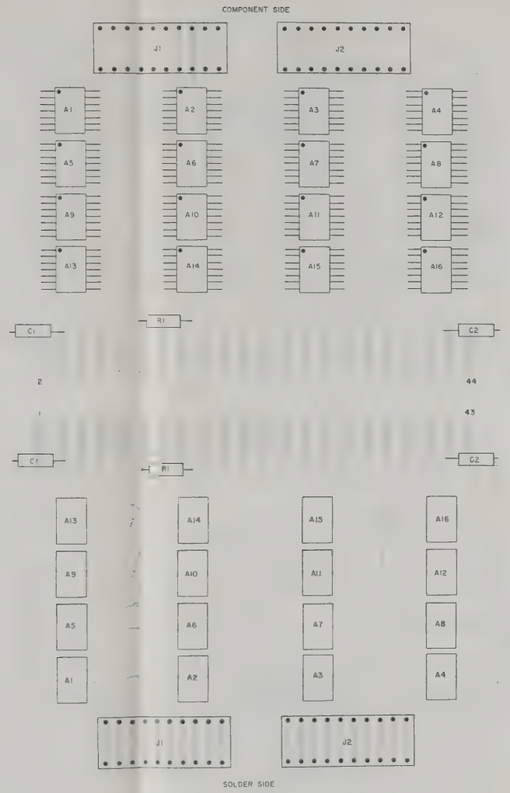
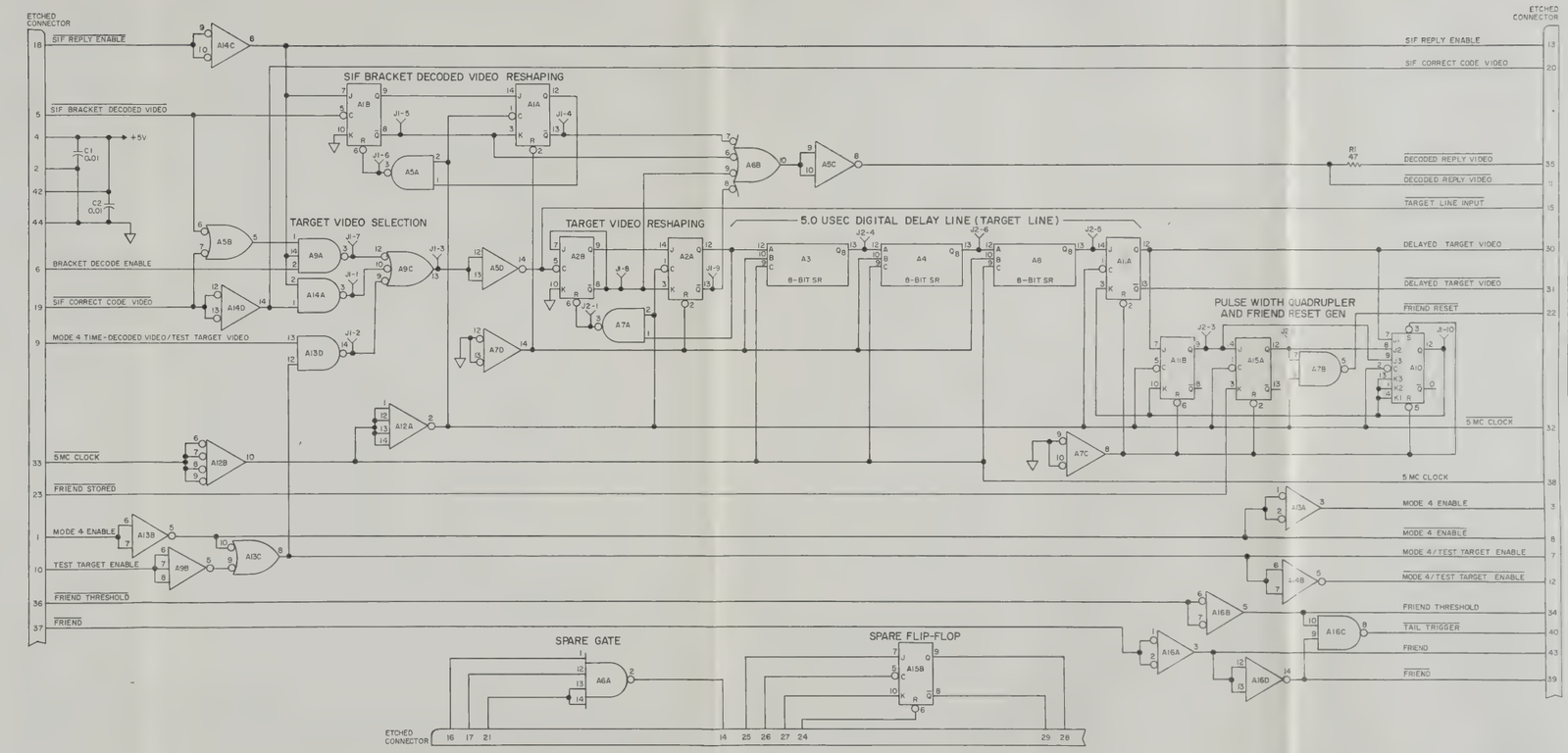
Figure 24-21. Test target generator card 1A2A1A3 schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A2, A11, A15	DUAL J-K FLIP-FLOP	4	11
A3, A4, A8	EIGHT-BIT SHIFT REGISTER	4	11
A5, A7, A13, A14, A16	QUAD TWO-INPUT GATE	4	11
A6	DUAL FOUR-INPUT GATE	4	11
A9	TRIPLE THREE-INPUT GATE	4	11
A10	JJJ-KKK FLIP-FLOP	4	11
A12	DUAL FOUR-INPUT GATE	4	11

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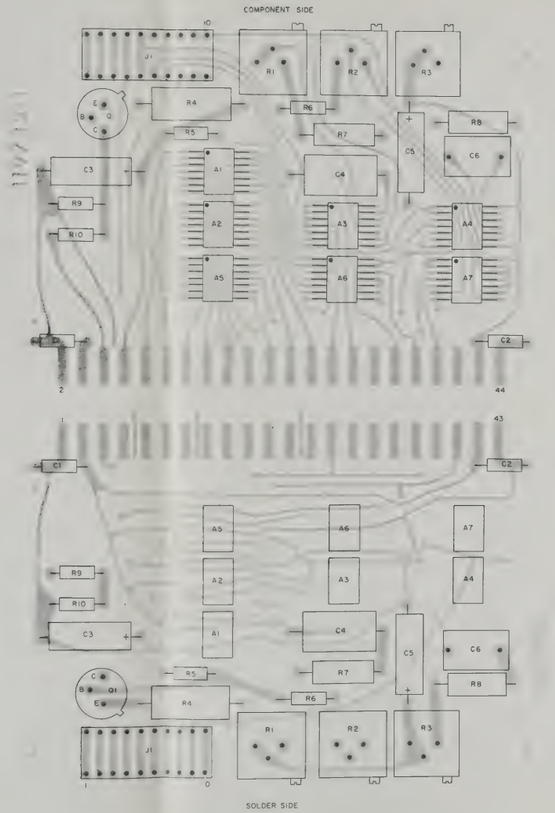
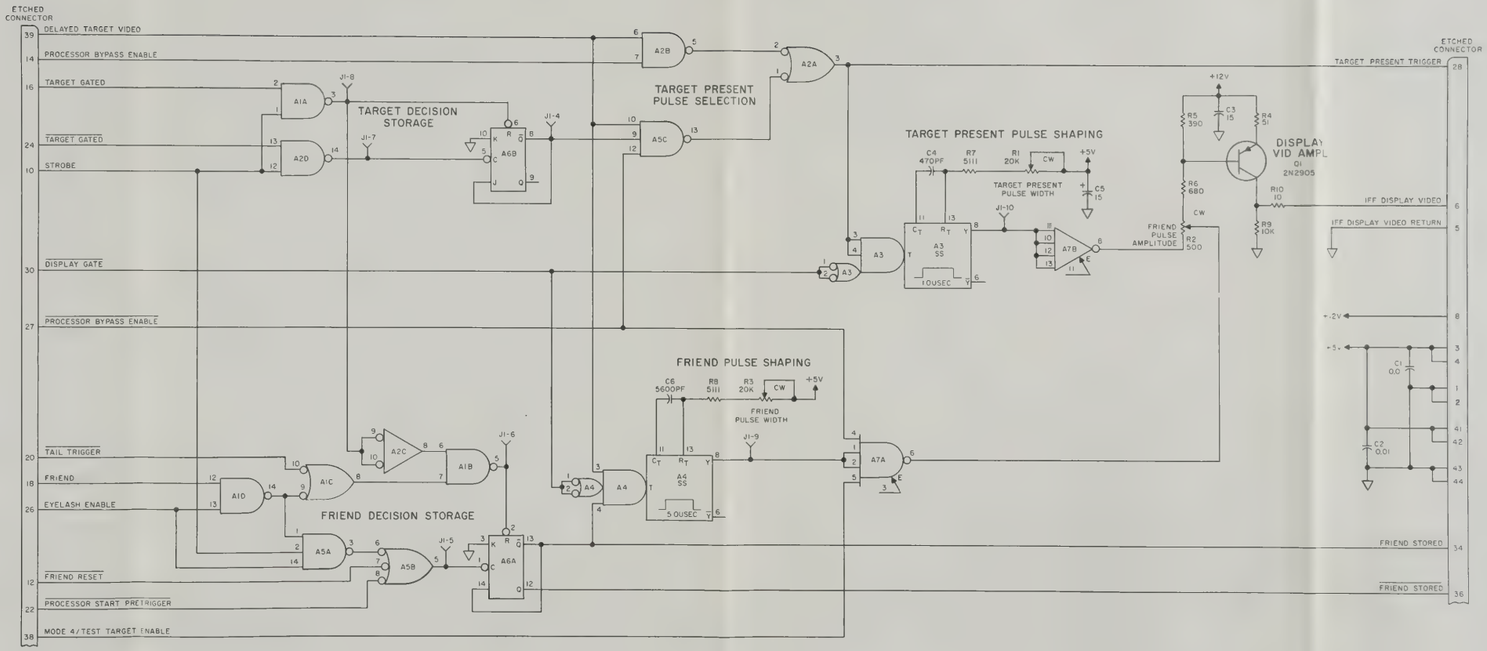
Figure 24-22. Target video card 1A2A1A4 schematic diagram.





NOTES

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A2	QUADRUPLE TWO-INPUT GATE	4	11
A3, A4	RETRIGGERABLE SINGLE SHOT	14	7
A5	TRIPLE THREE-INPUT GATE	4	11
A6	DUAL J-K FLIP-FLOP	4	11
A7	DUAL EXPANDABLE FOUR-INPUT GATE	14	7

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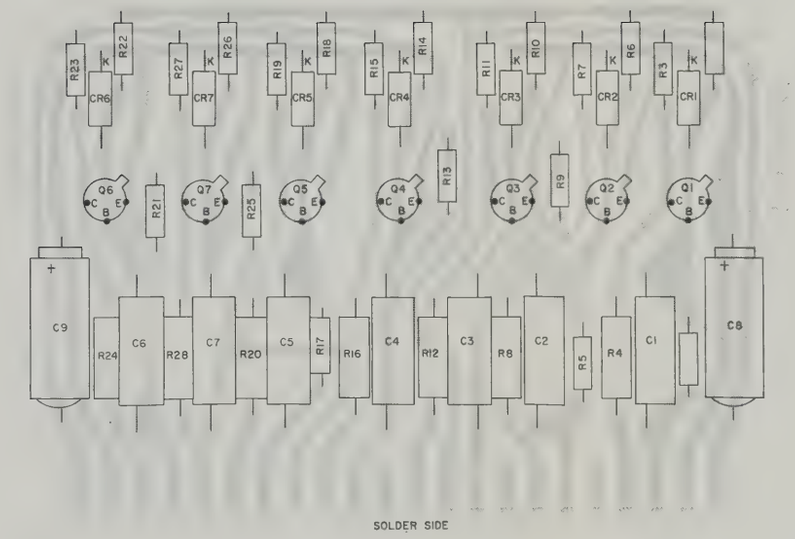
Figure 24-23. Display video card 1A2A1A5 schematic diagram.



NOTE:
1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS, CAPACITANCES IN UF

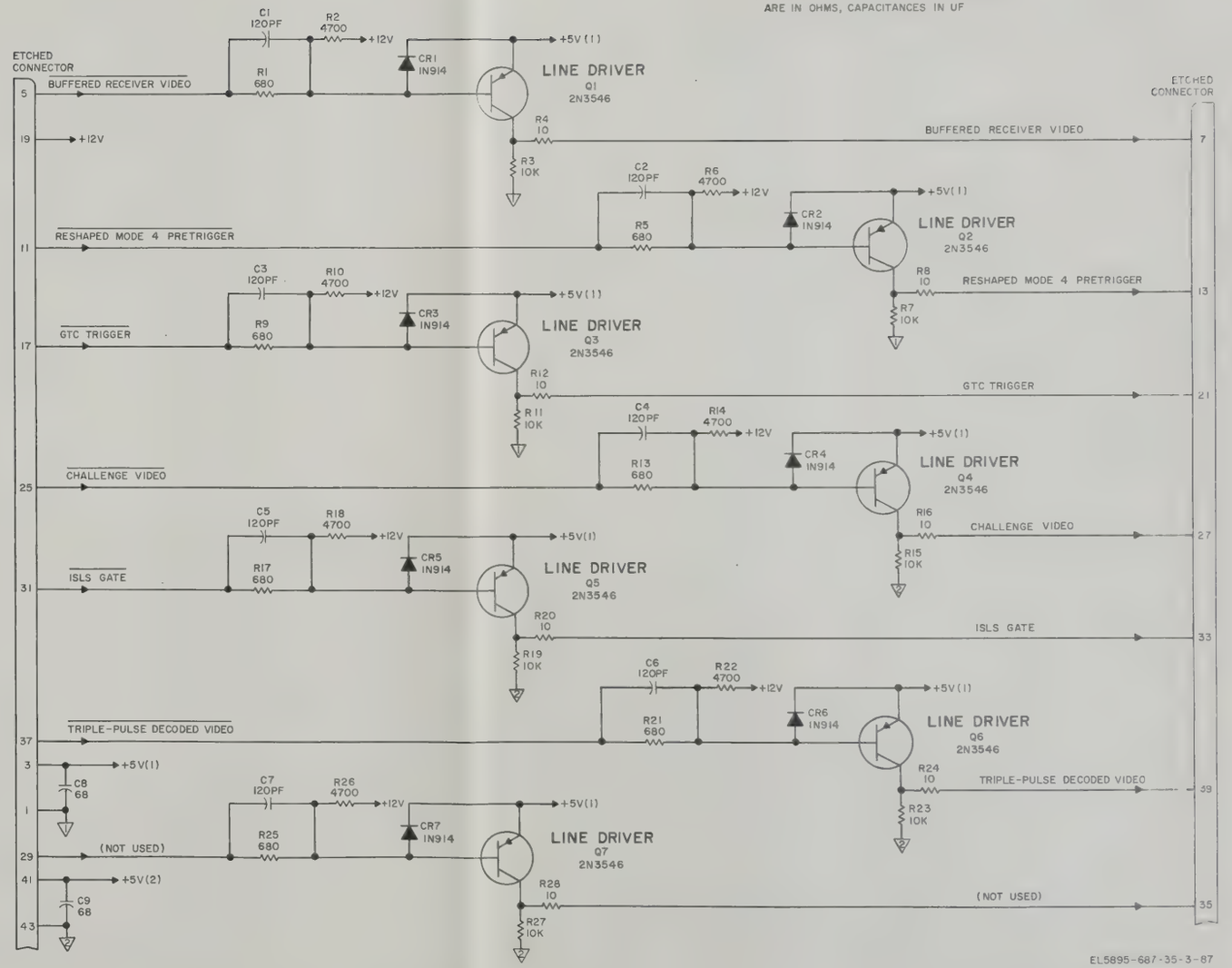
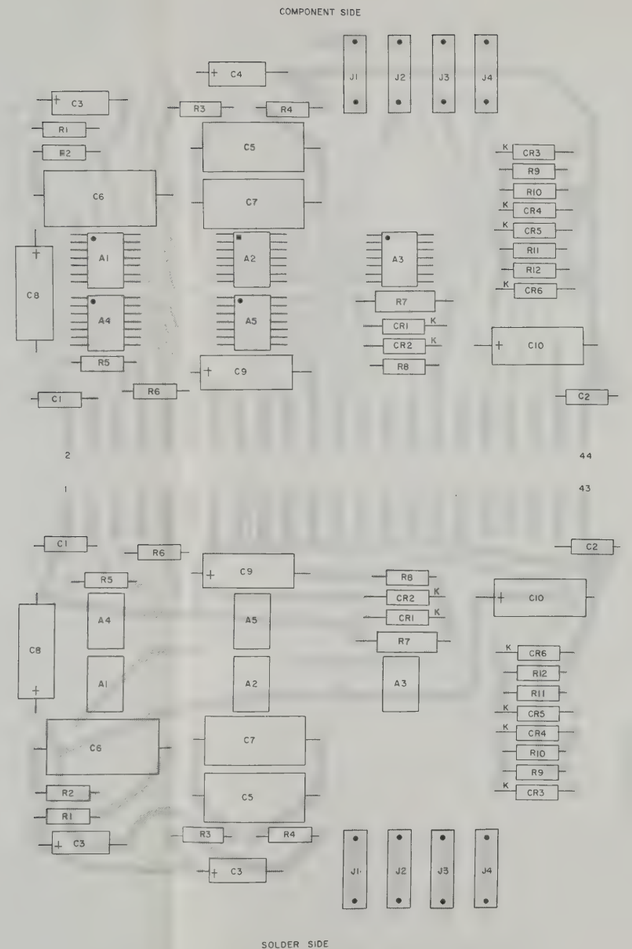
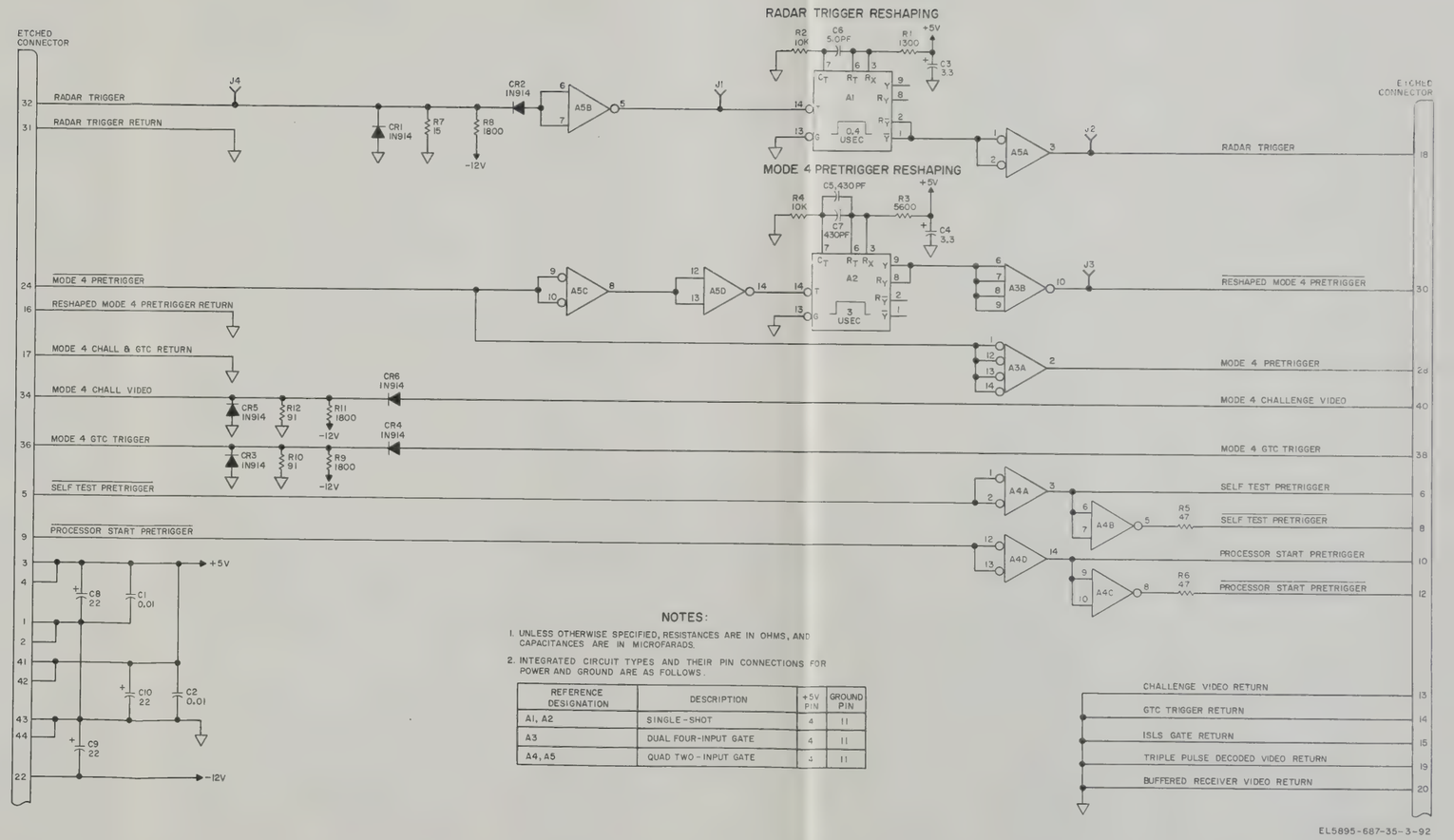


Figure 24-24. Low level line driver card 1A2A1A6 schematic diagram.



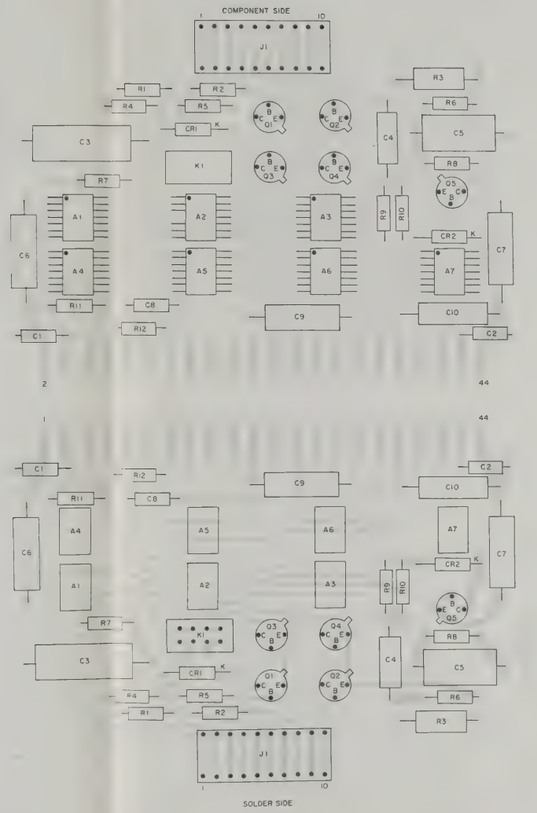


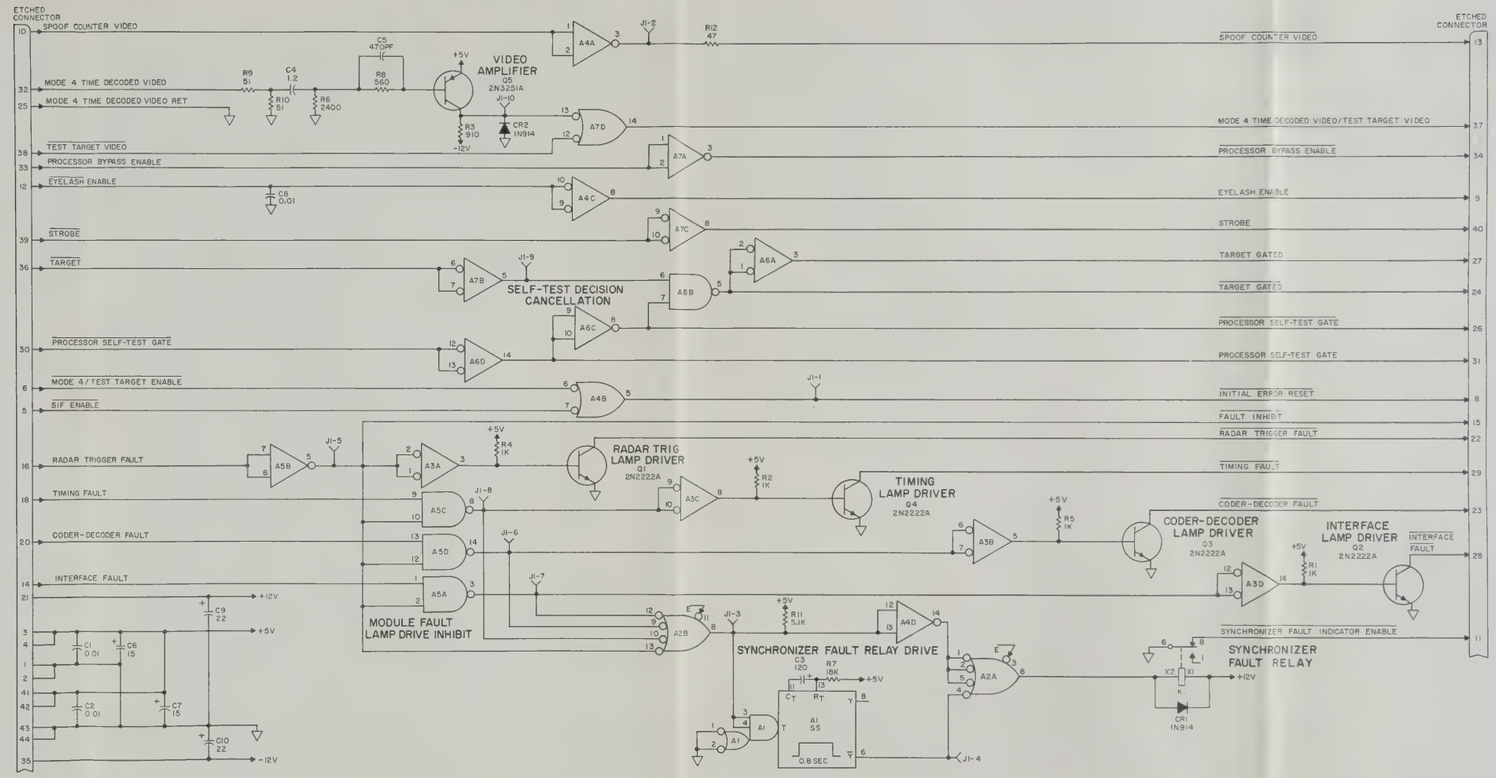
NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS.

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A2	SINGLE-SHOT	4	11
A3	DUAL FOUR-INPUT GATE	4	11
A4, A5	QUAD TWO-INPUT GATE	4	11

Figure 24-25. Buffer circuit 2 card 1A2A1A7 schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1	RETRIGGERABLE-SINGLE SHOT	14	7
A2	DUAL EXPANDABLE FOUR-INPUT GATE	14	7
A3	QUAD TWO-INPUT GATE	4	11
A4, A5, A6, A7	QUAD TWO-INPUT GATE	4	11

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Figure 24-26. Buffer circuit 1 card 1A2A1A8 schematic diagram.

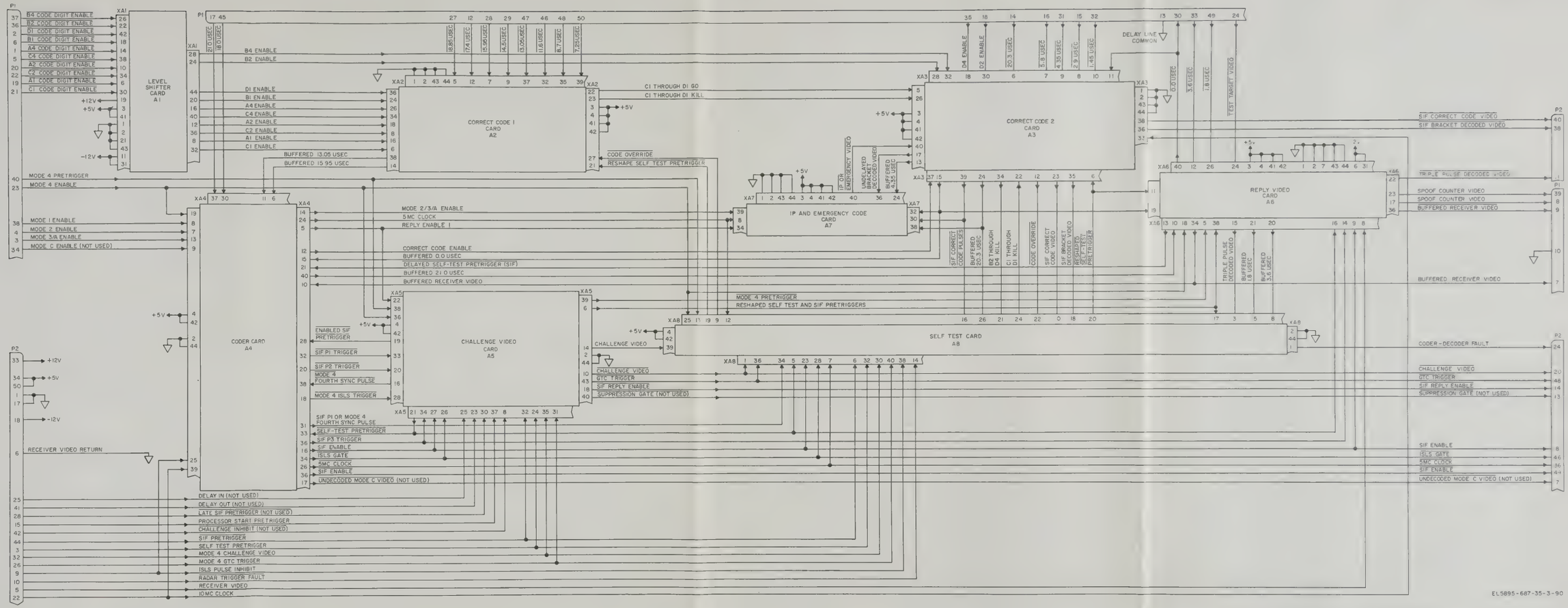
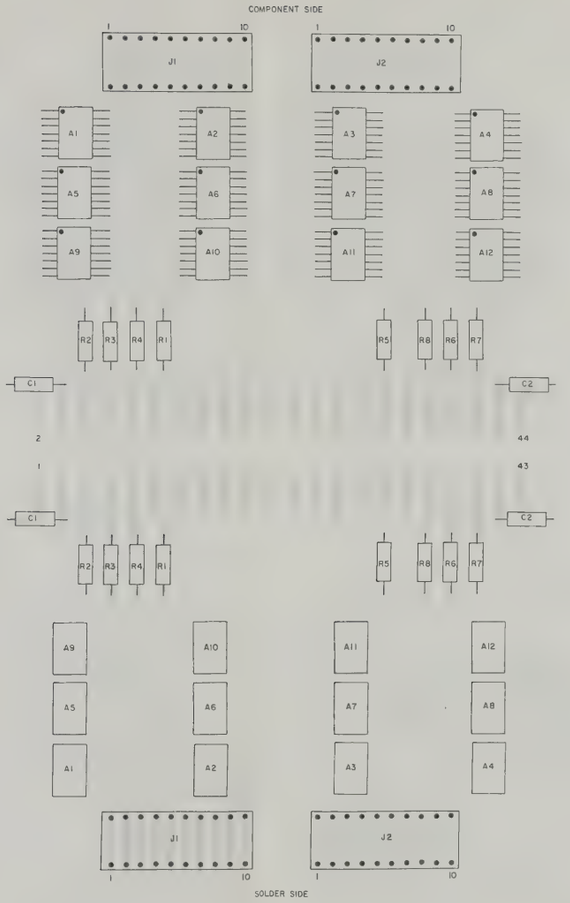
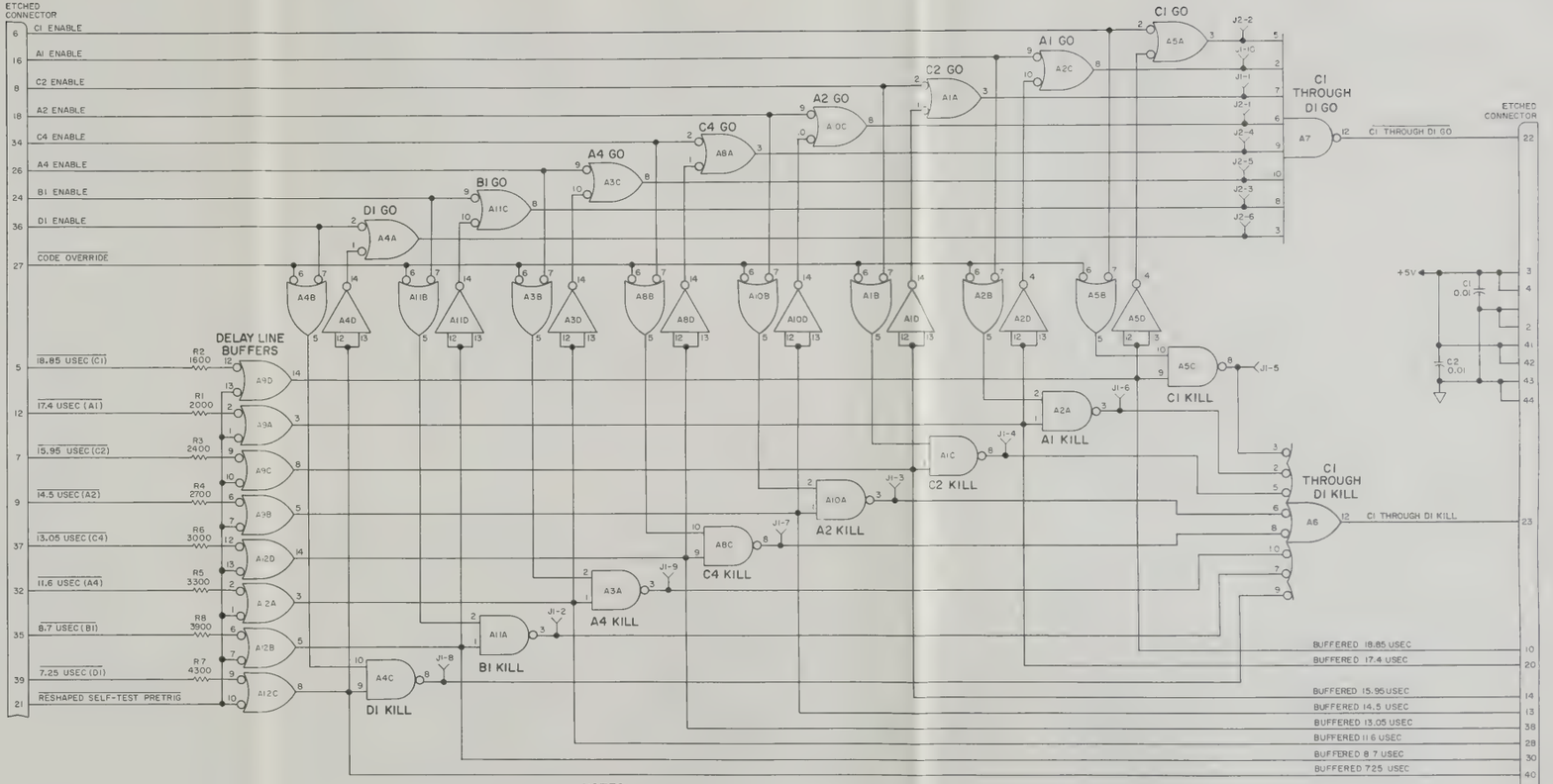


Figure 24-27. Coder-decoder module 1A2A2 schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS:

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1 THROUGH A5	QUAD TWO-INPUT GATE	4	11
A6, A7	SINGLE EIGHT-INPUT GATE	4	11
A8 THROUGH A12	QUAD TWO-INPUT GATE	4	11

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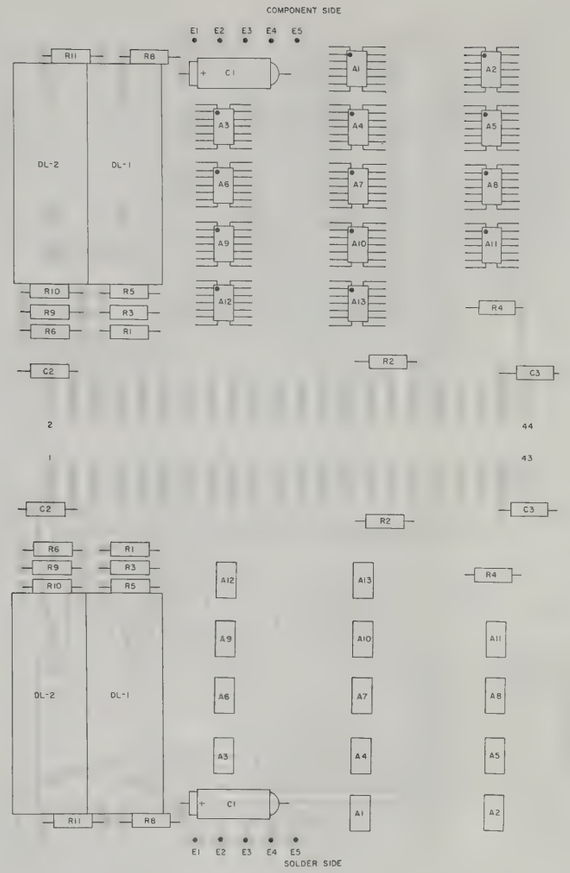
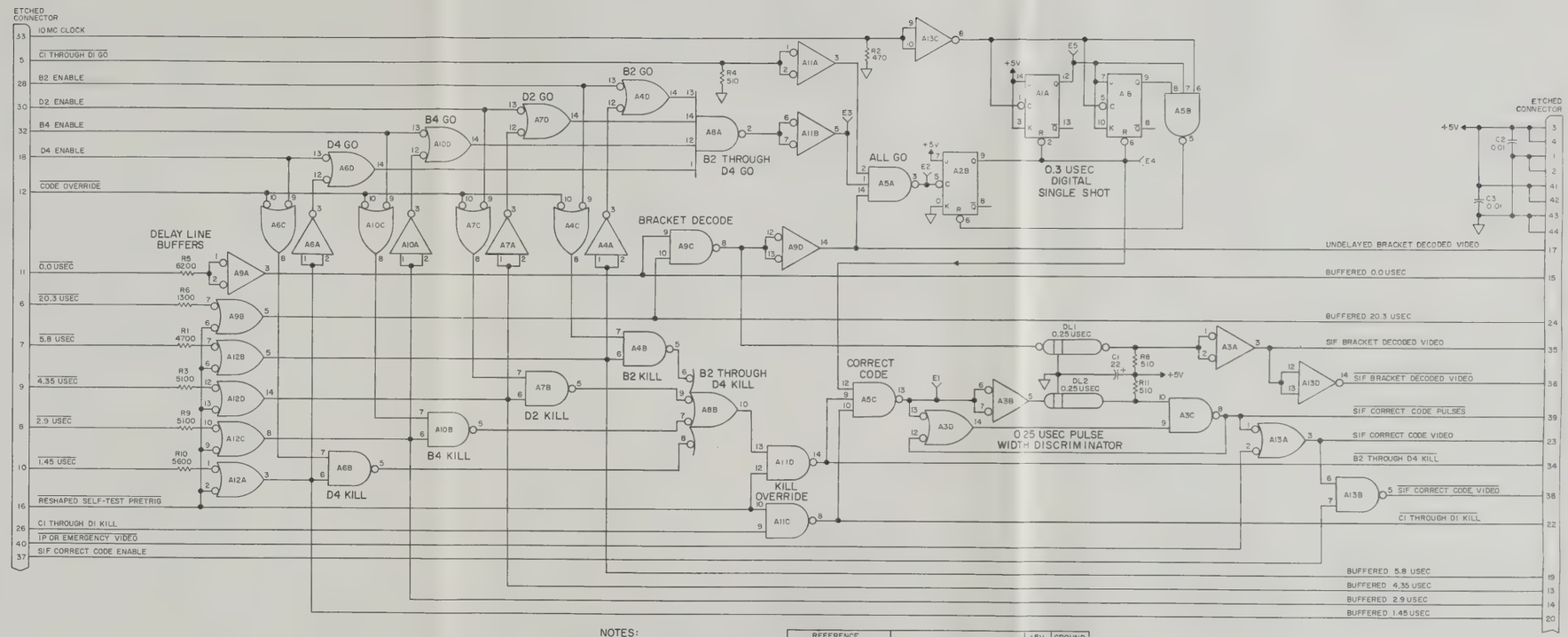
Figure 24-28. Correct code 1 card 1A2A2A2 schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS AND CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS.

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A2	DUAL J-K FLIP-FLOP	4	11
A3, A4, A6, A7, A9	QUAD TWO-INPUT GATE	4	11
A5	TRIPLE THREE-INPUT GATE	4	11
A8	DUAL FOUR-INPUT GATE	4	11
A10, A11, A12, A13	QUAD TWO-INPUT GATE	4	11

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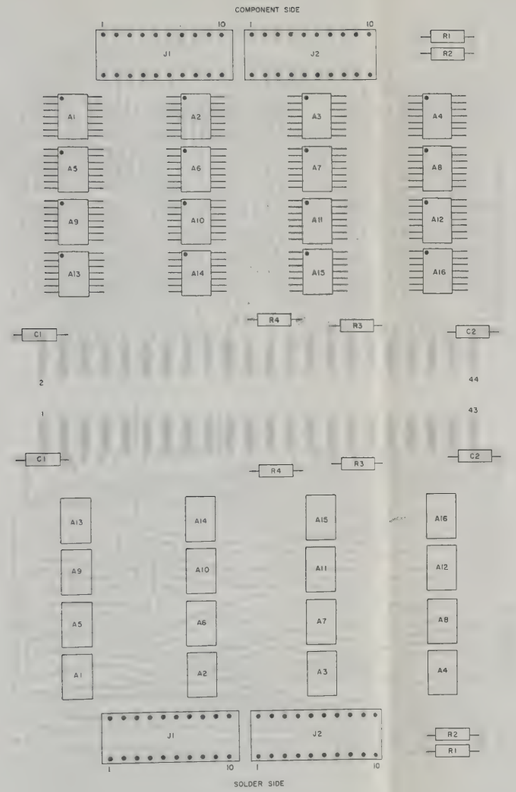
Figure 24-29. Correct code 2 card 1A2A2A3 schematic diagram.



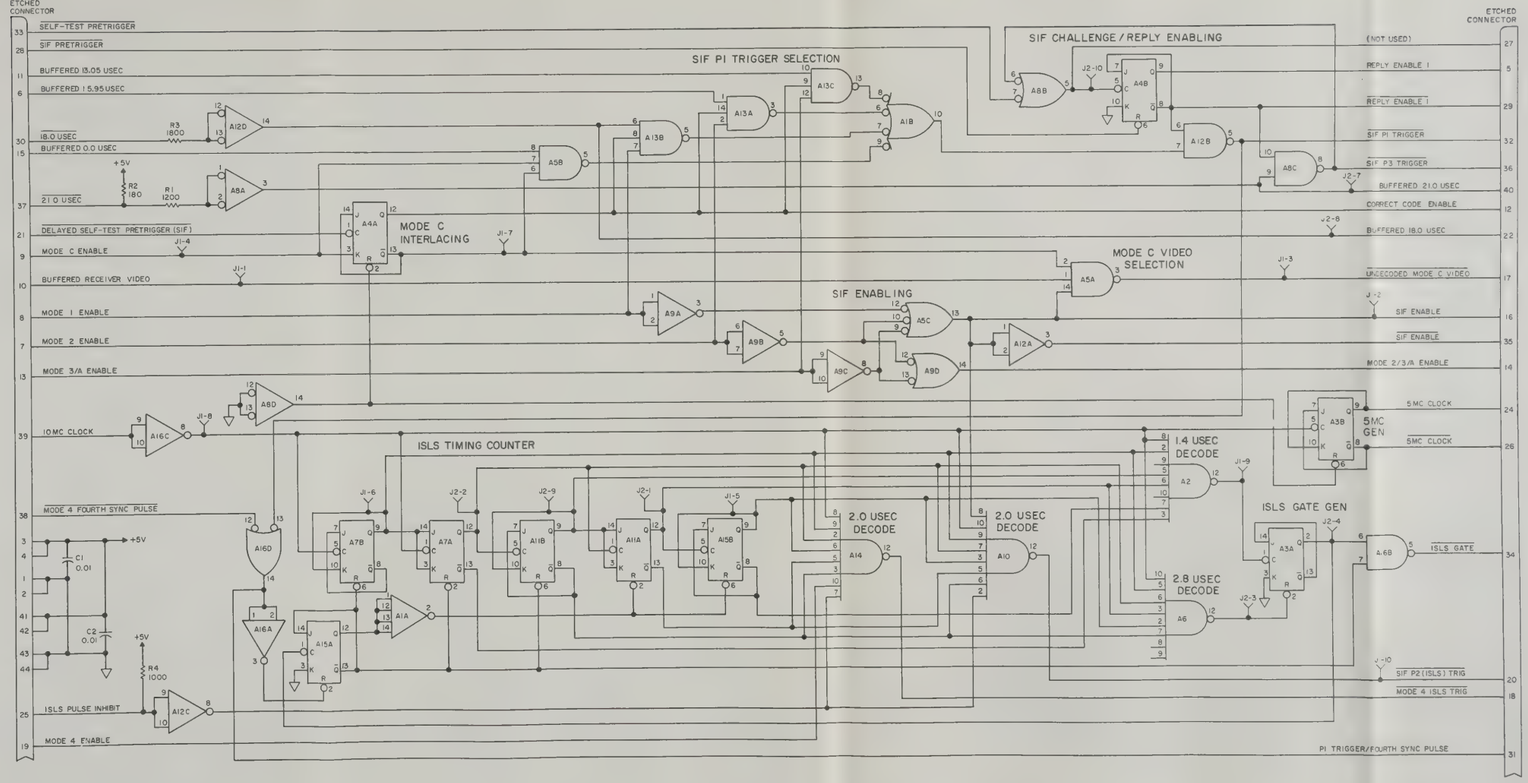


Figure 24-30. Coder card 1A2A2A4 schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1	DUAL FOUR-INPUT GATE	4	11
A2, A6, A10, A14	SINGLE EIGHT-INPUT GATE	4	11
A3, A4, A7, A11, A15	DUAL J-K FLIP-FLOP	4	11
A5, A13	TRIPLE THREE-INPUT GATE	4	11
A8, A9, A12, A16	QUAD TWO-INPUT GATE	4	11

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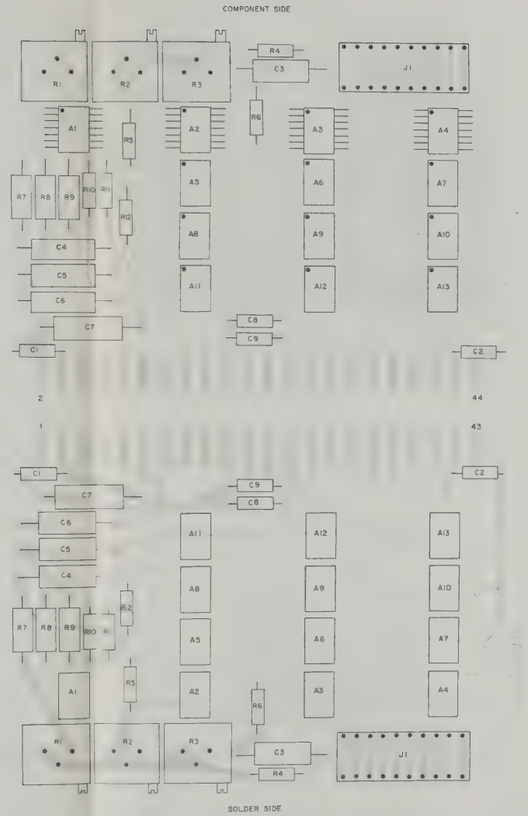

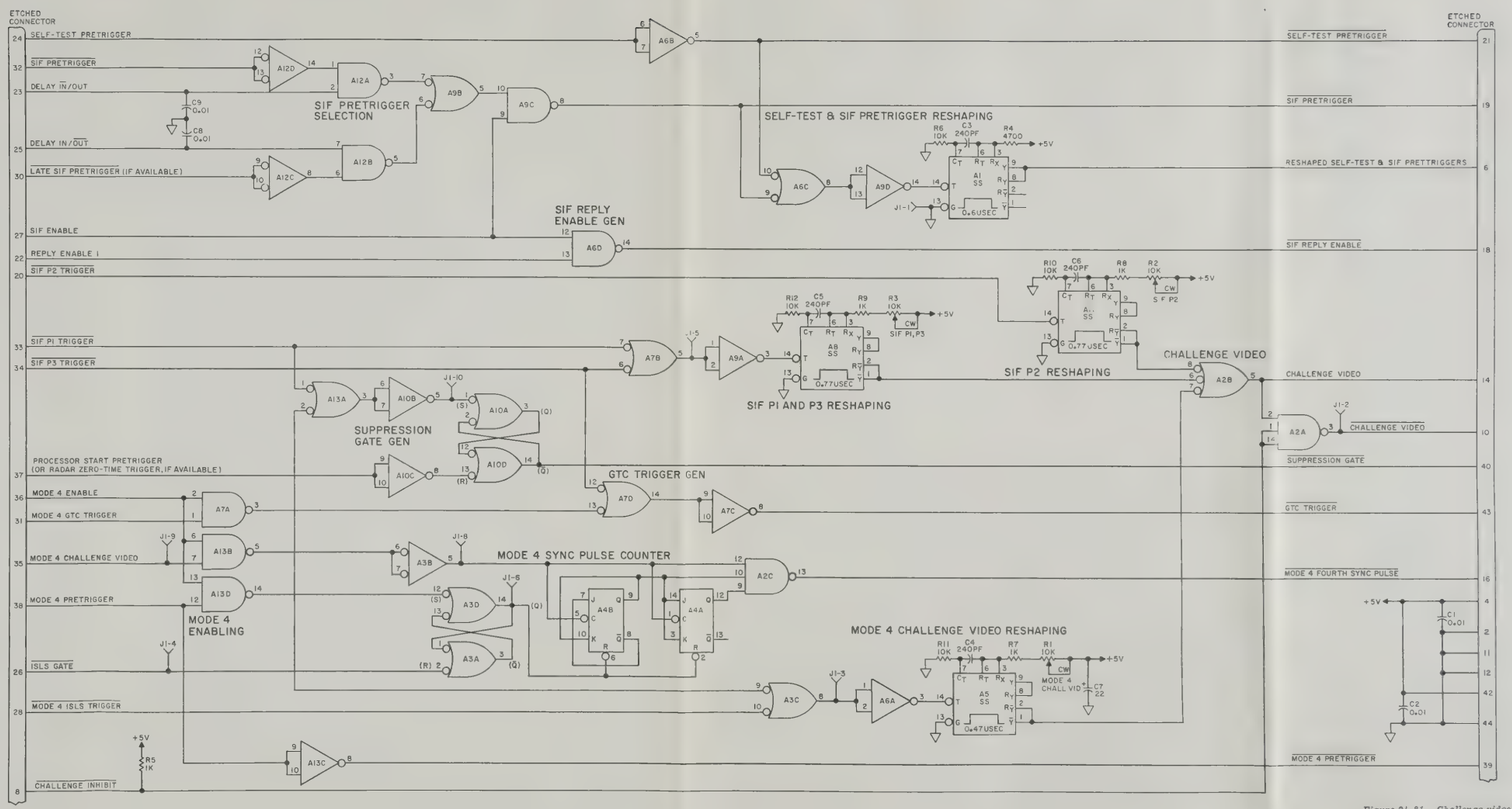

Figure 24-31. Challenge video card 1A2A2A5 schematic diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS:

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A5, A8, A11	SINGLE SHOT	4	1
A2	TRIPLE THREE-INPUT GATE	4	11
A3, A6, A7, A9, A10, A12, A13	QUADRUPLE TWO INPUT GATE	4	11
A4	DUAL J-K FLIP-FLOP	4	11

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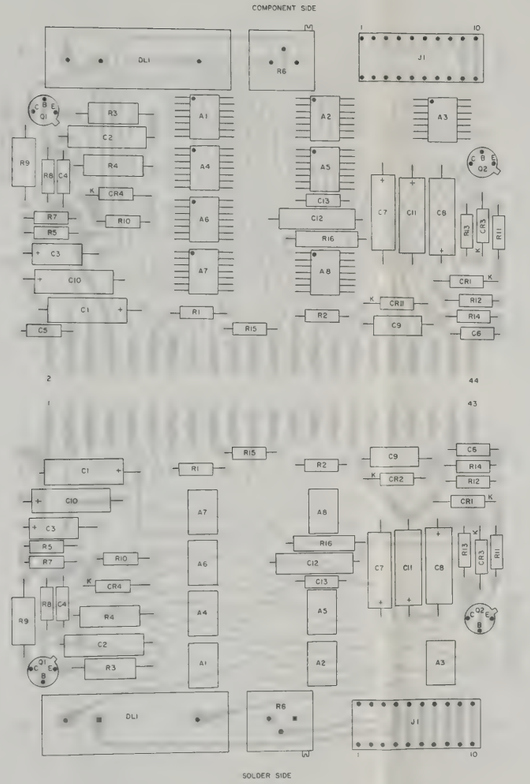

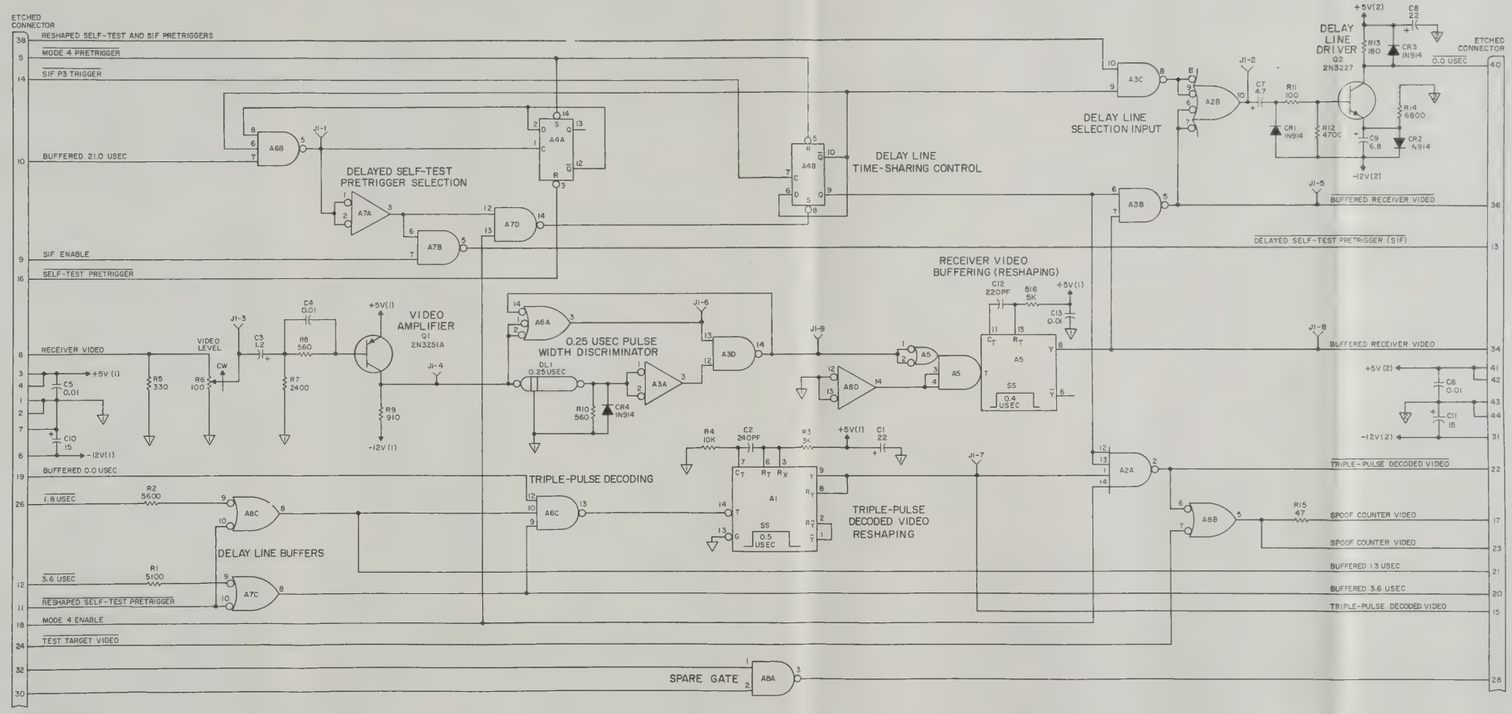

NOTES

1 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, AND CAPACITANCES ARE IN MICROFARADS.

2 INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE LISTED BELOW. INTEGRATED CIRCUITS A2 & A3 ARE CONNECTED TO +5V(2) AND GROUND 2, ALL OTHERS ARE CONNECTED TO +5V(1) AND GROUND 1.

REFERENCE DESIGNATION	DESCRIPTION	+5V P/N	GROUND PIN
A1	SINGLE-SHOT	4	1
A2	DUAL FOUR-INPUT GATE	4	11
A3, A7, A8	QUAD TWO INPUT GATE	4	11
A4	DUAL D FLIP-FLOP	4	11
A5	RETRIGGERABLE SINGLE-SHOT	14	7
A6	TRIPLE THREE-INPUT GATE	4	11

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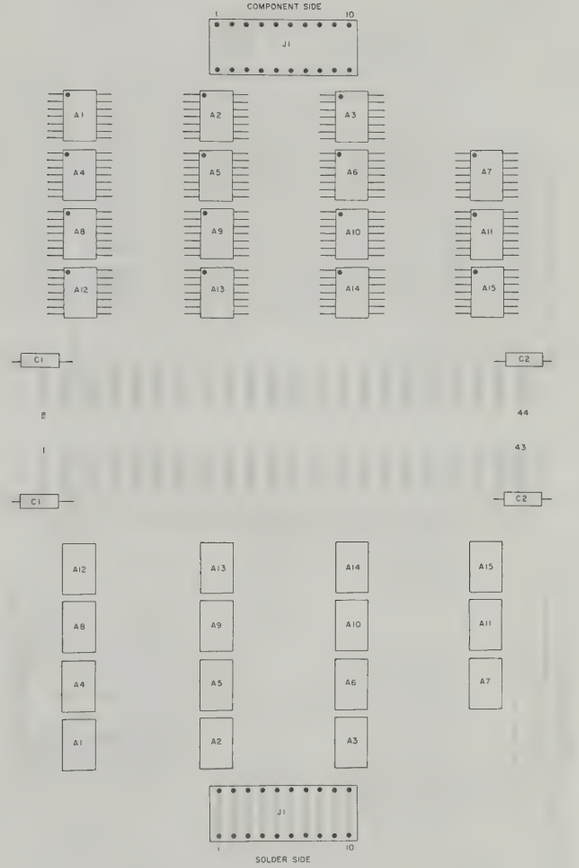
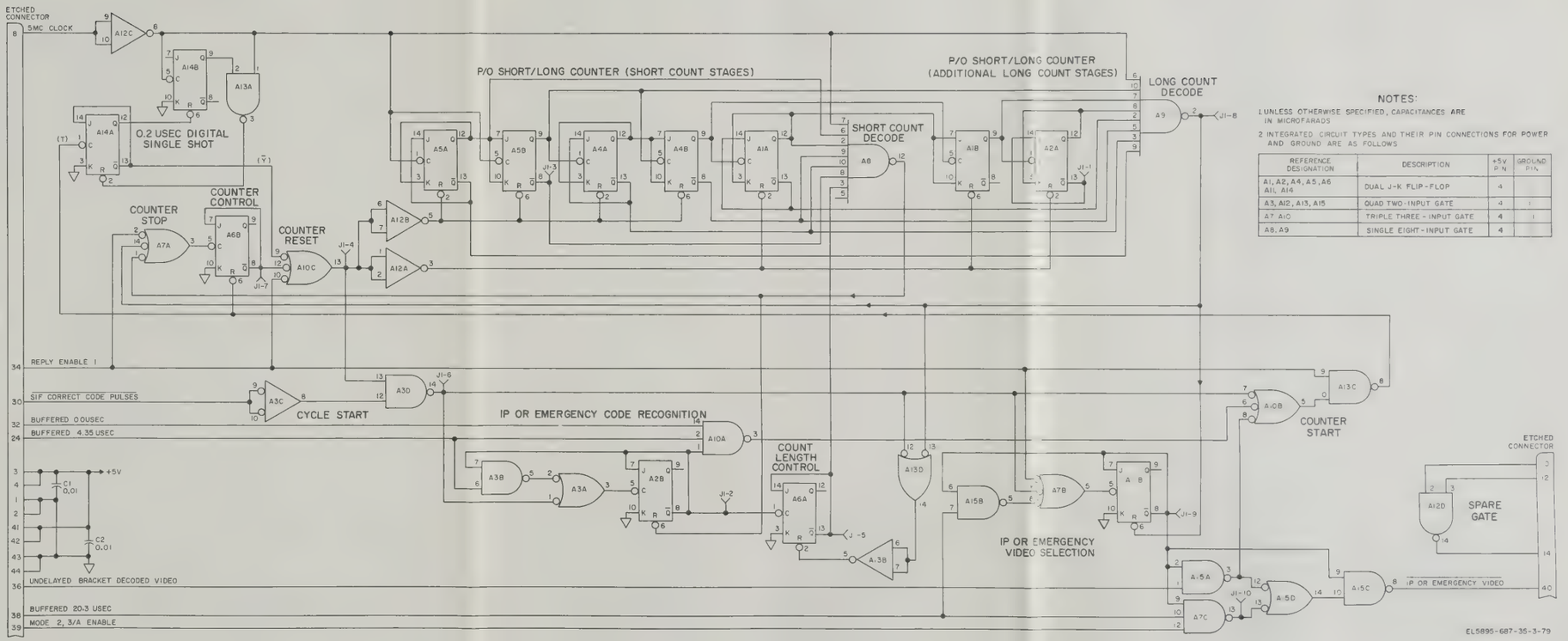
Figure 24-32. Reply video card 1A2A2A6 schematic diagram.



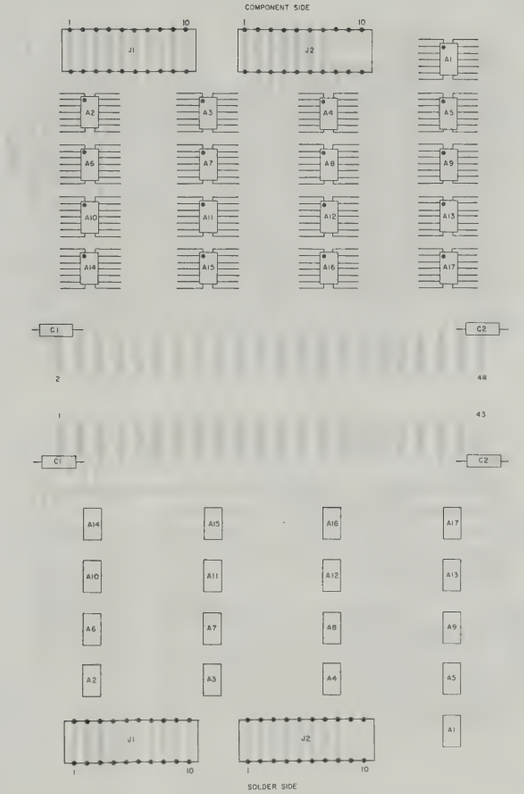


NOTES:

1. UNLESS OTHERWISE SPECIFIED, CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A2, A4, A5, A6 A11, A14	DUAL J-K FLIP-FLOP	4	
A3, A12, A13, A15	QUAD TWO-INPUT GATE	4	1
A7, A10	TRIPLE THREE-INPUT GATE	4	1
A8, A9	SINGLE EIGHT-INPUT GATE	4	

Figure 24-33. I/p and emergency code card 1A2A2A7 schematic diagram.



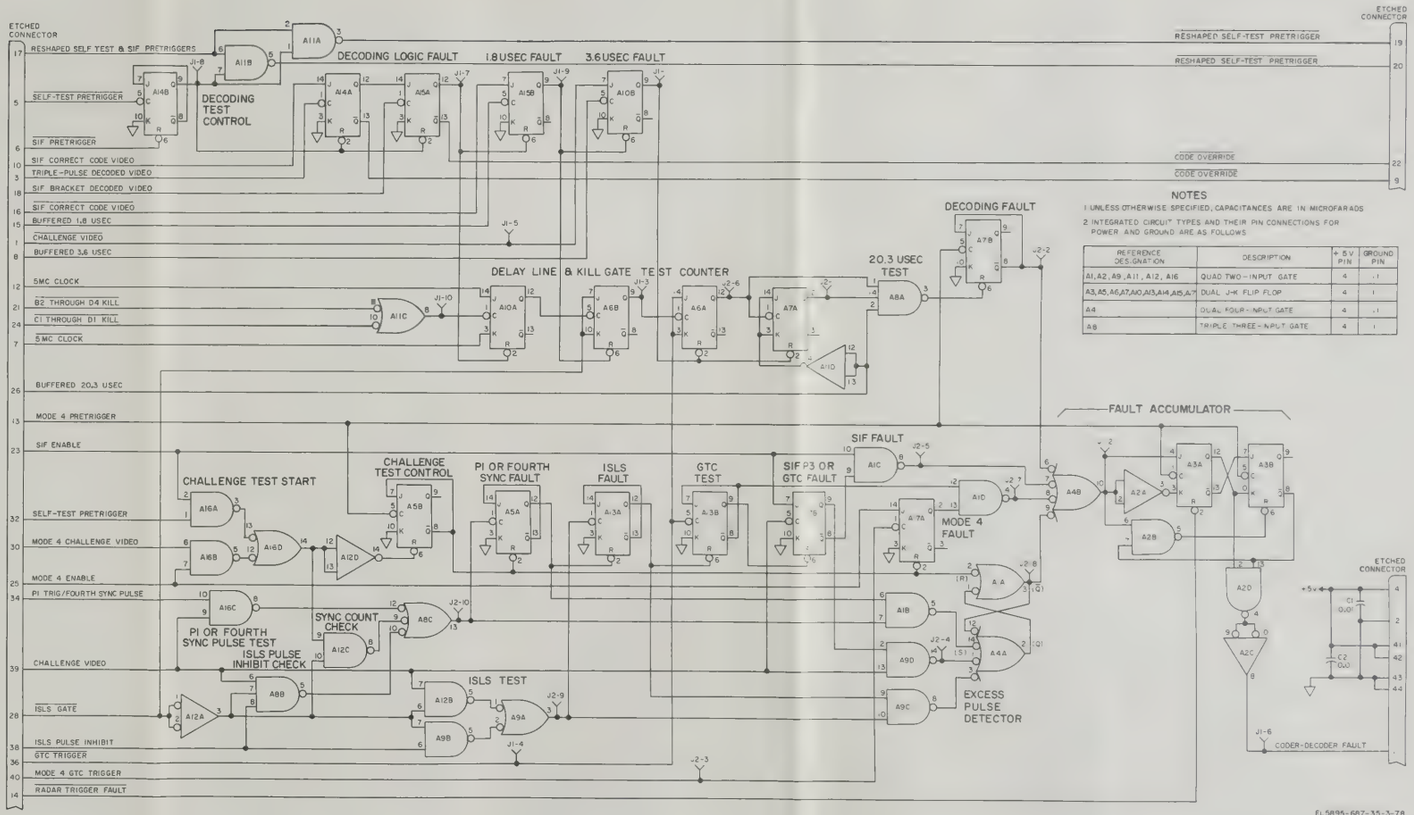


Figure 24-34. Coder-decoder self-test card 1A2A2A8 schematic diagram.

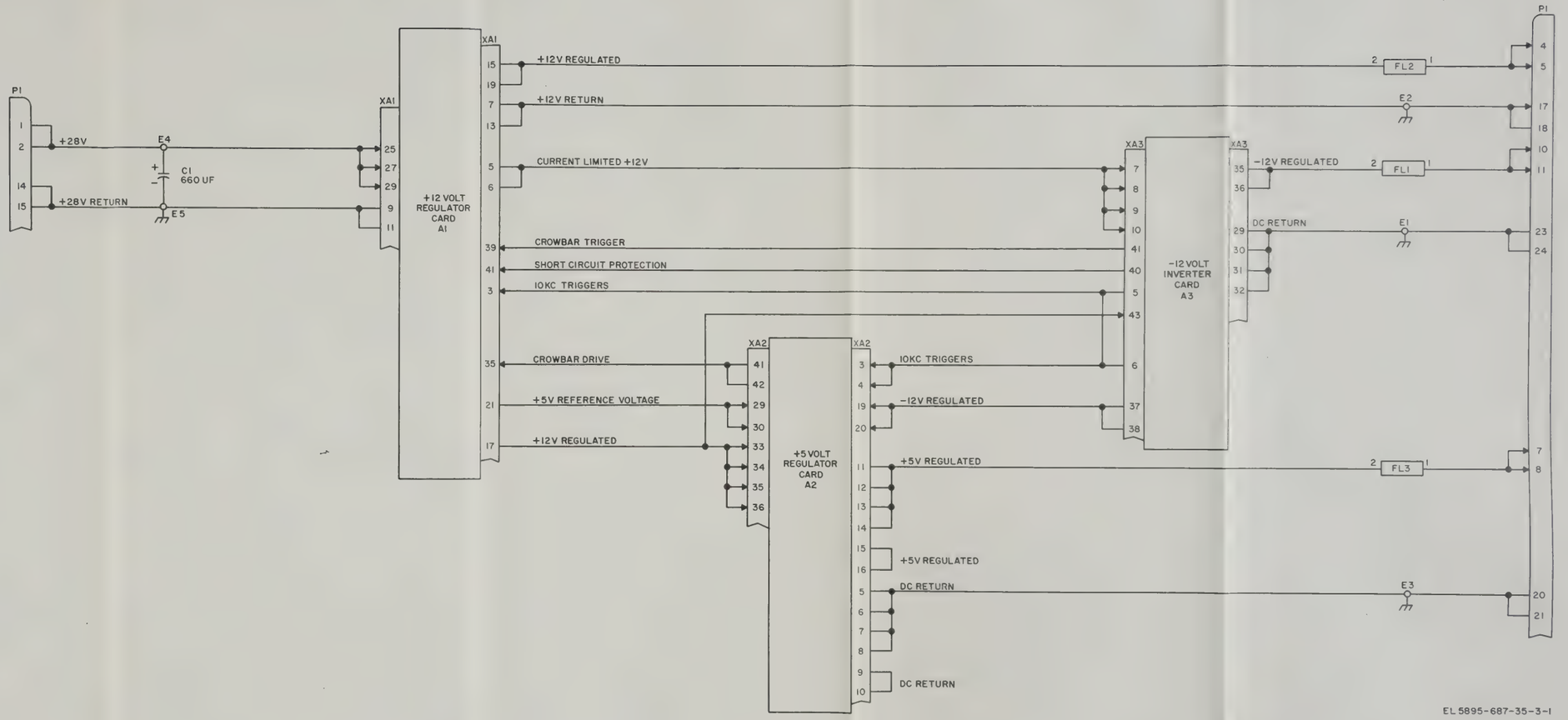
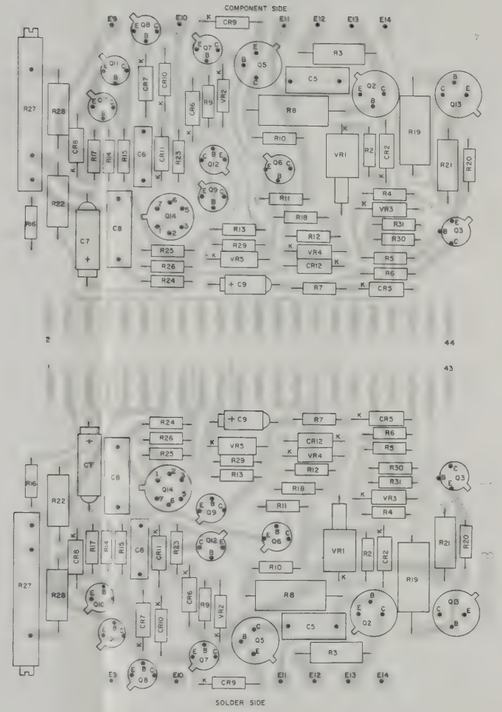
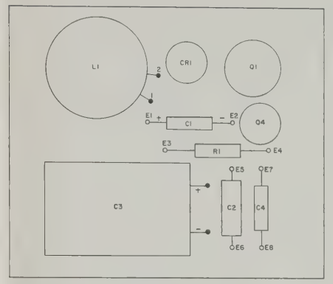


Figure 24-35. Power supply module 1A2A3 schematic diagram.





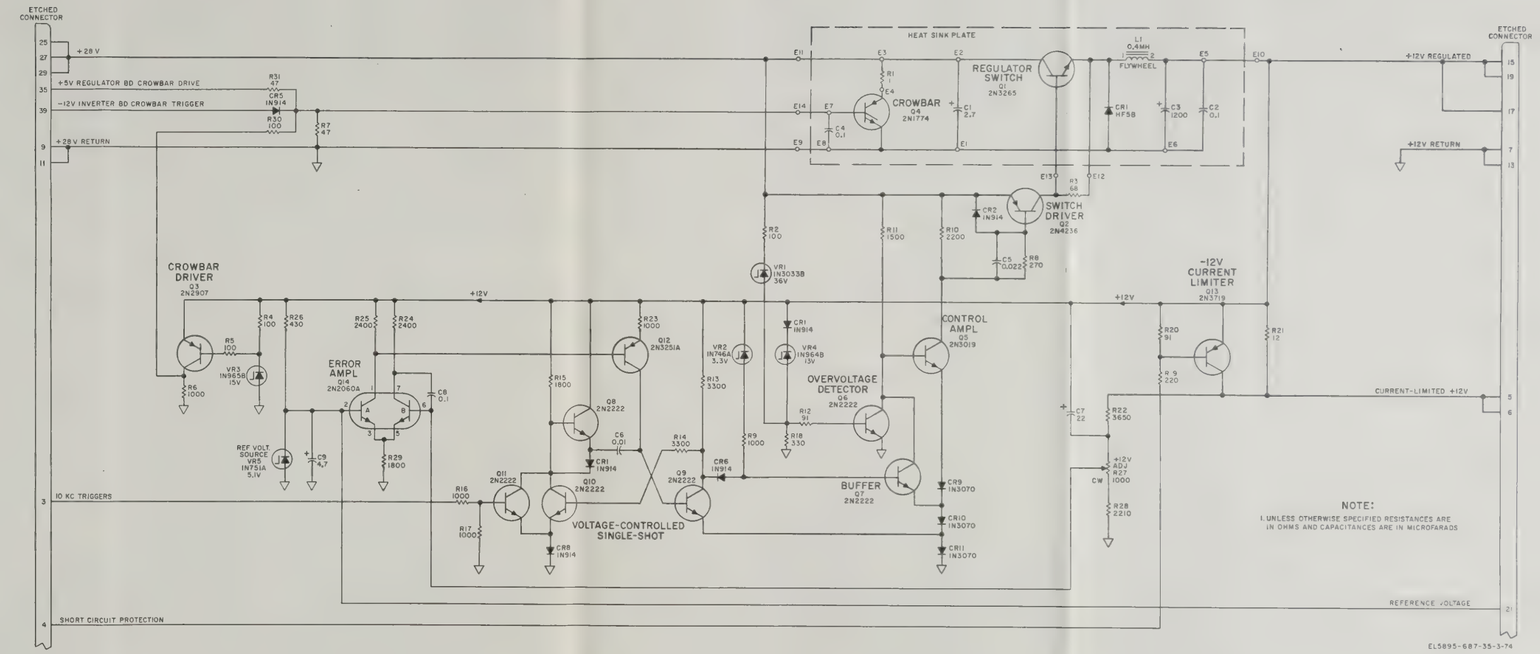
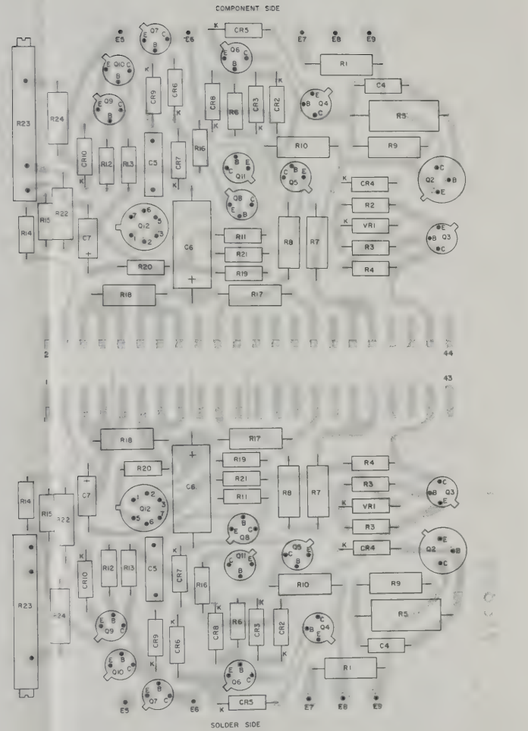
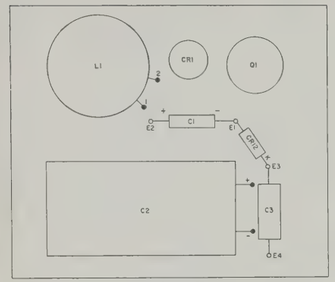


Figure 24-36. +12-volt regulator card 1A2A3A1 schematic diagram.





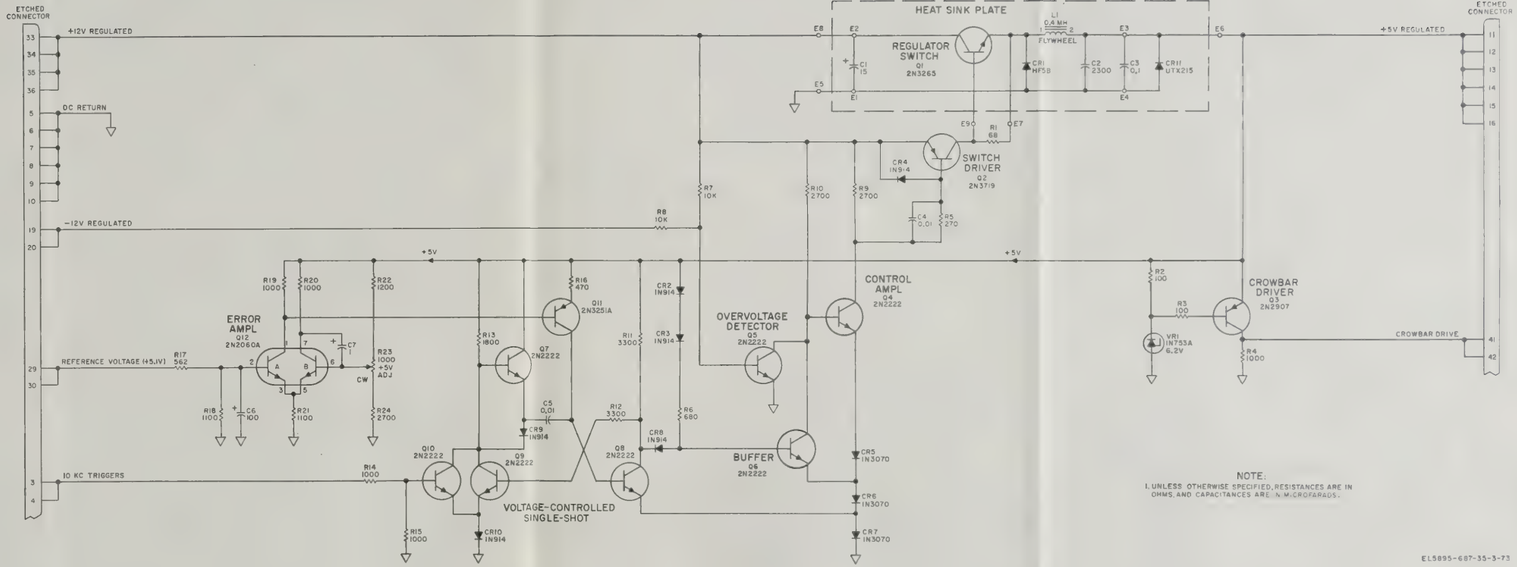
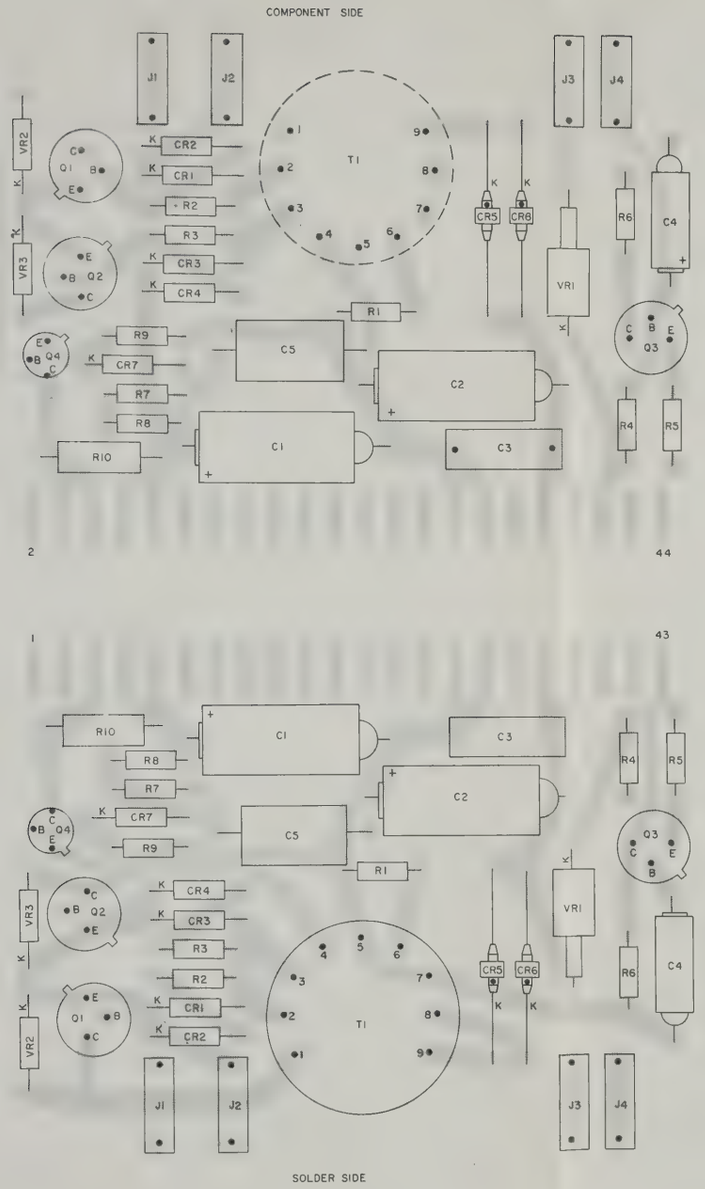


Figure 24-37. +5-volt regulator card 1A2A3A2 schematic diagram.



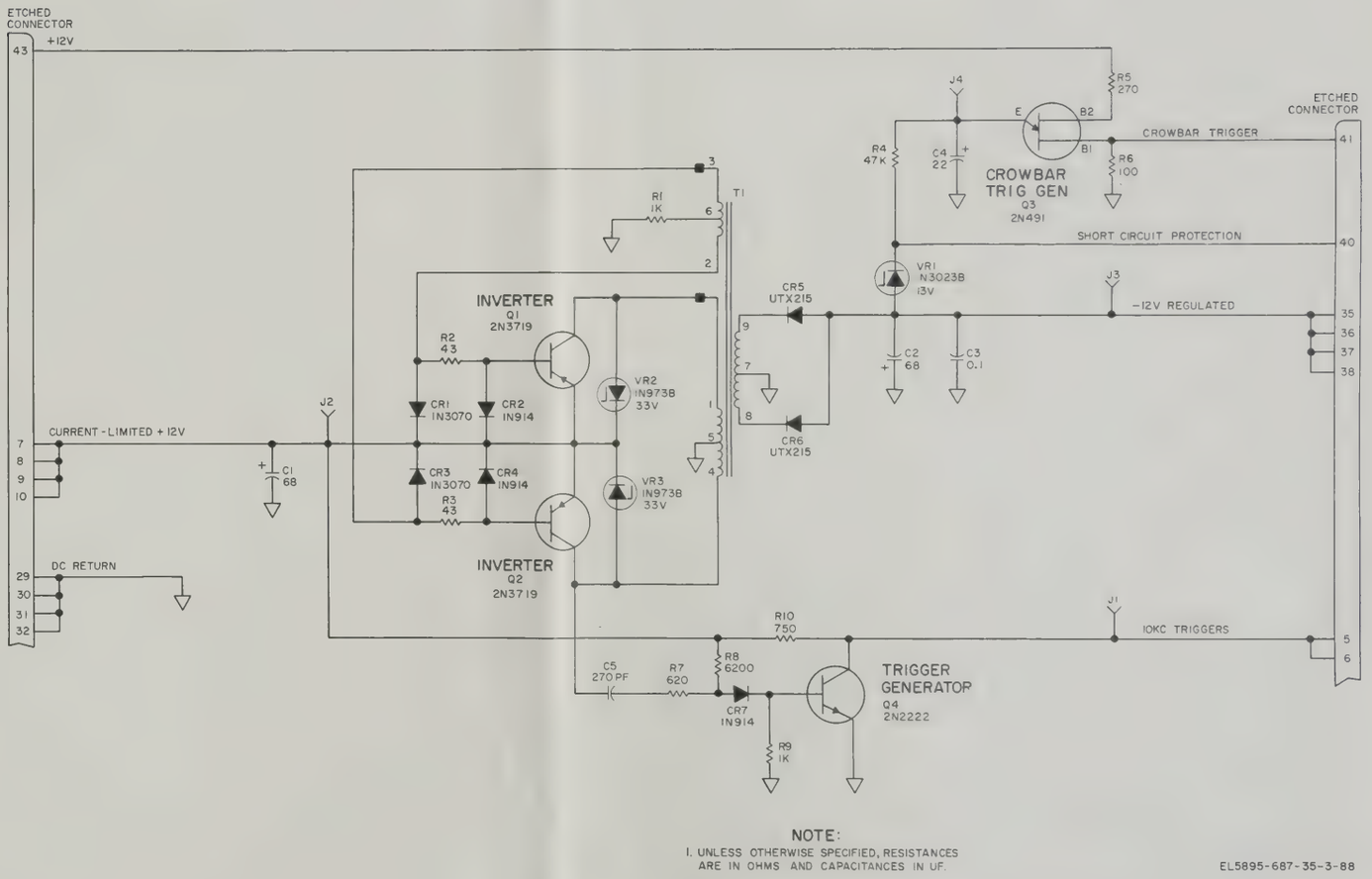


Figure 24-38. —12-volt inverter card 1A2A3A3 schematic diagram.

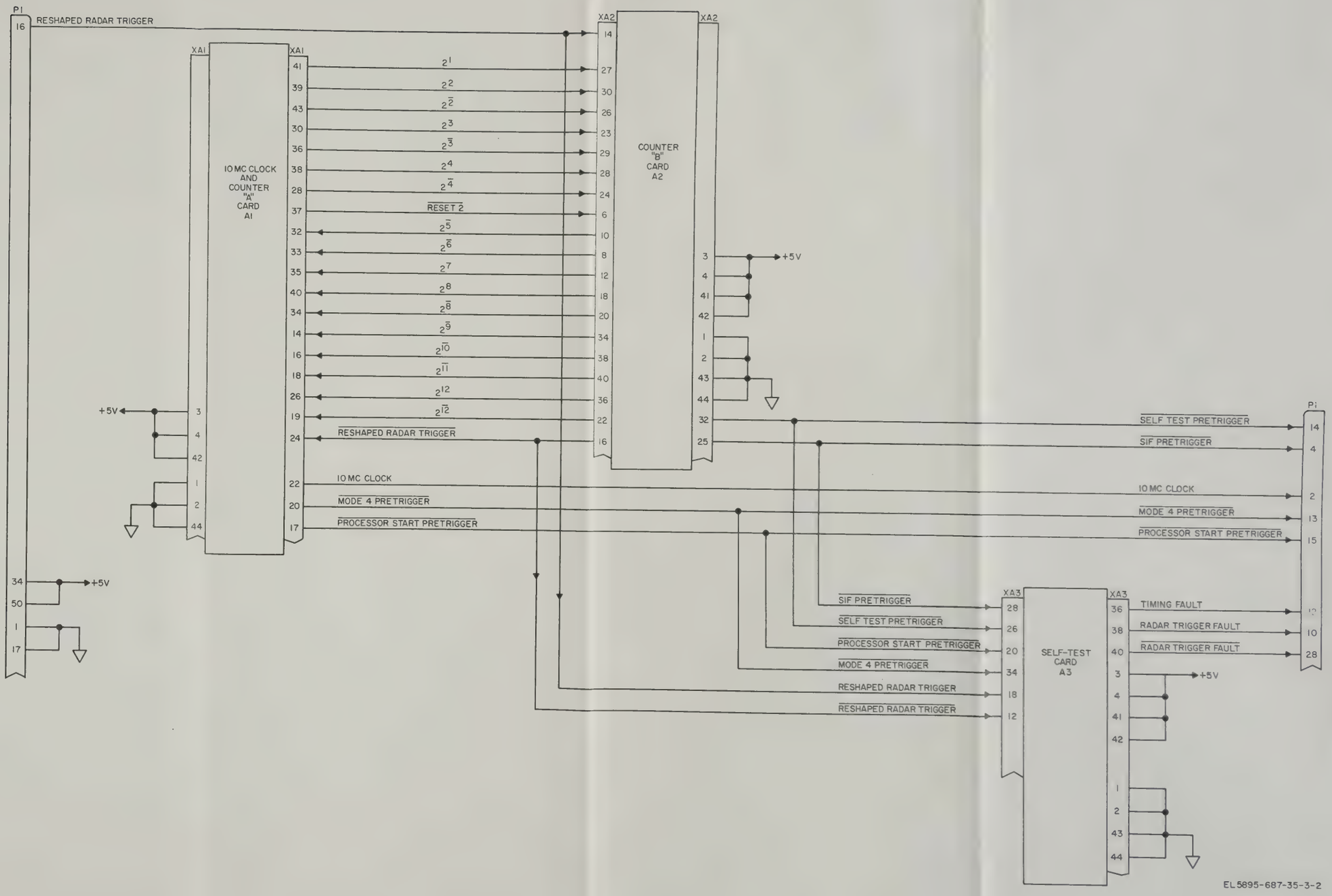
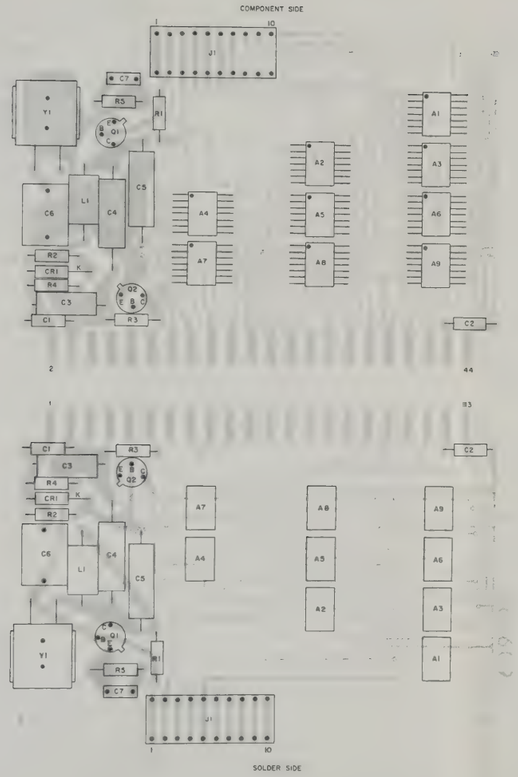
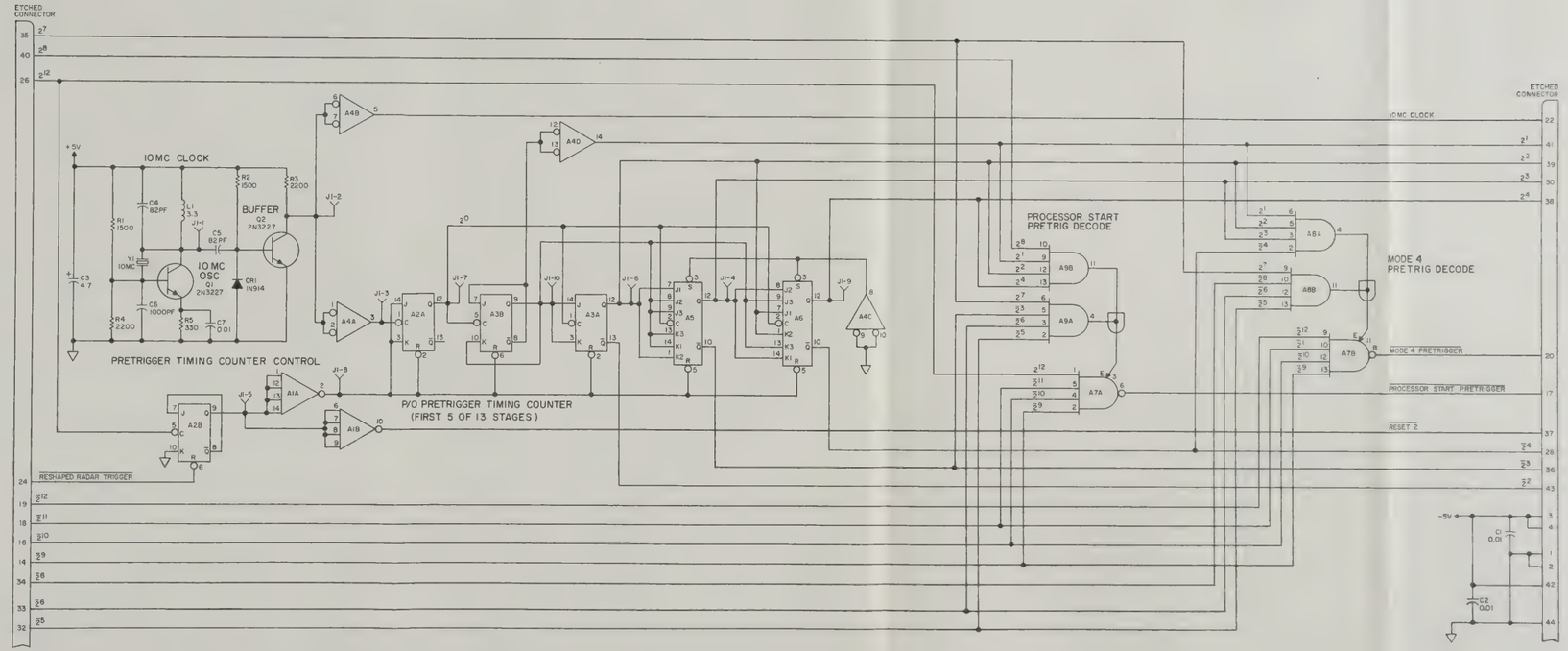


Figure 24-39. Timing module 1A2A4 schematic diagram.





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, AND INDUCTANCES ARE IN MICROHENRYS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1	DUAL FOUR-INPUT GATE	4	11
A2, A3	DUAL J-K FLIP-FLOP	4	11
A4	QUAD TWO-INPUT GATE	4	1
A5, A6	JJJ-KKK FLIP-FLOP	4	11
A7	DUAL EXPANDABLE FOUR-INPUT GATE	14	7
A8, A9	DUAL FOUR-INPUT EXPANDER GATE	—	7

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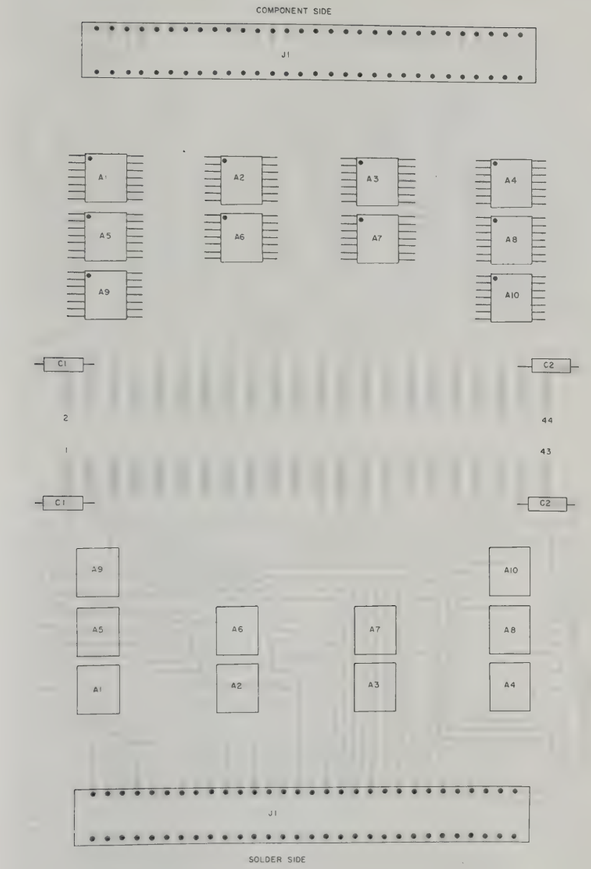
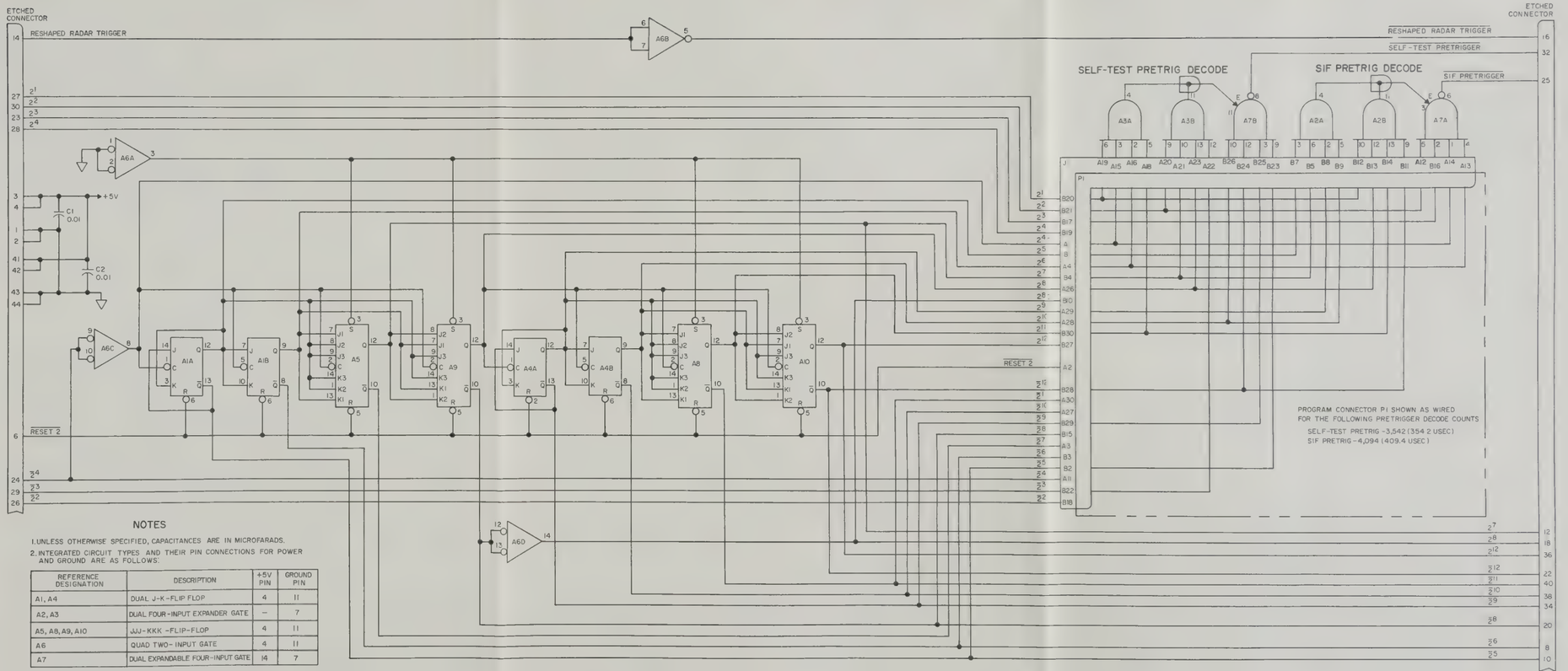
Figure 24-40. 10-mc clock and counter A card 1A2A4A1 schematic diagram.



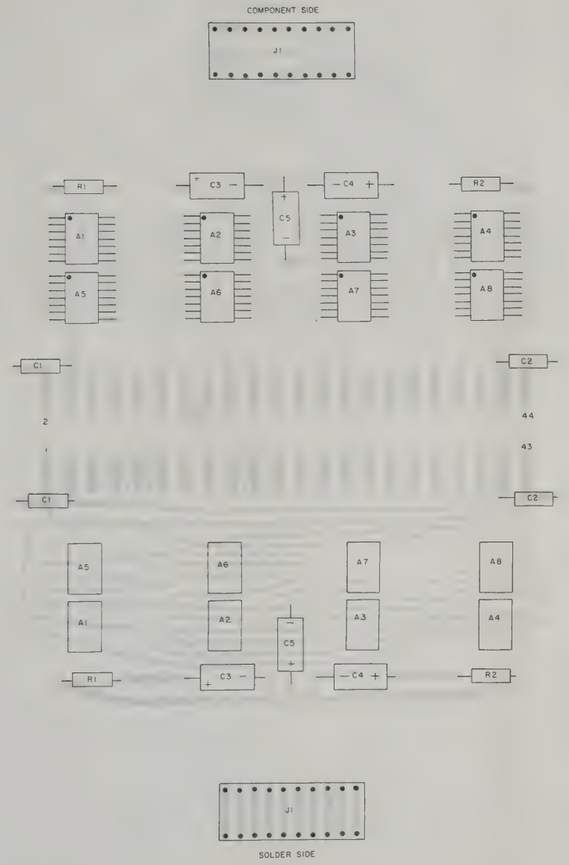


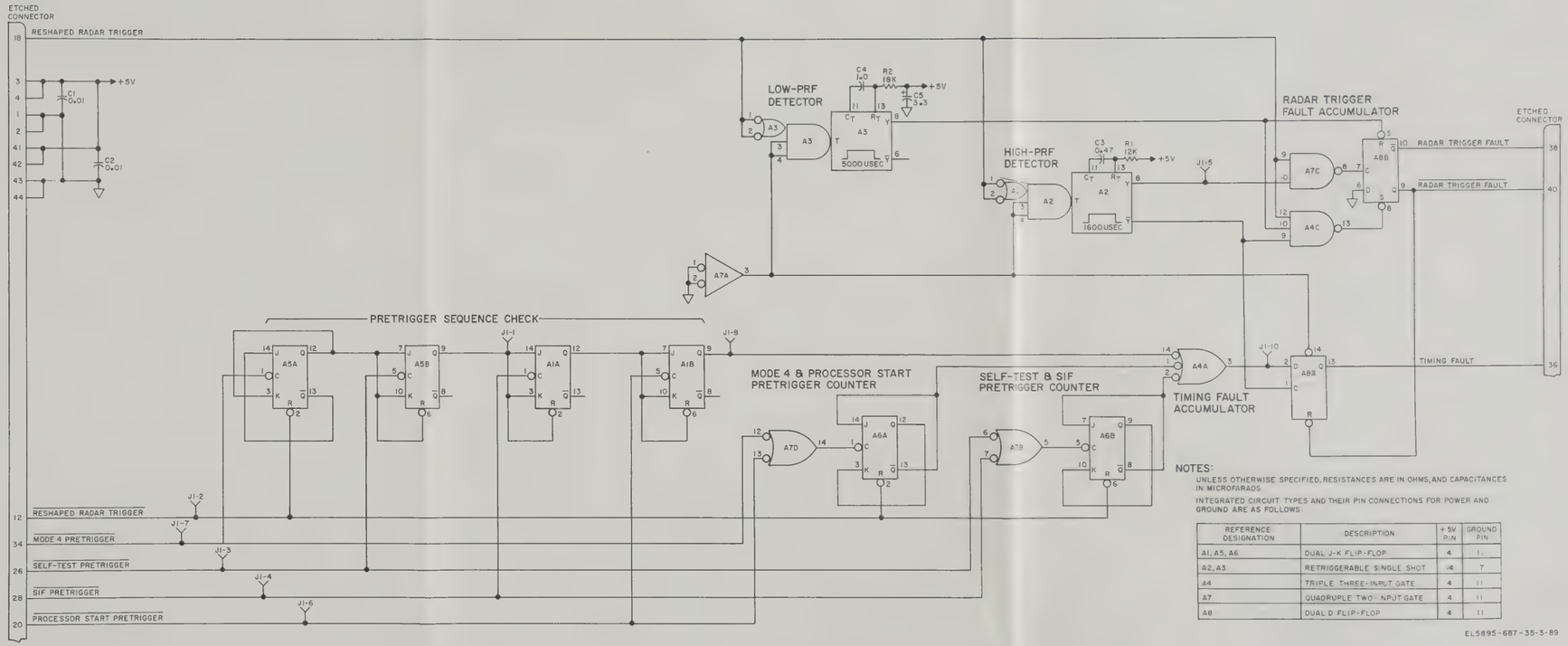
NOTES

1. UNLESS OTHERWISE SPECIFIED, CAPACITANCES ARE IN MICROFARADS.
2. INTEGRATED CIRCUIT TYPES AND THEIR PIN CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS:

REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A4	DUAL J-K-FLIP FLOP	4	11
A2, A3	DUAL FOUR-INPUT EXPANDER GATE	—	7
A5, A8, A9, A10	JJJ-KKK -FLIP-FLOP	4	11
A6	QUAD TWO- INPUT GATE	4	11
A7	DUAL EXPANDABLE FOUR-INPUT GATE	14	7

Figure 24-41. Counter B card 1A2A1A2 schematic diagram.





REFERENCE DESIGNATION	DESCRIPTION	+5V PIN	GROUND PIN
A1, A5, A6	DUAL J-K FLIP-FLOP	4	11
A2, A3	RETRIGGERABLE SINGLE SHOT	14	7
A4	TRIPLE THREE-INPUT GATE	4	11
A7	QUADRUPLE TWO-INPUT GATE	4	11
A8	DUAL D FLIP-FLOP	4	11

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